Liquid Core Waveguide Sensors with Single and Multi-Spot Excitation

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Liquid Core Waveguide Sensors with Single
and Multi-Spot Excitation

Lynnell Uilani Wai Yee Zempoaltecatl

A thesis submitted to the faculty of
Brigham Young University
in partial fulfillment of the requirements for the degree of

Master of Science

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December 2013

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ABSTRACT

Liquid Core Waveguide Sensors with Single and Multi-Spot Excitation

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Master of Science

Using silicon based microfabrication and materials, a photonic platform, capable of single bioparticle analysis, has been developed. This platform combines liquid and hollow core waveguides on the micron-scale (5 µm x 12 µm) to isolate femtoliter sized sample volumes. Fluorescence excitation and signals in the visible range are directed into and out of the sample volume at an orthogonal angle to maximize signal-to-noise.

In order to guide light in a low-index material antiresonant reflecting optical waveguides (ARROWs) were incorporated into the platform. This thesis reveals the development path of these structures over several device generations including innovations in material, geometries, and fabrication techniques to increase detection sensitivity. As a result of these developments, this photonic platform has shown to successfully detect virus samples and other particles.

This thesis also presents a new idea for increasing the signal to noise ratio (SNR) by incorporating Y-splitter devices into the design. Specifically, the 1 x 2 and 1 x 4 splitter structures can be used as orthogonal excitation points to the liquid core waveguide. When fluorescently tagged particles are introduced into the hollow core, these points create an optical signal that is correlated in time and space. The data collected by a photodetector can then be processed by an algorithm to increase SNR. Such advancements have shown to increase the SNR by 175 times.

Keywords: Integrated optics, microfluidics, microfabrication, biophotonics, ARROWs
ACKNOWLEDGEMENTS

This work would not have been possible without the help, collaboration, and support of many people. I would like to thank those who have contributed to making this research project a success.

I thank my advisor, Dr. Aaron Hawkins, for recruiting me as an undergraduate research student in IMMERSE. That experience provided my first exposure to the Cleanroom and microfabrication processes. It also gave me the confidence to apply the skills and knowledge that I have gained throughout my studies in a practical setting.

I am thankful to my first mentor, Mark Hamblin, who trained me on majority of the equipment and procedures that I used throughout my career – both as an undergraduate and a graduate student. Mark taught me how to work carefully, efficiently, and independently. Because of this mentored research opportunity I was prepared and qualified to be accepted into graduate school.

My research continued as a graduate student working closely with Dr. Hawkins. I appreciate the one-on-one guidance, technical training, and teaching moments that he has provided me over the years. His example of being goal-oriented, innovative, and self-motivated has inspired me to develop those same attributes. I also thank the professors on my graduate committee, Dr. Gregory Nordin and Dr. Richard Selfridge for their encouragement and support in this work.

Our lab manager, Jim Fraser, has been extremely helpful in the Cleanroom. He has always been very willing to answer questions, assisted in fixing broken machines, and kept the
work environment safe and clean. My success in this research certainly would not have been possible without his great leadership and kindness.

The training I received from my second mentor, Yue Zhao, was extremely helpful throughout my graduate career. She taught me the fundamental principles and fabrication techniques of my current research. Everything I learned from her became the foundation upon which this research was built. I am also grateful to Yue for the dedication and ownership she demonstrated throughout her time here at BYU.

My colleagues have been a great asset to me during this research experience. Here at BYU, I have worked together with many students on this project: Matthieu Giraud-Carrier, Yaeji Lim, Michael Olson, Thomas Wall, Matthew Stott, and Alan Weinert. I have also collaborated with Dr. Holger Schmidt’s Applied Optics group at the University of California Santa Cruz: Josh Parks, Damla Ozcelik, and Jennifer Black. Thanks to each of you for your insights and contributions to this project.

Above all, I am thankful to my husband Ruben, who has done so much to encourage and inspire me. Ruben’s confidence in my abilities has helped me to persevere through all the late nights and long days. His moral support and reassurance sustained me throughout this work and contributed greatly to my success.
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1 INTRODUCTION

The combination of science and creativity has the potential to greatly improve the way diagnostic medical tests are currently administered. For example, if a man becomes sick and recognizes that he has symptoms of a particular disease, to confirm this diagnosis he often must go to a doctor’s office and provide a biological sample (blood, urine, saliva, etc.). This sample is then taken to a laboratory, whereupon various tests are performed, an analysis is done, and eventually the results are delivered to the patient.

This method of diagnosing a particular illness or disease can be time consuming, taking days or even weeks to complete; instead of using this valuable time to treat the disease, the patient finds himself waiting for test results. Furthermore, the lab equipment and lab technicians that are needed to perform the tests and carry out the analyses make this method expensive and less than ideal.

In the newly emerging Lab on a Chip field, scientists and engineers are developing ways to integrate multiple laboratory functions into one device, thereby eliminating some of the tests and procedures that are performed by lab technicians. Such a device can range from a few square millimeters in size to a few square centimeters and is commonly made on glass, plastic, or silicon substrates.
1.1 **Lab on a Chip**

There are many advantages to using a lab on a chip for diagnostic testing. Figure 1-1, highlights a few advantages of this approach with a simple comparison between a laboratory setting and a lab on a chip.

![Laboratory vs Lab on a Chip](image)

**Figure 1-1: Comparison between a laboratory setting and a lab on a chip.**

First, tests done in a lab require manual analysis and can take a long time to process, whereas a lab on a chip can produce nearly instant analyses at the point of care. This is a much faster method and eliminates the need for a large number of lab technicians. Second, the lab on a chip is very compact and small. Due to its size, it has lower sample consumption and requires less sample volumes from a patient, thereby decreasing unnecessary waste. It also has greater portability because it is self-contained; complex diagnostic tests would not have to pass through a large central laboratory facility. Such a test could be done anywhere – at home, in the car, at work, in the jungle, etc. Even allowing tests to be quickly performed and analyzed while waiting...
in a doctor’s office could greatly speed up treatment. Finally, labs on a chip have low fabrication costs when produced in high volumes. Because of these advantages, a great deal of effort has been put into developing lab on a chip devices with important applications.

1.1.1 Applications

Similar types of quick, compact diagnostic devices are already very well-known. Take, for example, a glucometer (glucose meter). This is used by diabetic patients to measure the approximate concentration of sugar in their blood and only requires a single drop of blood. Another commonly used device is a pregnancy test. With a small sample of urine, a woman can find out whether or not she is pregnant. For both of these tests the results are produced in a matter of seconds to a few minutes.

Figure 1-2: Examples of quick point-of-care tests are a glucometer and pregnancy test.
Many lab on chip devices are dedicated to improving the biomedical field but a majority of them are still in their developmental stages. One review paper discusses the possibilities and challenges of creating biosensors for the monitoring of biological warfare agents [1]. A different group of researchers was able to capture HIV subtypes (i.e., A, B and C) in a microchip and demonstrated repeated, efficient, and reliable results [2]. A third group is developing microfluidic technologies for cancer cell separation and detection but has not yet created a single device that incorporates all of its functionality [3].

1.2 Optofluidics

Labs on chip often integrate microfluidics (the physics, manipulation and study of small amounts of fluids) with optofluidics. Optofluidics refers to a group of devices, typically on the micro-scale, that combines optical and fluidic systems. A few examples include imagers [4], telecommunications elements [5], micro-fluidically tunable lenses and filters [6], [7], and biosensors [8].

The particular photonic platform that is the focus of this thesis relies heavily on integrated optics and was designed for the analysis of single bioparticles [9]. The most critical element of this platform (shown in Figure 1-3) is the orthogonal intersection of a hollow core waveguide and a solid core waveguide. In operation, fluidic reservoirs are placed at opposite ends of the hollow core to introduce liquid samples into the core, resulting in a liquid-core waveguide.
1.3 **Liquid Core Waveguides**

In a liquid core waveguide, light is guided through aqueous fluids with low losses. One way this is possible is by using the Anti-Resonant Reflecting Optical Waveguide (ARROW) principle [10], [11], [12]. Bioanalysis is done when fluorescently tagged molecules within the liquid sample are excited as they flow past the orthogonal solid core. The resulting fluorescence signal is confined in the liquid core and guided into another solid-core waveguide that directs it off the chip. At the edge of the chip the signal is collected by a photodiode and can be quantified and analyzed. The remainder of this thesis will focus on the design, fabrication and improvements of these silicon-based optofluidic waveguide platforms. It will also summarize a few tests that were performed along with the data and the results that were found.

1.4 **Contributions**

The research in this thesis takes three different improvements that were previously made to the optofluidic ARROW platform (on separate occasions) and incorporates them into one
structure. Because of the combination of these improvements, the completed devices were able to successfully detect single RNA (Appendix A.2 Conference Papers and Presentations.2). This work focuses heavily on the specific improvements that were made and how the modifications were incorporated into the fabrication process. In addition, a separate microfluidic layer was designed to mix the sample with a fluorescent label and was then integrated with the planar optical layer (Appendix A.2 Conference Papers and Presentations.1, Appendix A.2 Conference Papers and Presentations.4).

Also, a convenient method is introduced in the middle of the fabrication process that measures the thick top layer of oxide. This required several experiments with the Filmetrics 20 Film Measurement System to ensure that the measurements were accurate. With this new way of measuring the oxide part way through the fabrication process, time is saved and layers can be grown with greater accuracy.

Another major focus of this thesis is related to acquiring multiple excitation spots in the liquid core waveguide. This thesis reviews the design, fabrication, and testing that went into these structures. Because of this upgrade in the optofluidic ARROW platform, signal to noise ratios were dramatically increased (Appendix A.2 Conference Papers and Presentations.3).
2 THE BASIC ARROW

This chapter serves to present background information about the ARROW. In order to understand the benefits of using an ARROW, a review of total internal reflection is presented. Next, the design of the ARROW is described and the following section explains the general steps of fabrication.

2.1 Total Internal Reflection

Snell's law relates the angles of incidence and refraction of a light beam to the indices of refraction of the materials. This relationship is given by,

\[
\frac{\sin \theta_1}{\sin \theta_2} = \frac{n_2}{n_1}.
\] (2.1)

Figure 2-1 shows three different ways that the incident light may bend. The critical angle, \( \theta_c \), is defined as the incident angle at which the refracted angle will be 90\(^\circ\). This can be seen in Figure 2-1b. The first case, Figure 2-1a, illustrates a general case, such that the incident angle is less than the critical angle and the third case, Figure 2-1c, shows the case when the incident angle is greater than the critical angle. This third case is called total internal reflection because
the wave gets reflected back into the first medium. Total internal reflection (TIR) is only valid when \( n_1 \) is greater than \( n_2 \); otherwise, the \( \sin^{-1}(n_2/n_1) \) will be undefined. TIR can be used to contain an electromagnetic wave inside a medium if Snell's law is satisfied.

![Figure 2-1: Incident angles explained by Snell's law.](image)

2.2 Design

The optofluidic platform discussed throughout this thesis requires a liquid-filled hollow core. The layers of material surrounding the hollow core are called cladding layers and typically have a higher index of refraction than the liquid within the core. Table 2-1 shows the index of refraction for a few materials that are relevant to this research.
Table 2-1: Index of refraction for various materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Index of Refraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air</td>
<td>1.000</td>
</tr>
<tr>
<td>Water</td>
<td>1.333</td>
</tr>
<tr>
<td>Silicon Dioxide (SiO₂)</td>
<td>1.457</td>
</tr>
<tr>
<td>Silicon Nitride (SiN)</td>
<td>2.016</td>
</tr>
<tr>
<td>Tantalum Oxide (Ta₂O₅)</td>
<td>2.275</td>
</tr>
</tbody>
</table>

Air has the lowest index of refraction. Water has the next lowest index of refraction at 1.33 which is less than any option for cladding materials. In order for TIR to work, the reverse case is required— the index of refraction of the guiding material should be greater than the cladding material – so the TIR condition is not satisfied for water surrounded by these materials. Because TIR cannot be used to confine light, a different method of guiding light must be used for aqueous cores.

2.2.1 Fabry-Perot Reflectors

Rather than using TIR, a waveguide has been developed that incorporates Fabry-Perot reflectors [13]. Such reflectors are positioned parallel to each other and can be designed so that an anti-resonant etalon is produced. Figure 2-2 shows the transmission of a Fabry-Perot reflector as a function of phase shift for surface reflectivities of 0.5, 0.7 and 0.9. Anti-resonance occurs when the phase shift is equal to \( \left( m + \frac{1}{2} \right) \pi \). When this condition is met, transmission is
nearly zero and light is reflected back into the core [14]. This method of guiding light is favorable for the design of these waveguides since it allows light to be guided within a low-index material.

![Figure 2-2: Transmission of a Fabry-Perot Etalon as a function of phase shift.](image)

### 2.2.2 Cladding Thickness

This design requires that a specific index of refraction correspond to a calculated thickness as found by Equation (2.2),

\[ t_j = \frac{\lambda}{4n_j} (2m + 1) \left(1 - \frac{n_c^2}{n_j^2} + \frac{\lambda^2}{4n_j^2d_c^2}\right)^{-1/2}. \]  

(2.2)
This equation is valid for integer values of anti-resonance order \( m \) such that \( t_j \) is the thickness to be deposited, \( n_j \) is the index of refraction for the \( j \)th layer, \( n_c \) and \( d_c \) are the index of refraction and thickness of the core, and \( \lambda \) is the wavelength [11]. The transverse component of the wave vector will be reflected into the core and remain there if these parameters are met.

### 2.2.3 Cladding Layers

Named after their anti-resonant reflecting properties, these types of waveguides are called Anti-Resonant Reflecting Optical Waveguides (ARROWs). They are designed so that the leaky modes of the waveguide can be confined within a low-index core. The hollow core can now be filled with a liquid sample that is surrounded by multiple, alternating cladding layers of different refractive indices [15]. Light confinement is improved with multiple cladding layers. Figure 2-3 shows a generic side view of an ARROW and illustrates this principle. A wave, traveling in the \( z \)-direction, will be confined to the core if the cladding layers are designed to act as Fabry-Perot reflectors.

![Figure 2-3: Side (cross-section) view of a generic ARROW structure. Waves travel in the z-direction and are constrained inside the hollow core. Cladding layers of indices \( n_1 \) and \( n_2 \) surround the low-index core, \( n_{core} \).](image)
2.3 **Fabrication of Optofluidic Platform**

Construction of this optofluidic platform relies on standard silicon-based microfabrication techniques. Fabrication processes were done in the Integrated Microfabrication Lab (IML) at Brigham Young University (BYU). Figure 2-4 illustrates the basic process flow.

![Figure 2-4: ARROW platform fabrication steps: (a) ARROW layers deposited. (b) Sacrificial core patterned. (c) Top oxide layer deposited. (d) Ridge waveguides etched into top layer. (e) Sacrificial core exposed and removed. (f) Reservoirs attached.](image)

2.3.1 **Bottom Cladding Layers**

Using a four inch silicon wafer, this process begins with the deposition of ARROW cladding layers. They are deposited with a Plasma-Enhanced Chemical Vapor Deposition (PECVD). These cladding layers consist of alternating films of dielectric materials, silicon dioxide (SiO$_2$) and silicon nitride (SiN), and have an index of refraction between 1.5 and 2.1.
The purpose of these bottom cladding layers is to prevent light from leaking into the substrate. The design requires a stack of six bottom layers that alternate between materials. The thicknesses are predetermined by Equation (2.2).

2.3.2 **Sacrificial Core**

Then, a sacrificial waveguide core is patterned over the bottom layers using SU-8. It is referred to as a sacrificial core because its only purpose is to create a mold that the top layers will cover. Eventually, the SU-8 material gets etched out and the top cladding layers become the top and side walls that create the hollow-core waveguide. The target height and width for these cores are 5 µm and 12 µm, respectively.

Basic photolithography methods allow for accurate transfer of a design onto a wafer and are used to create the sacrificial core. This process incorporates a light sensitive material (photoresist), UV radiation, and a developing solution. The steps are summarized in Figure 2-5. First, a coat of photoresist is spun onto the base. In this research, SU-8 is spun onto the silicon substrate (over the bottom cladding layers). Then, a photomask containing the design is used to cover the wafer while it is exposed to UV radiation. This has a different effect on the photoresist depending on whether it is negative or positive. For negative resist, the areas that are exposed to the radiation become resistant to the developing solution, while the opposite is true for positive resist and the exposed areas become susceptible to it. After development the design from the photomask is directly transferred onto the wafer with positive resist and it is inverted onto the wafer with negative resist. Then, the base is etched, the resist is stripped, and the design is successfully transferred onto the wafer.
Since SU-8 is a negative resist the design of the sacrificial core can be directly transferred onto the wafer. The width of the core is controlled by the design on the photomask and the height of the core can be controlled by the spin speed, cure times, and exposure times of the resist. After developing the SU-8 it is not necessary to continue with an etch step because the purpose of the
sacrificial core is to create a mold for the hollow core. The core remains in place throughout the process until the last step when it is etched out.

2.3.3 Top Cladding Layers

Next, the top cladding layers are deposited over the sacrificial core using PECVD. Like the bottom layers, these layers consist of alternating films of dielectric materials: silicon dioxide (SiO₂) and silicon nitride (SiN). They also have a stack of six alternating layers. Their purpose is to prevent light from leaking out of the waveguide. They also serve as a platform through which solid ridge waveguides can be etched.

2.3.4 Ridge Waveguides

After depositing the top layers, the intersecting solid-core waveguides are patterned with the same SU-8 photolithography process as the hollow core (Figure 2-5). Unlike the core recipe that stops after development, this step continues the process by using the SU-8 pattern as a mask while etching into the top cladding layers. Reactive Ion Etch (RIE) and Inductively Coupled Plasma (ICP) are used. Once the ridge is etched the SU-8 is completely removed.

2.3.5 Core Expose

The last step requires the core ends to be exposed so that an acid etchant has access to the sacrificial core and can remove it. This is done with a positive photolithography step. The mask is designed such that all features are covered by resist except for the two ends of the sacrificial core. The resist serves to protect the core and ridges while the top cladding layers are etched and the two ends of the sacrificial core are exposed. This etch can be either a dry etch or a wet etch.
but the top layers must be entirely removed. Once the cores are exposed they are ready to be etched out. An acid etchant that takes about five to seven days to completely remove the SU-8 is used. This concludes the fabrication phase of the platform.

2.3.6 **Fluid Reservoir**

In order to integrate fluids into the platform, fluid reservoirs are then attached to the ends of the core. These reservoirs can introduce a fluid into one end of the waveguide and collect it at the other end. Fluid flow can be controlled using a pumping system.
3 THREE MAJOR IMPROVEMENTS

The fabrication technique, geometries and materials used in the process outlined in Figure 2-4 affect the performance and detection sensitivity of these waveguides. Optical performance is generally described as overall optical throughput $T$ and is calculated by Equation (3.1).

\[ T = e^{-\alpha_{sc}l_{sc}}\kappa^2_{i} e^{-\alpha_{lc}l_{lc}}. \]  

The length of the solid core is $l_{sc}$ and the length of the liquid core is $l_{lc}$. Propagation losses in the solid core and liquid core are $\alpha_{sc}$ and $\alpha_{lc}$, respectively. Such losses in the solid core happen because of absorption in the films and scattering from the roughness of the walls of the waveguide. Similarly, losses in the liquid core are also due to wall surface roughness. The value for $\kappa_i$ represents the interface efficiency [16], meaning the amount of light coupled between a solid-core and hollow-core waveguide. These losses can be contributed to non-uniform deposition of the top films of the waveguide which tend to cause a crevice at the interface. Figure 3-1 illustrates each of these parameters.
Over the course of multiple years and device generations, many adjustments have been made to the design to improve the optical performance of the ARROW-based platform. The sections below highlight three separate advances that have previously been made. As part of this research, each of the following modifications was applied to a single generation of devices. These changes have greatly improved the optical performance of the waveguides.

3.1 Fabrication Technique

3.1.1 Crevice Problem

One limitation in the fabrication of the basic ARROW platform is caused by non-conformal PECVD growth. The interface efficiency $\kappa_i$ decreases as the boundary between the solid and liquid core waveguides fail to create a smooth transition. Figure 3-2 shows an example of this scenario. Due to a faster growth rate on horizontal surfaces than vertical surfaces,
chemical vapor deposition (CVD) creates a seam in the core overcoat and weakens the structure, especially at the bottom corners of the hollow core. This can cause a crack to form during sacrificial etching [13]. It also greatly decreases the transmission of the device because the solid-core waveguide is effectively thinner than the hollow-core waveguide at the boundary seam, which creates optical mode mismatch.

Figure 3-2: Scanning Electron Micrograph (SEM) showing a crack that formed in the top layer of SiO$_2$ at a corner seam during sacrificial core removal.

3.1.2 Solution to Crevice Problem

The solution to the crevice problems was to “overgrow” the SiO$_2$ layer as seen in Figure 3-3. Since the crevice cannot be completely eliminated, some of the effects of mode mismatch can be avoided by making the lowest point of the crevice corner line up more closely to the top of the liquid-core waveguide [17]. This allows the light transitioning between the solid and liquid-core waveguides to be coupled with less loss.
Results of Improved Fabrication Technique

Increasing the thickness of the top oxide layer from 3 µm to 6.23 µm produced the results summarized in Figure 3-4. These results include both optical simulations as well as experimental measurements. The average loss coefficient for solid-core waveguides was 1.63 cm\(^{-1}\) with a standard deviation of 0.36 cm\(^{-1}\). The average hollow-core loss was 2.19 cm\(^{-1}\) with a standard deviation of 0.42 cm\(^{-1}\). The average coupling efficiency \(\kappa_i\) was calculated for each sample and plotted versus the thickness of top SiO\(_2\) in Figure 3-4. Increasing the top oxide from 3 to 6.23 µm effectively increased the throughput, \(T\), by 17.1 times [17].
3.1.4 Single Over-Coating

For these devices to behave according to theory, it is necessary that the thickness of each ARROW layer be exact according to Equation (2.2). This can be very difficult to produce because of limitations with fabrication. In addition to fluctuations in thickness, these top layers tend to decrease the interface efficiency, introduce surface defects, and cause mode mismatch.

To address this issue, another improvement has been made in the fabrication process: the alternating top cladding layers were removed and replaced with a single over-coating (SOC) of oxide [16]. This design allows for light to be coupled from the solid core directly into the hollow core without needing to pass through several top layers. Light is still confined below by the
ARROW principle and it is confined above by TIR (using the oxide-air interface) if the thickness of the oxide satisfies Equation (2.2).

Without these layers, the interface efficiency, $\kappa_i$ from Equation (3.1), decreases but the loss in the hollow core increases. The effect of lowering $\kappa_i$ outweighs the effect of increasing waveguide loss so this change will still improve the overall transmission. The fabrication process remains the same except for removing the alternating top cladding layers and depositing a single thick layer of SiO$_2$ instead. This is shown in Figure 3-5.

![Figure 3-5: Single over-coat of oxide](image)

3.2 Geometries

3.2.1 First Generation ARROW

Another limitation to the basic ARROW platform was found in its geometry. Figure 3-6 illustrates first-generation ARROW structures that were built on a flat substrate with thick SiO$_2$
as its terminal lateral layer. This design allows for light to leak into the thick oxide layers surrounding the hollow core (to the right and left as shown in the figure), thereby increasing optical loss.

![Figure 3-6: First generation ARROW platform on flat substrate.](image)

3.2.2 **Self-Aligned Pedestal**

To address the problem of light leaking into the thick oxide layers the design was modified so that the hollow ARROW core would be terminally surrounded by air on three sides [18]. Air terminated waveguides (Figure 3-7) were realized by depositing top cladding layers over sacrificial cores and self-aligned pedestals (SAPs).
3.2.3 Fabrication of Self-Aligned Pedestal

These pedestals are created by RIE etching into the bottom substrate using the core as an etch mask. A nickel film is added over the photoresist core (the same sacrificial material as previously used). The nickel serves as a robust etch mask that can withstand the RIE bombardment while leaving the underlying photoresist intact. The rest of the fabrication steps, including CVD over-coating, remain the same. This process is summarized in Figure 3-8. An SEM of the first generation SAP ARROW can be seen in Figure 3-9.
3.2.4 Result of Improved Geometry

Making this change in the geometry of the waveguide has shown to decrease loss; at 785 nm, a 5.8 µm x 12 µm waveguide demonstrated an average loss of 2.19 cm⁻¹ [19]. This represents a decrease of about 50% compared to the previous design.

3.3 Materials

3.3.1 Photoluminescence

A third limitation of the basic ARROW platform stems from the materials initially used. It is important that these materials produce a minimum amount of photoluminescence (PL). Luminescence describes the emission of radiation from a solid when it is supplied with some form of energy [20]. In other words, PL arises from the absorption of photons, and, when produced by an excitation beam, results in optical noise. Since the intended use of the optofluidic
platform is to measure fluorescence, this type of noise interferes with the signal that is produced and is therefore undesirable.

3.3.2 **Tantalum Oxide**

Former ARROW layers were made using SiN and SiO$_2$ because these materials are readily available in silicon microfabrication labs [21], [22]. But SiN has shown to produce high PL when guiding wavelengths of interest for bioparticle fluorescence excitation, making it non-ideal for use as a cladding layer. Tantalum oxide (Ta$_2$O$_5$) was discovered as a better option than SiN because it has a comparable refractive index to that of SiN, low absorption in the visible wavelength range, high resistance to acids, adheres well to SiO$_2$, and has a lower PL than SiN [23].

3.3.3 **Effect of Tantalum Oxide**

Figure 3-10 shows the normalized PL of PECVD SiN compared to that of sputtered Ta$_2$O$_5$. After annealing Ta$_2$O$_5$, the PL also drops substantially. The relevant PL range for cladding materials is typically between 660 nm and 690 nm for bimolecular detection on ARROWs (using a pump beam of 633 nm). PL at other wavelengths can be removed with a band pass filter [23]. More recently fabricated generations of ARROWs now incorporate Ta$_2$O$_5$ and SiO$_2$ as cladding layers instead of SiN and SiO$_2$. 


Figure 3-10: PL of PECVD SiN and SiO$_2$ films (T=250 °C) and sputtered Ta$_2$O$_5$ (T=250 °C), including as deposited films and after annealing in a vacuum chamber at 250° (excitation wavelength 633 nm) [23].
4  MAKING THE ULTIMATE ARROW

So far, this thesis has presented the basic ARROW structure in Chapter 2 and continued with specific improvements to the structure in Chapter 3. In this chapter, everything is put together by incorporating each of the improvements from Chapter 3 into a modified fabrication process. This will lead to the ultimate ARROW.

4.1  Fabrication: Putting It All Together

An earlier description of the fabrication process can be found in Section 2.3. In this section, those steps are reviewed in greater detail and a few additional in-between steps are included. These new steps reflect the changes and improvements made to the design of these chips. Instead of top ARROW layers a thick single over-coat SiO$_2$ layer is used. Instead of an ARROW structure that lays on a flat substrate a SAP is used. Instead of using SiN with SiO$_2$ as bottom layers Ta$_2$O$_5$ is used with SiO$_2$. The steps that will be explained in the following paragraphs are shown in Figure 4-1.
First, alternating layers of SiO$_2$/Ta$_2$O$_5$ pairs (Figure 4-1(a)) are deposited. The index and thickness of each layer is shown in Table 4-1. These layers can be deposited with PECVD or sputtering. To save time and effort, sputter coated wafers were used from a commercial vendor.
Table 4-1: Index and thickness of bottom ARROW layers.

<table>
<thead>
<tr>
<th>Layer</th>
<th>SiO$_2$</th>
<th>Ta$_2$O$_5$</th>
<th>SiO$_2$</th>
<th>Ta$_2$O$_5$</th>
<th>SiO$_2$</th>
<th>Ta$_2$O$_5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>1.47</td>
<td>2.107</td>
<td>1.47</td>
<td>2.107</td>
<td>1.47</td>
<td>2.107</td>
</tr>
<tr>
<td>t (nm)</td>
<td>265</td>
<td>102</td>
<td>265</td>
<td>102</td>
<td>265</td>
<td>102</td>
</tr>
</tbody>
</table>

Then, a pre-core layer of chrome (120 nm) is deposited over the bottom layers. The purpose of this layer is to protect the bottom layers from the acid etchant while the core ends are being exposed and etched. Without this layer the acid would etch into the ARROW layers and ruin the lower structure of the liquid core. This chrome layer was designed so that the liquid core would slightly overlap the chrome region at each of its ends. This can be seen in the drawing on the left of Figure 4-2. The drawing on the right shows a step that is done later in the process: all of the features on the chip, except for the core ends, are covered with a thick, protective layer of positive photoresist so that the core ends can be etched.

![Figure 4-2: A pre-core deposition of chrome is patterned to be later used as a stop-etch layer.](image-url)
These chrome regions are patterned with a positive photolithography step. After the deposition, AZ 3330 is spun onto the wafer at 5000 rpm for 1 minute and baked at 90 °C for 1 minute. The purpose of this first bake, or, soft bake, is to remove almost all of the solvents from the photoresist. It is then exposed to UV radiation for 8 seconds, developed in AZ 300 MIF developer for 1 minute, and baked at 110 °C for 2 minutes. This second bake is called a hard bake and is necessary to harden the photoresist and improve adhesion of the photoresist to the wafer surface. Then, the wafer is cleaned with an oxygen plasma descum for 1 minute at 100 Watts. At this point, the wafer is immersed into chrome etchant for about 3 minutes, or until the chrome is removed. The regions that remain are the ones that are covered by photoresist and the regions that are removed are the ones that were exposed to the UV light. Once the pattern has been defined, the photoresist is stripped with acetone and the wafer is rinsed with isopropanol (IPA).

After the pre-core layer is in place, the sacrificial core (Figure 4-1(b)) is patterned using a recipe that has been tested and developed over the course of several years. A puddle of SU-8 10 (about the size of a dollar coin) is spun at ~4300 rpm and then a soft bake is performed. This requires a bake time of 8 minutes at 65 °C, then a ramp in temperature to 95 °C for another 8 minutes and then a cool down with the temperature set to drop back down to 65 °C. Next the wafer is covered with a photomask and the resist is exposed to UV radiation for 20.5 seconds. Once this is done a post-exposure bake is performed which follows the same procedure as the soft bake. It starts at 65 °C for 6 minutes (instead of 8 minutes), the temperature gets ramped up to 95 °C for 6 minutes and then cooled back down to 65 °C. At this point it is ready for development in SU-8 developer. The time for the resist to develop is between 50 seconds to 1 minute + 30 seconds, depending on how fresh the resist is. The last step is to do two hard bakes.
This ensures that the sacrificial core creates a strong form that can sustain the rest of the fabrication process. The first hard bake starts at 65 °C, gets ramped up to 200 °C, stays for 10 minutes, and then gets cooled down to 65 °C. After an oxygen descum (40 Watts, 90 seconds) another hard bake is done. This time it starts at 65 °C and is ramped to 250 °C for 5 minutes. Then it is cooled back down to 65 °C.

The next step after completing the sacrificial core is to apply a coat of positive photoresist in preparation for a metal lift-off (Figure 4-1(c)). The process of doing a lift-off is simple and is diagrammed in Figure 4-3.

![Figure 4-3: Summary of lift-off process.](image)
It begins as any other lithography step would by spinning resist over a substrate. Then, while being covered with a photomask, it is exposed to UV radiation. After development, instead of etching into the substrate, a layer of metal is deposited. This material sticks to the substrate in all areas where the resist was developed away and gets removed after deposition when the resist is stripped. This is an efficient way to transfer a metal etch mask to the wafer.

For this process, AZ P4620 is used and spun at ~2000 rpm. The soft bake requires 60 seconds at 70 °C, then 60 seconds at 90 °C, and then 20 seconds at 120 °C. The regular exposure time is 65 seconds with the photomask and then a flood exposure is done for another 8 seconds without the photomask. This sufficiently exposes the core, along with the areas defined for the pedestal by the mask, in one step. Developing the resist in AZ 400K can take anywhere from 2 to 4 minutes. More important than the amount of time the wafer stays in the developing solution is the distance between the photoresist and the top of the core. If the distance is less than 2 µm it will not result in a clean lift-off. So, the develop time is mainly dependent on the lowering height of the resist. Figure 4-1(d) shows this completed step.

Next, the surface of the wafer is cleaned with an oxygen descum (40 Watts, 30 seconds) and a one-second hydrochloric dip (2 H2O:1 HCl) in preparation for the metal evaporation of nickel (Figure 4-1(e)). This 100 nm layer is evaporated over the entire wafer and lifted off with acetone. What remains is a layer of nickel that serves as an etch mask during the SAP etch—it protects the core and defines the pedestal regions where the solid ridge waveguides will be etched (Figure 4-1(f)).

The SAP is etched with three separate RIE/ICP processes (Figure 4-1(g)). The power, pressure, and gas flow of each recipe are recorded in Table 4-2.
Table 4-2: Plasma etching recipes for SAP ARROW.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>ICP (W)</th>
<th>RIE (W)</th>
<th>Pressure (mTorr)</th>
<th>SF₆</th>
<th>CHF₃</th>
<th>O₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂/Ta₂O₅</td>
<td>175</td>
<td>70</td>
<td>18</td>
<td>0</td>
<td>125</td>
<td>9</td>
</tr>
<tr>
<td>Si</td>
<td>275</td>
<td>0</td>
<td>120</td>
<td>0</td>
<td>75</td>
<td>0</td>
</tr>
<tr>
<td>Etch</td>
<td>275</td>
<td>60</td>
<td>35</td>
<td>20</td>
<td>30</td>
<td>0</td>
</tr>
<tr>
<td>Grass</td>
<td>0</td>
<td>200</td>
<td>150</td>
<td>52</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The first process etches through the bottom ARROW layers; the second process etches through the silicon substrate and requires both a passivation step and an etch step; and the third process removes “excess grass” [24]. The term excess grass refers to the formation of dense accumulations of vertical filaments of silicon [25]. This type of residue is undesirable because it leaves a roughly etched surface.

When these etches are complete, the nickel mask is stripped in nickel etchant (Figure 4-1(h)), the wafer is descummed at 50 Watts for 30 seconds, and then 6 µm of SiO₂ is deposited (Figure 4-1(i)). This layer replaces the alternating top ARROW layers.

Once again a photolithography step is used to pattern the SU-8 10 ridge mask. The process for the ridge lithography is very similar to that of the sacrificial core. The differences are in the spin speed (600 rpm), the cure times (soft bake: 10 minutes, post-exposure bake: 7 minutes, one hard bake: 180 °C for 10 minutes), the exposure time (9 seconds), and the develop time (1 minute 10 seconds). With the SU-8 pattern being used as the etch mask, the intersecting solid core waveguides are dry etched with a silicon dioxide anisotropic etch recipe (Figure 4-1(j)). The parameters are below in Table 4-3. Then the SU-8 is removed with Nanostrip (90 °C for 30 minutes).
Table 4-3: Plasma etching recipe for ridge etch.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>ICP (W)</th>
<th>RIE (W)</th>
<th>Pressure (mTorr)</th>
<th>Gas Flow (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>275</td>
<td>75</td>
<td>12</td>
<td>CF₄ = 50</td>
</tr>
</tbody>
</table>

Another lithography step is used to protect the core and ridges during the core expose. Again, AZ P4620 is used and spun at 1500 rpm for 60 seconds. Then a series of bakes is done to maximize the protection that the resist provides for the important features on the chip. First, a soft bake at 80 °C for 20 minutes, then a 30 minute rest at room temperature. Next, it is exposed to UV radiation for 30 seconds and developed until all the resist from the exposed areas is gone. The last bake, a hard bake, is done for 2 hours at 150 °C. This bake ensures that all the solvents are removed and solidifies the resist so that it can withstand the wet etch. Figure 4-1(k) shows the core ends being exposed. With the protective layer of AZ P4620 over the features, the wafer is then immersed into buffered hydrofluoric (BHF) acid. The etch time is dependent upon the etch rate of SiO₂ and the height of the top oxide layer and was found to be 15.4 nm/s. So, for a top oxide layer of 6000 nm, it would need to etch for 389.6 seconds or about 6.5 minutes.

Once the core ends are exposed, the final step is to etch out the cores (Figure 4-1(l)). This can be done with a Piranha mixture, which is three parts hydrogen peroxide to two parts sulfuric acid (3 H₂O₂: 2 H₂SO₄), set at 130 °C. For best results the wafer must be fully immersed in the acid and changed once every 24 hours. When done this way, cores can be completely etched out in about 5-7 days. (For faster etching the acid can be changed once every 12 hours.) This completes the fabrication process for the ARROW chips.
4.1.1 Cadence Designs

One advantage of microfabrication processing is that many devices can be created at the same time. The design that was used in this research can fit a total of 76 individual chips onto one 4-inch wafer. Figure 4-4 shows the mask layout that was designed for the ARROW platform in Cadence. Pictured in that design are a total of five masks, representing the five different photomasks that are used for the photolithography steps throughout the process. The first layer, which corresponds to the first mask, is the pre-core, the second is the core, the third is the pedestal, the fourth is the ridge, and the fifth is the core-expose.

A closer view of a single chip can be seen in Figure 4-5, along with a magnified view of the intersection between the solid and liquid core waveguides. The square pads at each of the

Figure 4-4: Mask layout of the ARROW platform made in Cadence.

A closer view of a single chip can be seen in Figure 4-5, along with a magnified view of the intersection between the solid and liquid core waveguides. The square pads at each of the
corners represent the stop-etch regions of chrome that protect the bottom layers from acid while the core ends get exposed. The arms of the liquid core extend to the chrome region at a $45^\circ$ angle. The SAP and perpendicular solid core ridges can be seen with the liquid core in the magnified view of the intersection.

![Figure 4-5: A single ARROW chip with a magnified view of the intersecting waveguides.](image)

4.1.2 Completed ARROW Chips

Figure 4-6 is an example of one of these wafers after the fabrication process is complete. The discoloration across the wafer is normal and is due to non-uniform layers of oxide. The intersection of the solid and liquid cores on an actual chip can be seen in Figure 4-7.
The following three images are SEMs of a completed ARROW chip. The first, Figure 4-8, is the cross section of the hollow core. The measurements are included in the figure. The target dimensions for the hollow core waveguide were 5 µm x 12 µm but the actual dimensions were 4.88 µm x 10.15 µm. The target height of the top oxide layer was 6 µm but the actual height was 5.08 µm.
The next SEM, Figure 4-9, was taken at the cross section of the excitation solid core ridge waveguide. It is through this perpendicular waveguide that the excitation beam is coupled into the hollow core. The target height for this waveguide was half the height of the top oxide layer. The actual height was 2.68 µm. The target width for this waveguide was 4 µm and the actual width was 3.44 µm at the top of the structure and 5.23 µm at the bottom.
This last SEM, Figure 4-10, was taken at the cross section of the collection solid core waveguide. The fluorescence signal that is produced when the excitation beam hits a tagged particle gets coupled into this lateral waveguide and collected at the end of the chip. The target width was 12 µm and the actual width was 11.85 µm at the top and 13.32 µm on the bottom. Like the perpendicular ridges, the target height for the lateral ridges was half the height of the top oxide layer. The actual height was 2.86 µm.

![Figure 4-10: SEM of collection solid core cross section.](image)

4.2 Top Oxide Measurements

When depositing a layer of PECVD oxide, there is no way of in situ monitoring its deposition rate or total film thickness. To get an idea of how fast it is growing, a timed pre-run is grown and then the amount of material that grew is measured. Next, the growth rate is calculated for that deposition \((rate = thickness/time)\) and, according to the thickness that is wanted for
the actual run, a new run time is calculated. This method gives a good idea of how long to grow an actual run but it is not exactly accurate.

4.2.1 Fluctuations in Oxide Growth Rate

Sometimes the growth rate fluctuates during a deposition. Since there is no way of predicting the exact rate during the run, the final thickness is often not what is expected. For example, the target height for the top oxide layer in Figure 4-8 was 6 µm but the actual height was only 5.08 µm. To investigate what was happening inside the growth chamber, an experiment was performed.

First, a film of oxide was grown on a test wafer for 3 minutes + 30 seconds and, using an ellipsometer, the height was measured to be 105 nm. With a calculated growth rate of 30 nm/min for that test, a new run time was calculated for a target height of 6 µm: \( \frac{6000 \text{ nm}}{30 \text{ nm/min}} = 200 \text{ min} \). So, another deposition was done for 200 minutes and was stopped every 30 minutes to measure the height of the oxide.

4.2.1.1 Filmetrics F20 Film Measurement System

Rather than using an ellipsometer for these subsequent height measurements, the Filmetrics F20 Film Measurement System, pictured in Figure 4-11, was used. The reason behind this choice was that, unlike the ellipsometer, which can only measure up to a few microns of oxide accurately, the F20 can measure up to 50 µm of oxide. This feature makes the F20 a better choice of instrument for these measurements since the final film growths that need to be measured for this project range from 5-6 µm.
The F20 system measures the thickness and index of refraction of a thin film in less than a few seconds. These characteristics are measured by reflecting or transmitting light through the sample and then analyzing the light over a range of wavelengths. Due to its wave-like properties, the light that is reflected from the top and bottom interfaces of the sample is either in-phase or out-of-phase. When the reflections are in-phase they add and when they are out-of-phase they subtract. This behavior is dependent on the wavelength of the light, $\lambda$, the thickness of the film, $d$, and its refractive index, $n$. For example, when the reflections are in phase, Equation (4.1) is true for some integer $i$.

$$\lambda = \frac{2nd}{i}. \quad (4.1)$$
The result of the interactions between the light reflections, as seen in Figure 4-12, is intensity oscillations in the reflectance spectrum. The amplitude of the oscillations is determined by the refractive index and extinction coefficient of the film. So, after an analysis of the period and amplitude of these oscillations, the thickness and index can be determined. For a given wavelength range, more oscillations indicate a thicker film.

Figure 4-12: Example of reflectance spectrum with oscillations.

4.2.1.2 Results of Oxide Growth Rate Experiment

Returning to the oxide growth rate experiment that was described earlier in Section 4.2.1, the next three figures present the results. Figure 4-13 shows the total height of the oxide at each 30 minute increment. After 200 minutes the expected height was 6000 nm but the actual height
was only 5746 nm. This represents an average growth rate of 28.73 nm/min which is slightly under the pre-calculated growth rate of 30 nm/min.

![Graph](image.png)

**Figure 4-13: Thickness of oxide layer after 200 minutes.**

In the next graph, Figure 4-14, the exact thickness of the oxide that was grown during each of the 30 minute increments is shown. The average growth per 30 minutes for the first 180 minutes was 855 nm. The drop in the graph during the last period of time was because it only represents 20 minutes as opposed to the full 30 minutes. The deposition was stopped at exactly 200 minutes to compare actual thicknesses to calculated thicknesses.
In the last graph, Figure 4-15, the fluctuations in growth rate can be seen throughout the duration of the deposition. Although the test wafer exhibited a growth rate of 30 nm/min just before carrying out this experiment, the actual growth rate after the first 30 minutes was only 25.3 nm/min. These slight changes in growth rate affected the final thickness of the top oxide layer but could not have been predicted based on the estimated run time.
This result was surprising for a couple of reasons. First, prior to carrying out this experiment, it was predicted that the growth rate would worsen over time and eventually slow down. This seemed like a reasonable assumption because the final height of the top oxide layer was consistently lower than the target height. Instead, the results remained fairly linear. Second, the calculated growth rate during the test run dropped from 30 nm/min to 25.3 nm/min within the first 30 minutes of the actual run. Throughout the entire run, this turned out to be the biggest dip in growth rate. For the growth rate to experience that much of a drop with only a few minutes between the test run and the actual run was unexpected because the test run only lasted 3 minutes + 30 seconds.
This experiment confirmed that the growth rate of a thick layer of oxide fluctuates over time. The inability to measure oxide thickness during the fabrication process presents some issues. First, the thickness of the top oxide layer determines how deep of an etch needs to be made when making the intersecting ridge edges (Section 2.3.4). Without knowing the actual height, the ridges could be unintentionally etched too far or not enough, thereby causing coupling problems. Second, if the top layer is too short the crevice that is created causes problems at the interface (Section 3.1.1). By knowing the actual thickness of the top layer before moving on to the next step in the process, a growth could continue until the desired height was reached. Third, an inaccurate thickness leads to a waste of time, materials, and labor spent on the entire process. These resources would not be wasted if the thickness of the layer could be measured before continuing the process and growing the accurate thickness.

4.2.2 Mid-Process Top Oxide Measurement Experiment

For convenience, a simple way was developed to measure the top oxide mid-process without needing to take an SEM. Using the Filmetrics 20 that was described in Section 4.2.1.1, a new experiments was performed. This experiment was designed to figure out how to incorporate the Filmetrics 20 into the fabrication process and to ensure that it would measure the top oxide layer properly in spite of the many layers below.

The experiment wafer was set up to simulate each of the areas on an ARROW wafer that could possibly be used for measuring the top layer of oxide. Each area underwent a different version of fabrication processing that paralleled the actual processing of the wafer. Then, a thick
layer of oxide was grown on the experiment wafer in increments and the thickness was measured. A diagram explaining each of the four sections is shown in Figure 4-16.

![Figure 4-16: Experiment wafer used for top oxide measurements.](image)

The first section, 1a, was a section of plain silicon that was used as the control section. The measurements that were taken from the other three sections were compared to the measurements from 1a. The next three sections represent the progression of the fabrication process at incremental steps. 1b had a layer of chrome over the silicon substrate and was not treated in any other way. This section was used mainly for comparison purposes. 2c also had a layer of chrome over the silicon substrate but was taken through the SAP etch. This section best represents what the actual wafer would see during processing. The chrome layer comes from the pre-core stop-etch layer and it does not have a protective layer during the SAP etch. This would
be the ideal location to measure the top oxide on the actual wafer because it has a big enough surface area and since it would not require any additional fabrication steps or mask designs. 2d was the most complex of the four sections; first it had a layer of chrome deposited over the silicon, then it was covered in nickel to protect it during a SAP etch and finally the nickel was removed after the etch recipes were completed. This section was simulated in case the results showed that exposing the chrome to the SAP etch in 2c negatively affected its ability to produce accurate measurements. If that were the case, section 2d would simulate having a protective layer of nickel over the chrome area during the SAP etch and later removing it for the measurements. This would require a new mask that would incorporate a protective nickel covering over the regions of chrome.

Once the experiment wafer was prepared with the four different sections it was ready for the oxide deposition. A 2 µm growth was calculated to take 60 minutes + 14 seconds. The total time was divided by four to get growth increments of 0.5 µm, which resulted in each of the four runs being 15 minutes + 3 seconds long. After each increment of time the oxide thickness was measured at all four sections and the results were recorded.

Prior to making measurements with the Filmetrics 20 a few changes needed to be made to the software. The next four images are screen shots of the Filmetrics software, FILMeasure, that was used to read the thickness measurements. The first window in Figure 4-17 is an example of the reflectance spectrum that was produced from a test wafer. On the right hand side of the window, about half way down the image, the “Structure” is listed as SiO₂ on Si. This describes the material being measured (SiO₂) and the substrate below it (Si) and was already listed as one of the options in the drop-down box. Although there are many other options to choose from, the structure of interest for this experiment, SiO₂ on Cr, was not an option.
One of the main purposes for doing this experiment was to figure out how to use the Filmetrics 20 to measure the top oxide layer mid-process. Learning how to adjust the structures of this software program was essential to accomplishing this goal. In order to create a new structure another window must be opened by clicking “Edit Structure,” located just below the “Structure” drop-down box. Figure 4-18 shows the new window that pops up.

Once inside the “Edit Structure” window, the layers must first be selected. In this case, the substrate was chosen as chrome, the layer was chosen as SiO₂ and the medium was air. The unit was selected to be microns and the approximate thickness was set for a default of 6 µm. Then, by clicking the “Save As” button on the bottom left corner of the window, the new structure was saved.
Using this newly input structure, the top oxide layer was measured after each 15 minute + 3 second time interval. Since the target height was 2 µm, the expected growth for every time interval was about 0.5 µm.

4.2.2.1 Results of Mid-Process Top Oxide Measurement Experiment

Table 4-4 below summarizes the results of this experiment. All measurements are in nanometers and the number beside each measurement is the corresponding goodness of fit percentage. The control section, 1a, grew (on average) 516 nm of oxide per 15 minute interval. These were all very accurate measurements because the goodness of fit was greater than or equal to 99.4 for each measurement. Section 1b produced similar measurements and was useful for just
that comparison. The section of greatest interest, 2c, still had high values for goodness of fit and was very comparable to the values recorded for 1a. This suggests that the chrome area is a valid place to measure the thickness of the top oxide layer. An interesting thing to note is that the measurements in 2d are very close to the measurements in 1a but the goodness of fit is much lower than the rest of the columns.

Table 4-4: Thickness of oxide layer when grown over separate areas of different fabrication processing.

<table>
<thead>
<tr>
<th>Run</th>
<th>Time</th>
<th>1a</th>
<th>1b</th>
<th>2c</th>
<th>2d</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>15 min 3 sec</td>
<td>520 nm / 99.6</td>
<td>517 nm / 99.2</td>
<td>520 nm / 98.0</td>
<td>530 nm / 47.1</td>
</tr>
<tr>
<td>2</td>
<td>15 min 3 sec</td>
<td>1054 nm / 99.7</td>
<td>1045 nm / 99.1</td>
<td>1042 nm / 97.7</td>
<td>1052 nm / 61.1</td>
</tr>
<tr>
<td>3</td>
<td>15 min 3 sec</td>
<td>1544 nm / 99.4</td>
<td>1533 nm / 98.7</td>
<td>1557 nm / 98.2</td>
<td>1533 nm / 69.0</td>
</tr>
<tr>
<td>4</td>
<td>15 min 3 sec</td>
<td>2065 nm / 99.6</td>
<td>2038 nm / 94.7</td>
<td>2085 nm / 97.5</td>
<td>2066 nm / 67.9</td>
</tr>
</tbody>
</table>

The results of this experiment show that the top oxide layer can be measured directly over the pre-core chrome stop-etch pads. This is a great benefit to the overall fabrication process of the ARROW platform because it provides a way to measure the thickness of the top oxide layer in the middle of the fabrication process. This can be done without needing to create any new masks or add any new fabrication steps. It also does not require an SEM at the end of the entire fabrication process. Because of this technique, the top oxide layer can be grown accurately and the expected height can be achieved. This eliminates potential coupling problems with the ridge and crevice problems at the interface.

In the future, this method of measuring a thick oxide layer should be used when depositing the top oxide. After depositing oxide onto the wafer for the calculated run-time, the
wafer can be removed and measured with the Filmetrics 20. If the height is lower than the expected height, the wafer can be returned to the chamber and the deposition can continue. On the other hand, if the target height has been reached, this step would be considered complete and the fabrication process would move forward.
5  TESTS MADE WITH ULTIMATE ARROW

Once the ultimate ARROW has been successfully fabricated, it can be used to perform various tests. The purpose of these tests is to see whether or not it can perform single particle analysis. This chapter focuses on one particular test that was done by first introducing fluorescently labeled virus samples into the hollow core waveguide and then comparing those results to a control experiment.

5.1  Method

Figure 5-1 shows a schematic of an optofluidic chip with a sample virus being introduced into the hollow-core waveguide.
Fluorescent molecules attached to the viruses are excited at the intersection of the hollow and solid cores. This excitation volume is on the order of ~100 fL and is small enough to reach single molecule detection sensitivity. Figure 5-2 is a photograph of the chip and the experimental test setup.

![Figure 5-2: Photograph of chip.](image)

For this experiment, both H1N1 and H3N2 virus samples at clinically relevant concentrations (10⁴/mL) were used [26]. RNA was extracted from both samples and mixed with a fluorescent molecule tag designed to bind specifically to the H3N2 RNA. Fluorescence signal is produced only if a tag successfully binds to a target RNA sample. When a sample is mixed with a tag that does not match there is no fluorescence. Figure 5-3 shows a diagram of this type of labeling approach.
5.2 Results

Figure 5-4 is an intensity graph of the fluorescence signal produced by H3N2 samples flowing through the excitation volume versus time. The graph shows 565 spikes in 200 seconds, which corresponds to the individual detection of 565 H3N2 RNA. This means that the ARROW platform was able to successfully detect single RNA within the liquid core.
The differences in intensity peaks can be attributed to the different positions of the nucleic acids within the excitation volume. If the nucleic acid is not exactly centered within the excitation volume, the signal is much weaker. The peaks also change due to variations in labeling efficiency.

By comparison, Figure 5-5 was generated by combining H3N2 probes with H1N1 targets. Since the H3N2 probe was only designed to bind to the H3N2 virus, the purpose of this experiment was to see if any of the H1N1 particles would fluoresce without having the proper probe attached to it. This graph shows very few intensity peaks of much smaller values, suggesting that the probes and targets did not bind and no strong fluorescence signals were created.

Figure 5-5: Negative control using H1N1 target and H3N2 probes.
This result shows that amplification-free detection of clinical relevant virus samples, and other bioparticles, can be made with this optofluidic platform. The type of probe that was used in conjunction with the virus sample was essential to this sensor functioning properly. From these two experiments, it was shown that having the proper probe allowed for individual RNA to be detected and not having the proper probe lead to basically no detection at all. With its ability to selectively detect virus samples and other bioparticles, the ultimate ARROW optofluidic platform is well on its way toward a self-diagnostic at-home test.

5.3 Hybrid Optofluidic Integration

Up to this point, the silicon-based optical detection layer that has been presented still involves laboratory-scale functions. For instance, sample preparation requires common laboratory equipment (vortexers, shakers, and separation columns) that are large in comparison to the chip itself. The next step towards a self-functioning lab on chip device is to integrate a microfluidic processing unit with the optofluidic sensing platform explained in this thesis. The purpose of this processing layer is to facilitate particle mixing. Figure 5-6 illustrates this concept.

![Figure 5-6: Schematic depiction of hybrid optofluidic integration of microfluidic sample preparation (top) and optical analysis (bottom) layers.](image)

58
The following image in Figure 5-7 shows how this layer was integrated. First, a PDMS (polydimethylsiloxane) layer was formed. Master molds were lithographically defined for channels (30 µm high and 75 to 200 µm wide) using SU-8. Then, PDMS elastomer and curing agent were mixed in a 10:1 ratio and degassed for one hour, after which the mixture was poured onto the silanized SU-8 master and baked for one hour at 60 °C. Next, manifold, or access, layers were bonded to the PDMS layer with a 30 W oxygen plasma for 30 seconds. Finally, metal reservoirs were inserted into holes that were punched into the PDMS layer and epoxy was applied to the lower edges and placed on top of the ARROW chip. Tygon tubing was used to connect the device to a Luer lock syringe which introduced the fluid into the channels.

Figure 5-7: Expanded view of PDMS integration with an ARROW optofluidic chip.
5.3.1 Mixing

Successful mixing of a raw sample and fluorescent label was shown with this hybrid optofluidic device using the setup in Figure 5-8 [27]. A $\lambda$-DNA sample was mixed with SYBR Gold fluorescent dye in the PDMS microfluidic layer and introduced into the ARROW chip. Single molecules of labeled $\lambda$-DNA were excited with a 488 nm Ar-ion laser and detected with an APD.

![Figure 5-8: Schematic of optical setup for PDMS controlled particle detection.](image)

The result of this experiment is shown in Figure 5-9. The dashed horizontal line shows the threshold level above the background and is defined here as three times the standard deviation of a SYBR Gold control signal. Fluorescence peaks representing single $\lambda$-DNA molecules are present throughout the time trace and are well above the noise threshold. A zoomed-in section (inset of Figure 5-9) unambiguously displays the individual fluorescence signals. Differences in signal strengths between individual nucleic acids are caused by an
inhomogeneous labeling efficiency, the spatially dependent velocity and collection efficiency of the liquid core waveguide. However, since this is a direct detection experiment of single nucleic acids above a background threshold, the variation in signal strengths does not affect the assay.

Figure 5-9: Time dependent fluorescence trace of on-chip mixed, labeled, and detected single λ-DNA molecules.
6 Y-SPLITTER ARROW

Even with all the improvements that have gone into making the ultimate ARROW, there are still modifications that can be made to the design. For example, an additional feature involving some form of multi-spot excitation could be used to correlate the optical signals of a particle in space and time. Such a feature would address the problem of trying to recover weak signals that are masked by noise. This chapter discusses the theory, fabrication, design, and experimental results of these structures. Throughout this chapter they will be referred to as Y-splitters.

6.1 Theory

A Y-splitter originates from one waveguide and splits into two waveguides in the shape of a Y. From there, the splitting can continue propagating forward at each of the newly created waveguides in a tournament bracket like manner. Figure 6-1 shows how a Y-splitter (1 x 2, 1 x 4, or 1 x 8) can be used to excite multiple locations along a liquid core ARROW.
Figure 6-1: Y-Splitters can be used for multi-spot excitation at liquid core.

There are two ways by which light can be collected. The first way is to have a similar structure on the opposite side of the liquid core. This is illustrated in Figure 6-2.

Figure 6-2: Light can be collected by duplicating the Y-structure on the opposite side of the core.
The second way to collect light is through individual waveguides. This configuration is shown in Figure 6-3.

![Figure 6-3: Light can be collected by individual waveguides.](image)

For example, the 1 x 4 Y-splitter shown in Figure 6-4 has four equally spaced solid core waveguides that intersect the liquid core [28].

![Figure 6-4: Schematic of integrated optofluidic chip using Y-splitter structure.](image)
When measuring particles traveling down the liquid core, each particle passes 4 optical excitation spots, and creates signals that are correlated in time and space. These signals are collected and detected by an APD and result in 4 sequential temporally encoded fluorescence peaks. Even if these signals are weak and masked by noise, the signal can be recovered by applying the following algorithm:

\[
S(t) = f_1(t) * f_2(t - \Delta T) * f_3(t - 2\Delta T) * f_4(t - 3\Delta T),
\]

(6.1)

where \(\Delta T\) is the time difference between each signal. Every other signal variation (i.e. noise) that is not time-correlated is filtered out efficiently. This method can be further enhanced by simply increasing the number of excitation spots [28].

### 6.2 Fabrication

The fabrication of these devices follows the same process that was described for the ultimate ARROW in Chapter 4. The biggest difference, and most interesting change, is when making the intersecting ridge waveguides. Rather than having straight ridges, these ridges incorporate the Y-splitter. A few solid prototypes were designed and then fabricated, as described in the following sub-sections.

#### 6.2.1 Design

The length of the Y-splitter mid-section, \(W\), depends on the angle of the split, \(\theta\), and the distance between the two ends, \(d\). This is described by Equation (6.2) and illustrated in Figure 6-5.
The exact numbers for three different designs are given in Table 6-1. The parameters are included in the diagrams of Figure 6-6.

![Design parameters for Y-splitter.](image)

\[
\tan \theta = \frac{d}{2W}. 
\]  

(6.2)

<table>
<thead>
<tr>
<th>Design</th>
<th>d</th>
<th>y</th>
<th>w₁</th>
<th>w₂</th>
<th>w₃</th>
<th>θ₁</th>
<th>θ₂</th>
<th>θ₃</th>
<th>Z</th>
</tr>
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<tbody>
<tr>
<td>1 x 2</td>
<td>25 µm</td>
<td>25 µm</td>
<td>1000 µm</td>
<td>-</td>
<td>-</td>
<td>0.7162°</td>
<td>-</td>
<td>-</td>
<td>2975 µm</td>
</tr>
<tr>
<td>1 x 4</td>
<td>25 µm</td>
<td>25 µm</td>
<td>1000 µm</td>
<td>1000 µm</td>
<td>-</td>
<td>0.7162°</td>
<td>1.4321°</td>
<td>-</td>
<td>1950 µm</td>
</tr>
<tr>
<td>1 x 8</td>
<td>25 µm</td>
<td>25 µm</td>
<td>1000 µm</td>
<td>1000 µm</td>
<td>1500 µm</td>
<td>0.7162°</td>
<td>1.4321°</td>
<td>1.9092°</td>
<td>440 µm</td>
</tr>
</tbody>
</table>
6.2.2 Solid Prototypes

Figure 6-7 shows some of the first Y-splitters that were successfully made. The picture on the left shows a 1 x 2 Y-splitter and the one on the right shows a 1 x 4 Y-splitter. These prototypes were fabricated directly on a silicon substrate.
Using these solid Y-splitter prototypes of varying angles, tests were performed to determine the ideal angle of the split. A quick analysis of the graph in Figure 6-8 shows that the throughput of the waveguide is highest for angles less than $5^\circ$. 

![Figure 6-7: Examples of 1 x 2 and 1 x 4 Y-splitters.](image)

![Figure 6-8: Throughput of solid Y-splitter waveguides as a function of angle.](image)
6.2.3 First ARROW Y-Splitters

An example of the first splitters that were fabricated on an ARROW chip is shown below in Figure 6-9; it is an SEM of a 1 x 2 Y-Splitter at the junction. Here, it is clear that the split does not join at a clean point but rather, a dull curve. This is an issue that arises during the fabrication of the ridge and can be attributed to variations in feature heights across the wafer.

![Figure 6-9: SEM of Y-splitter.](image)

In order to explain why this issue occurs, an understanding of the feature heights is necessary. These solid core ridge waveguides are built on top of the SAP, which typically measures about 12 µm high. On top of that, in some areas, the hollow core waveguide is about 5 µm high. So, the tallest feature, from the bottom of the SAP to the top of the core, is about 17 µm.
During the ridge etch the core must be protected by SU-8 so an additional 3-4 µm of SU-8 should cover the core. This brings the total height of the SU-8 at the core to about 21 µm. The ideal thickness of SU-8 over the SAP is also 3-4 µm which puts the height above the SAP at about 16 µm. Since photoresist is spun across the entire wafer it tends to planarize as much as possible and fill in all gaps.

Herein lies the problem: if the tallest feature needs to remain protected by the SU-8, the middle-sized feature needs to pattern the ridges by having some parts stay and some parts develop away, and the gaps between the SAPs need to be completely developed away, it is difficult to identify a single lithography recipe that is capable of satisfying all three conditions. For example, exposing the resist too long means the inner gaps do not get cleared out and exposing too short means everything gets washed away. Likewise, developing for too long means unwanted areas get washed away and under developing means not enough resist gets washed away. Furthermore, it is difficult to get the SU-8 thick enough to protect the core waveguides.

Due to the wide variations in feature heights across the wafer, this step presents a unique challenge. In order to overcome it, a recipe must be developed that can achieve all three goals: protect the core, pattern the ridges, and develop all the field SU-8. Once this is accomplished, the Y-junction will be more crisp and well-defined.

6.3 Method

When CdSe quantum dots were introduced into the hollow core waveguide these intersecting solid core waveguides were used to excite the quantum dots. An overhead CCD
camera captured the fluorescence signal that was created and can be seen as four excitation spots in Figure 6-10.

![Four excitation spots in liquid core waveguide.](image1)

**Figure 6-10:** Four excitation spots in liquid core waveguide.

As each particle passed an excitation spot a signal was created and could be collected and measured off the chip. Figure 6-11 is a graph of the four peaks that were created. With some simple signal processing, this time correlated output can lead to much higher signal-to-noise ratios than a single excitation beam.

![Fluorescence signal generated from single 1μm particle.](image2)

**Figure 6-11:** Fluorescence signal generated from single 1μm particle.
6.4 Results

We introduced 1 μm diameter fluorescent particles into the channel and excited them with a HeNe (λ=633 nm) laser [28]. The raw data from the detector is shown in Figure 6-12.

![Figure 6-12: Raw data obtained from detector.](image)

The average signal level detected was ~105 counts/ms, and the average noise level was about 0.81 counts/ms. This resulted in a signal to noise ratio (SNR) of 130. The data was then processed using the algorithm in Equation (6.1) and ΔT=1 ms was chosen which resulted in the data shown in Figure 6-13.
The post-processed data represents an average signal level of about 3,189 counts/ms and an average noise level of 0.14 counts/ms. This means that the improved SNR is 22,778. With these Y-splitter ARROW chips, the overall SNR was improved by 175 times. This improvement in SNR is a major accomplishment. With such a large increase in SNR, the processed data is cleaner, meaning less noisy, and more reliable. By using the Y-splitter ARROW platform, single particles can be detected with greater accuracy.
7 CONCLUSION

7.1 Summary

Throughout the past ten years, specific improvements have been made to this ARROW-based platform. The research in this thesis covers the advancements that have been made in the past two years and focuses on combining the individual improvements that were previously made into one structure. The first improvement dealt with the coupling losses associated with a crevice that was formed by an under-grown top oxide layer. The solution was to grow a thicker top layer of oxide and eliminate the alternating top ARROW layers. The second improvement addressed the issues related to the inefficient geometry that was previously used, which was surrounded by oxide on two sides, and caused greater losses the waveguides. To decrease loss in the waveguide the previous design was substituted for the self-aligned pedestal, which was surrounded by air on three sides and facilitated better wave guiding. The last improvement involved switching out the SiN ARROW layer for Ta2O5 which produced less photoluminescence. Because of the improvements that were made to the platform, a point has been reached where single bioparticles can be measured in clinically relevant concentration.

A detailed description of the fabrication process is also included in this work and a new, convenient way of measuring the top oxide layer mid-process is introduced. This method uses a
Filmetrics 20 Film Measurement System and provides a way to accurately deposit the top oxide layer to a desired thickness without waiting until the end of the process to measure it.

Another major focus of this research project was dedicated to designing a newer generation of devices that contains multi-spot excitation at the liquid core. Such devices have been successfully fabricated and have shown to dramatically improve the SNR of the ARROW-based optofluidic platform.

7.2 Future Work

Although some promising results have already been seen, specific improvements and modifications have yet to be made to the current design. These modifications would move this project even closer to producing a self-diagnostic biosensor.

7.2.1 Y-Splitter Ridge Fabrication

One improvement that could be made to help this research progress would be to get better definition at the point of the Y-intersection. This would imply a change in the fabrication of the intersecting solid core ridges. That change could mean using a different resist, exposing the resist for a different amount of time, using different cure times, or editing the etch recipes.

An SEM of one device is shown in Figure 7-1. The black lines that are drawn over the figure show where the device should actually be, according to the design. The deviation in structure causes scattering at the intersection and decreases the coupling efficiency. Therefore, improving this intersection has the potential to improve the coupling efficiency and decrease the amount of scattering.
Multimode Interference

Another area of research that could be explored is called a multimode interference or MMI. The basic idea behind an MMI is that a single excitation beam at the input can split into multiple beams at the output. The number of beams at the output is dependent upon the wavelength of the input light, the width of the MMI structure and its length. A schematic of a sample structure is illustrated in Figure 7-2 [29].
This could replace the Y-splitter intersecting ridge and still provide the ability to perform signal processing. Furthermore, the design can be made such that 6, 7, 8 or 9 output beams could be made.

7.2.3 Particle Focusing

One final suggestion deals with focusing the particles inside the liquid core to the center of the volume. This issue was brought up in Section 5.2; to summarize, if the particles are not flowing through the center of the liquid core, the fluorescence signal that gets detected off the chip is weak and crowded with noise. Also, the particles will not even fluoresce if they do not flow past the beam of the excitation laser. The strongest signal is produced for particles that are exactly in the center of the waveguide. A feature that would help to focus the particles to the center of the waveguide would significantly improve the performance, transmission, and optical signal of these devices.
As improvements and adjustments to the ARROW-based optofluidic platform continue to be made, it has the potential to one day produce an instant diagnosis of an illness or even identify early stages of cancer—this would be life-changing!
REFERENCES


APPENDIX A. LIST OF PUBLICATIONS

A.1 Refereed Journal Publications


A.2 Conference Papers and Presentations


APPENDIX B. PROCESS RECIPES

B.1 SU-8 Recipes

SU-8 10 Sacrificial Core

1. Apply SU-8 10 using Laurell Spin Processor
   a. Pour small puddle of photoresist onto wafer (size of dollar coin)
   b. Spin photoresist using 3-step program
      i. 500 rpm, 6 sec
      ii. 4300 rpm, 60 sec
      iii. 6000 rpm, 2 sec
2. Soft bake on hotplate
   a. Set at 65 °C, 8 min
   b. Ramp to 95 °C, 8 min
   c. Cool to 65 °C
3. Expose 20.5 sec (north aligner, hard contact), 7.3 mW/cm²
4. Post exposure bake on hotplate
   a. Set at 65 °C, 6 min
   b. Ramp to 95 °C, 6 min
   c. Cool to 65 °C
5. Develop photoresist in SU-8 developer for ~1 min and rinse with IPA
6. Hard bake 1 on hotplate
   a. Set at 65 °C
   b. Ramp to 200 °C, 10 min
   c. Cool to 65 °C
7. Descum in Planar Etch II (PE2) – 40 W, 90 sec, 100 sccm O₂
8. Hard bake 2 on hotplate
   a. Set at 65 °C
   b. Ramp to 250 °C, 5 min
   c. Cool to 65 °C
9. Measure height of sacrificial core using the Profilometer (target height: 5 µm)
SU-8 10 Ridge

1. Dehydration bake in clean oven – 150 °C, 30 min
2. Apply SU-8 10 using Laurell Spin Processor
   a. Pour large puddle of photoresist onto wafer (little more than size of dollar coin)
   b. Spin photoresist using 3-step program
      i. 500 rpm, 6 sec
      ii. 600 rpm, 60 sec
      iii. 6000 rpm, 2 sec
3. Soft bake on hotplate
   a. Set at 65 °C, 10 min
   b. Ramp to 95 °C, 10 min
   c. Cool to 65 °C
4. Expose 9 sec (south aligner, hard contact), 7.3 mW/cm²
5. Post exposure bake on hotplate
   a. Set at 65 °C, 7 min
   b. Ramp to 95 °C, 7 min
   c. Cool to 65 °C
6. Develop photoresist in SU-8 developer for ~1 min + 30 sec and rinse with IPA
7. Hard bake on hotplate
   a. Set at 65 °C
   b. Ramp to 180 °C, 10 min
   c. Cool to 65 °C
10. Descum in PE2 – 40 W, 30 sec, 100 sccm O₂
8. Measure height of SU-8 over sacrificial core using the Profilometer (target height: 5 μm)

B.2 Positive Photoresist Recipes

AZ 3330 Etch Mask

1. Dehydration bake in clean oven – 150 °C, 15 min
2. Apply AZ 3330 using Laurell Spin Processor
   a. Pour big puddle of photoresist onto wafer (about 2 inches in diameter)
   b. Spin photoresist using 1-step program
      i. 5000 rpm, 60 sec
3. Soft bake on hotplate
   a. 90 °C, 60 sec
4. Expose 8 sec (south aligner, hard contact), 7.3 mW/cm²
5. Develop photoresist in AZ 300 MIF developer for 60 sec and rinse with water, dry
6. Descum in PE2 – 100 W, 60 sec, 100 sccm O₂
7. Hard bake on hotplate
   a.  110 °C, 2 min

**AZ P4620 for Nickel Lift-off**

1. Dehydration bake in clean oven – 150 °C, 15 min
2. Apply AZ P4620 using Laurell Spin Processor
   a. Pour big puddle of photoresist onto wafer (about dollar coin size)
   b. Spin photoresist using 2-step program
      i.  2000 rpm, 30 sec
      ii. 6000 rpm, 2 sec
3. Soft bake on hotplate
   a.  70 °C, 60 sec
   b.  90 °C, 60 sec
   c.  120 °C, 20 sec
4. Expose 66 sec using photomask (north aligner, constant intensity), 7.3 mW/cm²
5. Flood expose 8 sec without photomask (north aligner, constant intensity), 7.3 mW/cm²
6. Develop photoresist in diluted AZ 400K developer 1:4 (25 mL, 100 mL) for 2-4 min and rinse with water, dry
7. Descum in PE2 – 40 W, 30 sec, 100 sccm O₂
8. Measure height across sacrificial core (target height: 2 µm)

**AZ P4620 Etch Mask**

1. Apply AZ P4620 using Laurell Spin Processor
   a. Pour big puddle of photoresist onto wafer (little bigger than dollar coin size)
   b. Spin photoresist using 1-step program
      i.  1500 rpm, 60 sec
2. Soft bake on hotplate
   a.  80 °C, 20 sec
3. Rest at room temperature for 30 min
4. Expose 30 sec (south aligner, constant intensity), 7.3 mW/cm²
5. Develop photoresist in diluted AZ 400K developer 1:4 (25 mL, 100 mL) for ~2 min + 30 sec and rinse with water, dry
6. Hard bake on hotplate
   a.  150 °C, 2 hr
B.3 Deposition Recipes

Pre-core Chrome Stop-etch Layer

1. Deposit 120 nm chrome in E-beam at 3 Å/s
2. Pattern chrome using “AZ 3330 Etch Mask” recipe described in Appendix B.2 Positive Photoresist Recipes
3. Etch chrome using Chrome Etchant, 3 min
4. Strip AZ 3330 with acetone and IPA using Solitec Spinner
5. Descum in PE2 – 150 W, 3 min, 100 sccm O₂

Nickel Lift-Off

1. Pattern AZ P4620 photoresist using “AZ P4620 for Nickel Lift-off” recipe from Appendix B.2 Positive Photoresist Recipes
2. Dip wafer in diluted hydrochloric acid (HCl) 1:2 for a few seconds
3. Deposit 75 nm nickel in E-beam at 1 Å/s
4. Remove photoresist and lift off nickel
   a. Soak in acetone, 7-10 min
   b. Rinse with IPA
5. Descum in PE2 – 50 W, 30 sec, 100 sccm O₂

PECVD SiO₂ Top Layer

1. Deposit 6 µm SiO₂ using the recipe in Table B-1
2. Measure with Filmetrics 20 Film Measurement System to confirm height

<table>
<thead>
<tr>
<th>Recipe</th>
<th>Gas 1: SiH₄ (sccm)</th>
<th>Gas 2: N₂O (sccm)</th>
<th>Pressure (mTorr)</th>
<th>RF Power (W)</th>
</tr>
</thead>
<tbody>
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<td>SiO₂</td>
<td>145.2</td>
<td>29</td>
<td>1100</td>
<td>30</td>
</tr>
</tbody>
</table>

B.4 Wet Etch Recipes

TC-1 Cleaning

1. Preheat hotplate to 55 °C
2. Mix hydrogen peroxide and RS-6 – 1:10 H₂O₂: RS-6 (10 mL, 100 mL)
3. Place on hotplate; place wafer in TC-1, 10 min
4. Rinse with water, dry

Core Expose

1. Etch SiO₂ in Buffered Hydrofluoric (BHF) acid, 500 sec or until SiO₂ is completely gone
2. Rinse with water, dry

Sacrificial Core

1. Preheat hotplate to 130 °C
2. Place the wafer into a Teflon etch boat to prepare for sacrificial core removal
3. Mix Piranha with hydrogen peroxide and sulfuric acid – 3:2 H₂O₂:H₂SO₄ (60 mL, 40 mL)
4. Place on hotplate; place wafer etch boat into Piranha
5. Cover the dish with a glass lid. Weight the lid down to decrease evaporation loss.
6. Change solution every 12-24 hrs until cores are completely etched, 5-7 days
7. After cores are removed, rinse the wafer
   a. Place wafer in a dish of water at room temperature, 24 hrs
   b. Place wafer in a dish of Nanostrip at room temperature, 24 hrs
   c. Place wafer in a dish of water at room temperature, 24 hrs
8. Dry wafer and prepare for shipping

B.5 Dry Etch Recipes

Self-Aligned Pedestal

1. Etch SiO₂/Ta₂O₅ layers in the Trion using the recipe in Table B-2, ~8-10 min (target height: 1.3 µm)
2. Clean wafer using “TC-1 Cleaning” recipe in Appendix B.4 Wet Etch Recipes
3. Etch Si in the Trion using the recipe in Table B-2, 3 full cycles (target height: 6 µm)
4. Etch grass in the Trion using the recipe in Table B-2, 60 sec (target height: 7 µm)
5. Clean wafer using “TC-1 Cleaning” recipe in Appendix B.4 Wet Etch Recipes
6. Remove the nickel mask in Nickel Etchant
7. Clean wafer using “TC-1 Cleaning” recipe in Appendix B.4 Wet Etch Recipes
8. Descum in PE2 – 50 W, 30 sec, 100 sccm O₂
9. Dehydration bake in clean oven – 150 °C, 30 min
Table B-2: Plasma etching recipes for self-aligned pedestal in Trion.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>ICP (W)</th>
<th>RIE (W)</th>
<th>Pressure (mTorr)</th>
<th>Gas Flow (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$/Ta$_2$O$_5$</td>
<td>175</td>
<td>70</td>
<td>18</td>
<td>SF$_6$: 0</td>
</tr>
<tr>
<td>Si Passivation</td>
<td>275</td>
<td>0</td>
<td>120</td>
<td>CHF$_3$: 75</td>
</tr>
<tr>
<td>Si Etch</td>
<td>275</td>
<td>60</td>
<td>35</td>
<td>O$_2$: 0</td>
</tr>
<tr>
<td>Si Grass</td>
<td>0</td>
<td>200</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

Ridge

1. Etch SiO$_2$ in the Trion using the recipe in Table B-3, 540 sec (target height: half the thickness of the top oxide layer)
2. Remove SU-8 10 in Nanostrip, 90 °C, 30 min
3. Dehydration bake in clean oven – 150 °C, 30 min

Table B-3: Plasma etching recipe for ridge etch in Trion.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>ICP (W)</th>
<th>RIE (W)</th>
<th>Pressure (mTorr)</th>
<th>Gas Flow (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>275</td>
<td>75</td>
<td>12</td>
<td>CF$_4$ = 50</td>
</tr>
</tbody>
</table>
APPENDIX C.    FABRICATION PROCESS FLOW

C.1 Optofluidic ARROW Platform

1. Obtain a <100> wafer that has commercially grown ARROW bottom layers
2. Scribe the back of the wafer with the wafer identification number
3. Deposit 20 nm SiO₂ as an adhesion promotion layer
4. Pattern the “Pre-core Chrome Stop-etch Layer” described in Appendix B.3 Deposition Recipes
5. Define the “SU-8 10 Sacrificial Core” from Appendix B.1 SU-8 Recipes
6. Deposit nickel onto wafer using the “Nickel Lift-Off” recipe in Appendix B.3 Deposition Recipes
7. Etch the “Self-Aligned Pedestal” according to Appendix B.5 Dry Etch Recipes
8. Grow the “PECVD SiO₂ Top Layer” using the recipe in Appendix B.3 Deposition Recipes
9. Pattern “SU-8 10 Ridge” as outlined in Appendix B.1 SU-8 Recipes
10. Etch the “Ridge” listed in Appendix B.5 Dry Etch Recipes
11. Protect the features on the wafer with the “AZ P4620 Etch Mask” found in Appendix B.2 Positive Photoresist Recipes
12. Etch the core ends using the “Core Expose” recipe in Appendix B.4 Wet Etch Recipes
13. Remove the “Sacrificial Core” using the recipe from Appendix B.4 Wet Etch Recipes