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Characterization and Optimization of an Image
Charge Detector for the Measurement of
Martian Dust

Jace Rozsa

A thesis submitted to the faculty of
Brigham Young University
in partial fulfillment of the requirements for the degree of
Master of Science

Aaron R. Hawkins, Chair
Shiuh-hua Wood Chiang
Daniel E. Austin

Department of Electrical and Computer Engineering
Brigham Young University

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ABSTRACT

Characterization and Optimization of an Image Charge Detector for the Measurement of Martian Dust

Jace Rozsa
Department of Electrical and Computer Engineering, BYU
Master of Science

Image charge detector (ICD) technology has existed for decades. However, not until recently has an ICD been proposed for use in space exploration, specifically for studying the characteristics of the dust on Mars. Characterizing the dust on Mars is crucial for designing equipment to aid manned missions. It also improves our understanding of Mars’ climate and weather systems. An ICD utilizing printed circuit board (PCB) electrodes, coupled with a custom differential amplifier, is best suited for this type of measurement because of its light weight, simplicity, and noise performance. The noise floor of our particular amplifier is measured to be 1030 e- and simulated to be as low as 140 e-. Both of these measurements are taken without averaging. To further verify and understand this device, I developed a novel simulation method using ANSYS Maxwell 3D to simulate the interaction between the charged particle and the electrodes of the ICD. The results from this simulation are then easily passed to Cadence where we can clearly see the response of the custom amplifier to the charged particle. This knowledge is used to study various types of electrode geometry for improved noise performance, as well as understand how particle trajectory affect the resulting signal.

Once the validity of the Maxwell simulation is established, I use it, along with experimental data and a mathematical model based on conformal mapping, to optimize the ICD for noise performance. I find that the maximum noise performance does not lie in simply increasing the number of sensing stages, as was previously thought. The optimum number of stages is a function of the parasitic capacitance of the amplifier, with the greater parasitic capacitance leading to the greater number of stages for the optimum.

Keywords: mass spectrometry, finite element model, optimization, modeling
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CHAPTER 1. INTRODUCTION

1.1 Project Objective

This project is primarily funded by NASA grant 80NSSC17K0101. Our goal is to create a lightweight, energy efficient device to fully characterize the charge and mass of the dust on the surface of Mars. For this phase of the project, we are working to move the current device concept from a technology readiness level (TRL) of 2 to 3. The last TRL, 9, is reached once a concept has proven flight worthiness through various successful mission operations, and while this device is still early in development, our design decisions have been made with that end in mind. We have optimized for weight, simplicity, and energy efficiency, all while maintaining standards of device functionality.

1.2 Thesis Outline

This thesis is organized into eight chapters. Chapter 2 motivates the problem of understanding Martian dust. Chapter 3 covers relevant information on image charge detection and charge detection mass spectrometry. Such information will give a clearer picture of how our proposed device functions. Chapter 4 contains details of how I developed the novel simulation technique we used for further understanding how our device interacts with charged dust particles. I go into specifics about the charge-sensitive electronics in chapter 5. Chapter 6 details the test setup that I helped build and design to verify the functionality of our device with actual charged particles. In chapter 7, I discuss methods I developed to optimize our device for charge
sensitivity. Finally, chapter 8 contains details about the future work necessary to further develop this concept.

1.3 My Contributions

I was personally responsible for the following aspects of the project:

- Developing an accurate simulation model to give us an in depth understanding of the operating principles of our device.
- Verifying the accuracy of the simulation by comparing its results with known mathematical models and experimental results.
- Collaborating with other team members on designing and building a novel experimental apparatus for testing the device.
- Verifying and troubleshooting the test apparatus and designing solutions.
- Running experiments with physical particles and producing publishable results.
- Compiling and editing papers for publication
- Deriving a mathematical model for calculating the capacitance of a PCB detector given a specific geometry
- Developing a method for determining the number of stages for optimum noise performance
CHAPTER 2. DUST ON MARS

2.1 Motivation

Dust is ubiquitous on the surface and in the atmosphere of Mars. Mars dust even made headlines recently after NASA's Opportunity was permanently knocked out by a massive dust storm [1]. Clearly, dust will need to be taken into account as we continue to explore the red planet. We are interested in the dust on Mars primarily for 2 reasons: 1. It drives climate and, 2. It can pose a serious threat to crewed missions.

2.2 Climate Driver

Because dust is so pervasive in Mars' atmosphere, it accounts for the majority of the solar IR radiation absorbed [2-4], making it a dominant driver for radiative models and climate [5]. Some have concluded that the role of dust on Mars in climate is analogous to that of water on Earth [6]. Certainly an important part of this role is the planet's dust storms. Storms are widely varied in size and duration but larger storms have been observed to engulf the entire planet and last for months [7,8].

It is likely that the atmospheric dust grains on Mars carry electric charge [9-11]. Such a charge could be significant in a number of phenomena including dust suspension, transport, sedimentation, and surface capture [8,12, 13]. Triboelectric processes (contact with other surfaces) are expected to account for most of the charging while some effect due to
photoemission is also speculated [14-16]. While no direct measurement has been made of Martian dust particle charge, lab simulations have been conducted under conditions similar to those of Mar's atmosphere. These studies have found that simulant dust grains ranging from 1-3 μm in diameter typically carry 1,000-10,000 elementary charges (negative or positive) from triboelectric charging alone [17,18]. These charges have the potential to generate large electric fields during dust storms [19,20], which can be relevant when interpreting remote sensing data. It is crucial that the effect of charged dust be taken into consideration when trying to understand the surface of Mars.

2.3 Hazards Caused by Dust

The risks posed to crewed missions by Martian dust are numerous. The most significant of these is the damage it can cause to in situ resource utilization systems. These systems are used to derive pure oxygen from the atmosphere of Mars, not only with the purpose of breathing but also to use as a propellant. Such a system is under development for the Mars 2020 rover and is intended to produce 440 g/hr of oxygen (a crewed mission requires 2.2 kg/hr) [21-23]. Dust could introduce serious problems for filtration systems. Especially considering that such resource utilization devices would need to run continuously in order to generate the necessary quantity of oxygen. Failure of these types of systems would mean absolute disaster for the crew and the mission.

Mars dust also poses a strong health hazard. A 2002 study of common silicates found on Mars discovered that the particles reacted with small quantities of water to produce highly reactive compounds known to cause lung disease [24]. In fact, these same compounds were
determined to be the culprit of the respiratory illnesses suffered by miners on Earth. This is a troublesome finding since dust is easily brought into the airlock and can then be inhaled.

Finally, dust is known to reduce efficiency of solar panels by .28% per day on average (see figure 2-1) [25]. During dust storms the sun can also be completely blocked out, rendering solar panels useless. This is precisely what decommissioned Curiosity.

Figure 2-1: Dust accumulated on solar panels of Opportunity [1]

2.4 **Our Device**

Despite all this, no instrument for directly measuring the charge and mass of dust on Mars' surface has been selected for future missions. Understanding the size and charge distributions of dust would facilitate the design of more robust equipment and inform
sophisticated climate models. Additionally, a device that takes continuous measurements would have the ability to monitor dust activity at different times of the day or year, during dust storms, or while the rover is engaging in various activities. Such data would further deepen our understanding of the Martian atmosphere.

Currently, the size distribution and concentration of suspended dust grains have only been inferred from inconsistent and unreliable optical scattering data. Multiple-wavelength data provided by the Mars Pathfinder showed a geometric cross-section-weighted mean particle radius of $1.6 \pm 0.15 \mu m$ [5]. However that result is contradicted by data from Mariner 9, Viking, Phobos, Phoenix, Spirit, Opportunity, Mars Science Laboratory, and other missions which gave mean particle radii ranging from $< 1.0 \mu m$ to $2.57 \mu m$ [2,3,5, 26-29]. These discrepancies between data sets are not simply due to changing conditions. Additionally, the widths of the distributions for the above data sets are uncertain [5]. One of the problems with the current models is that they assume single-modal particle size distributions while multi-modal distributions are likely due to the variety of minerals and processes present on the Martian surface [6]. Optical models are also cross-section weighted, giving basically no information about sub-mean sized particles, despite the fact that such particles may be the most plentiful [5].

The device that we have proposed relies on charge-detection mass spectrometry (CD-MS) to directly measure the charge and mass of dust particles. A diagram of the device is shown in figure 2-2. Since CD-MS requires a light vacuum environment, dust particles are brought into the device using a vacuum pump already present on the rover. The particles then flow past the sensing electrodes where their charge and mass are determined before they are output through a filter. This device can operate continuously, providing dust concentration at various times. It employs multiple sensing electrodes using printed circuit boards, allowing for the device to be
lightweight (less than 220 g). The device will also consume less than 340 mW of power. The purpose of this work is to move this concept from a technology readiness level (TRL) of 2 to 3 (on a scale of 1-10).

Figure 2-2: Overview of Proposed Instrument
CHAPTER 3. ICD AND CD-MS

3.1 Basic Principles

Image charge detection (ICD) is a technique for non-destructively observing a charged particle in motion and can be used to infer the particle's charge, velocity, mass, and other characteristics. In its simplest form, ICD functions as follows: As a charged particle approaches a conducting material, charge is built up on the surface of that material. As the particle continues its trajectory, and moves further away from the material, the surface charge recedes. This change in surface charge generates a small electrical current, which can then be manipulated and analyzed to characterize the particle.

ICD has been used in a variety of applications including ion-traps [30,31], ion implantation [32], and various forms of mass spectrometry [33-36]. In this context, ICD is employed for use in charge detection mass spectrometry (CD-MS).

CD-MS is a technique for the analysis of charged particles such as dust, polymers [37-39], biomolecules [40,41], and aerosols [42]. CD-MS is particularly useful in the detection of large particles because its mass detection limit is much higher than that of traditional mass spectrometry [40]. In CD-MS applications, the charge of the particle is first determined directly using ICD. Then the particle's mass can be measured by accelerating the particle with an electric field and using the time of arrival of the resulting signal peaks to determine the particle's acceleration. Acceleration, combined with the particle's charge and the applied electric field, can
then be used to deduce the particle's charge-to-mass ratio (m/z) [43]. This technique is known as time-of-flight (TOF) CD-MS.

3.2 History

CD-MS for the analysis of microparticles was first reported in 1960 [44]. This result featured pairs of conducting plates inside a shielded cylinder. In 1995, Fuerstenau and Benner presented the first biological application of this technique [40]. Their design consisted of a conductive sensing cylinder co-linearly flanked by two grounded cylinders of the same size, as shown in figure 3-1. Since then, many ICD systems, and virtually every CD-MS system, have utilized cylindrical electrodes, often with multiple sensing and grounded stages [45, 31, 32, 36] (example shown in figure 3-2). The ability to use copper electrodes on printed circuit boards (PCBs) for detecting image charges in CD-MS was reported in [45] and an image of that type of detector is displayed in figure 3-3. This development is significant because it greatly simplifies electrode alignment and manufacturing. It also opens the possibility for charge-sensitive electronics to be integrated directly with the detector, eliminating the need for excessive wires or cables and reducing complexity and parasitic capacitance. As stated in the previous chapter, our device employs this PCB technique for ICD.
3.3 Particle Acceleration

There are a number of ways to perform the particle acceleration necessary for deducing particle mass. One of these is through pairing an ICD electrode with an ion trap that is designed to oscillate ions in a linear, back-and-forth motion [33]. Not only does this reveal the particle's m/z, but it also takes advantage of repeated particle measurements which, as we will show later,
reduces detection limit. While theoretically this type of device may be possible using PCBs, it is currently impractical for use on Mars due to complexity and weight.

For a linear array of sensing electrodes, it has been demonstrated that particle acceleration can be achieved using an electric field that is generated through differential biasing of adjacent electrodes, e.g. the first electrode is grounded and the second is set to a potential of 1 V [46]. Another method uses a similar concept but the electric field is instead generated by a voltage pulse [47]. Both methods rely on the timing of the measured signal peaks to calculate m/z. Our device uses a similar, simpler, technique. Figure 3-4 shows a PCB detector with a long electrode placed in between two sets of sensing electrodes. A DC voltage is applied to this electrode to supply the field for particle acceleration. An example signal is also shown in figure 3-4. The times t_1, t_2, and t_3 are used to determine the particle’s acceleration due to the DC voltage applied to the acceleration region. This method is both simpler electronically and more power-efficient than current methods.

Figure 3-4: PCB detector with acceleration region and resulting signals
3.4 Current Challenges

Despite the widespread use of ICD, little work has been done by way of modeling interactions between charged particles, sensing electrodes, and amplifying electronics. A simple model was proposed in [48] and [49]. Their method is extremely powerful and is often used in conjunction with software simulators because closed-form mathematical solutions to their proposed equations only exist for certain simple geometries. Recently, modeling methods relying on this theorem have been proposed for ICD using simulators like SIMION [32,50]. However, such methods have typically only been reported using cylindrical electrode geometries.

Because of the lack of a thorough mathematical or simulation model, there is an incomplete understanding of how the signal output from the sensing electronics relates back to the charged particle. For example, the peak amplitude and the area under the transient output signal curve are both affected by the charge of the input ion, but it is unclear which of those two measures are most relevant in determining ion charge. Also, while there has been some speculation about the effect that the spacing between adjacent electrodes has on the rise time of the current signal [45], broader questions about the relationship between electrode geometry and the resulting induced signal still remain unanswered. For example, it is unclear how the signal is affected if we increase the distance between PCBs, creating a larger channel through which the particle can pass. Or, what happens to the signal if you shrink the electrode's size along a certain dimension? These questions are especially relevant for a PCB detector because making such adjustments can lower input parasitic capacitance, which would lower the amplifier's detection limit. However, making these design changes without an understanding of how the signal output is affected can lead to unforeseen errors.
Particle trajectory is another important factor to consider when dealing with PCB electrodes. This is because a charged particle's trajectory may fall outside of the space in between opposing plates. Cylindrical electrodes, on the other hand, don't suffer from this problem. Figure 3-5 depicts a simple PCB detector with a particle and vector showing its trajectory. In the figure, the particle is poised to travel right down the center of the detector, perfectly spaced in between the two PCBs and perfectly bisecting the electrodes along their x dimension. In this situation, it is assumed that the full charge from the particle will be induced onto the plates. However, what happens if that trajectory shifts in the x direction? We assume that at some point, less than the full particle's charge will be induced onto the electrodes, causing the output data to underestimate the amount of charge on the particle. The question is, when does that happen? How small of a region can the particle travel through and still induce its full charge onto the detector? This understanding is crucial in determining the degree of uncertainty in your measurements. A detailed model would illuminate some of these unanswered questions about how electrode geometry and particle trajectory affect the signal in an ICD system.

![Figure 3-5: CAD model of a PCB detector](image_url)
Another one of the fundamental challenges of ICD is reduction of the detection limit, with the ideal detector having the capacity to detect a single elementary charge. One approach for reducing this limit is by cascading multiple sensing electrodes in series (see figure 3-2). This allows for noise from the electronics to be averaged out across the multiple signals acquired, lowering the limit of detection by a factor of $\sqrt{N}$ ($N$ being the number of sensing electrodes) [43,46,51]. Similarly, the noise limit can also be lowered by repeated passes across the sensing electrodes through the use electrostatic mirror electrodes [33,52,53].

While this technique is extremely useful and can easily be employed by the design presented here, the fundamental noise limit is set by the electronics themselves. A common approach for improving the performance of the electronics is to cool the device or the input transistor [54]. Since most ICD systems use common similar singled-ended amplifier topologies, cooling is often the only option explored [38,45,46], resulting in expensive and energy hungry systems. However, the signals induced onto the sensing and grounded electrodes are near differential (as will be shown later) and lend the detector to use with a differential amplifier [31, 43]. Figure 3-5 shows a diagram of a typical PCB detector. In a single-ended ICD system, $V_{l,neg}$ would be connected to ground and $V_{l,pos}$ to the input of the amplifier. For a differential amplifier, both sets of electrodes are connected to amplifier inputs. We show that by utilizing a differential topology, the noise floor of the ICD system can be significantly reduced. For the current work, we report direct experimental comparisons between the singled-ended and differential topologies in order to highlight the improved noise performance of the latter. These comparisons are made without the noise reducing technique of repeated measurements in order to focus on the electronics.
CHAPTER 4. MODELLING

4.1 Primary Objectives

We have two main objectives in developing a simulation model for image charge detection (ICD) systems. The first is to gain insight into how electrode geometry and particle trajectory affect the induced signal. For example, figure 4-1 shows detecting electrodes identically printed on two PCBs. The PCBs are spaced apart from each other to create a channel through which charged particles can travel. Figure 4-1 also depicts a particle aligned to travel along the center axis of the detector (trajectory 1). We seek to understand what the induced signal will look like for particle trajectories that don’t follow the center axis. If the particle’s path is shifted along the x-axis, for example, how will that affect the induced charge on the electrodes? Will the particle’s charge be fully induced? A thorough simulation technique provides insight into the design of electrodes in such a way so as to minimize this kind of uncertainty. This technique also has the potential to facilitate electrode design such that the resulting signal is more compatible with the charge sensitive electronics. For example, the simulation can predict how the spacing between electrodes affects the rise time of the induced current signal. The bandwidth of the sensing amplifiers determines what range of rise times the device can tolerate. Thus, given the expected velocity of the incoming particle, we can determine what electrode spacing we need to ensure that the resulting signal falls within the bandwidth of our amplifier. The flexibility in design afforded by the PCB electrodes enables us to easily make
such adjustments. This flexibility also facilitates the exploration of new detector geometries which can be aided by the current simulation technique.

![Figure 4-1: CAD model of detector with particle and trajectory](image)

Our second goal is to better understand how this induced signal is processed by the charge sensitive electronics. Almost all ICD systems consist of a charge-sensitive preamplifier followed by subsequent shaping and filtering electronics [34,38,43,45,46,55]. The shaping stages are typically used to convert the preamplifier output to a series of peaks, making it easier to extract time-of-flight information from the signal. However, in order to definitively answer whether the relevant information from the output waveform is the peak amplitude or area under the curve (as discussed in the previous chapter), we will focus directly on the output of the preamplifier and exclude any discussion of shaping amplifiers, although such shaping stages will be included in the final device.
4.2 Maxwell 3D

The chosen electrostatic simulator was ANSYS Maxwell 3D [56]. We verified the accuracy of the software by comparing it with studied physical models[57]. We began by simulating the interaction between a charged particle and a single, square copper plate measuring 1 cm x 1 cm. We then plotted the surface charge density on the plate and compared the results to those found by [57]. Their work involved comparing the accuracy of the moment and image charge methods for calculating induced charge on a planar, rectangular surface. The geometry they worked with is identical to the one described here. Our simulated results are shown in figure 4-2. The white shading denotes areas of high charge density and the black those of low charge density. The particle is also shown in each plot. As expected, when the particle is close to the plate, the peak of the charge density is found directly below the particle. However, as the particle moves further away from the plate, charge density peaks accumulate on the edges of the plate, with the highest peaks found in the corners. These results are consistent with those found in [57].

![Figure 4-2: Charge density induced on copper plate by particle a) 5 mm and b) 5 cm distance from the plate.](image)

In order to produce signals generated by a moving particle, we create multiple Maxwell files, each with the charged particle located at an incremental position along the particle trajectory. Each file can be thought of as a frame taken along the particle’s trajectory. The
accuracy of the method is maintained because the particles in these applications travel far slower (typically on the order of 10 m/s) than the speed of light. Because the computational cost of running so many simulations (over 1000 per particle trajectory) is so high, the analysis is performed using BYU’s Fulton supercomputer. This means that all the computations need to be performed without the aid of a graphical user interface. Once computed, the simulation files are then moved to a local server where the total charge induced onto the plates in each frame is extracted by integrating the charge density over the surface of the plates, producing a total induced charge vs. position plot. This is done automatically using a Python script. Further processing of this plot along with an assumed particle velocity allows for the differentiation of the charge waveform, producing a current vs. time plot. A flowchart summarizing this process is shown in figure 4-3.

Figure 4-3: Flow chart depicting process for producing induced signals by charged particles.

We return again to image theory for an accuracy check. We generated simulated charge vs. position and current vs. time plots for a charged particle passing over a single conducting plate 1 cm by 1 cm in size. We also produced the same plot using equation 1, which was derived using image theory [57].
\[
\rho(t) = \frac{-Q}{\pi \varepsilon_0} \left[ \tan^{-1} \left[ \frac{(x_{pl} + vt + x_0)}{h \sqrt{(x_{pl} + vt + x_0)^2 + h^2 + (y_0)^2}} \right] - \tan^{-1} \left[ \frac{(x_{pl} + vt - x_0)}{h \sqrt{(x_{pl} + vt - x_0)^2 + h^2 + (y_0)^2}} \right] \right] \tag{1}
\]

In the equation, \( Q \) is the particle charge, \( x_{pl} \) is the initial \( x \) position of the particle, \( x_0 \) and \( y_0 \) are the \( x \) and \( y \) positions of the particle, respectively, \( h \) is the height of the particle above the plate, and \( v \) is the particle velocity. The calculated charge density was integrated over the size of the plate to obtain charge vs. particle position. The resulting plots are shown in figure 4-4 with the black lines representing the image theory plots and the gray lines showing those derived from simulation (dotted line represents the location of the plate). A particle speed of 50 m/s was assumed in order to produce the current vs. time result. The plots were normalized by the charge on the particle to show the percentage of the original charge induced on the plate. When compared to a finite element analysis, image theory should underestimate the total charge induced by the particle and the discrepancy between the two methods should become more pronounced as the particle moves further away from the plate [57], this is confirmed by our simulation and can be seen in figure 4-4.
Figure 4-4: Comparison of current simulation technique (Maxwell) with image theory (Im), a) charge vs. position and b) normalized current vs. time

4.3 Charged-particle Simulations

A clear advantage of the proposed model over mathematical methods like image theory is that the analysis can easily be applied to actual detector geometries which are too complicated to analyze using closed-form equations. Detectors with multiple electrodes are an example of such a geometry. The following signals were derived using the electrode design of figure 4-1. As shown in the figure, the first and last electrodes are connected to the negative input terminal of the amplifier, while the middle electrode is connected to the positive input. Both the top and bottom PCBs have the same connections such that when a particle passes through the space between PCBs, the induced signals on the top and bottom electrodes are routed to the same amplifier input. The dimensions of the detector are labeled in the figure. Using the same process described in figure 4-3, the black curves in figure 4-5 show the signals induced on $V_{i,pos}$ from a particle traveling along trajectory 1, with figure 4-5a showing the normalized charge vs. position and figure 4-5b the current vs. time. The current vs. time plot is the most relevant for our
application as this is the signal that will be input into the preamplifier. The gray plot of figure 4-5 will be explained shortly.

Figure 4-5: Comparison of signals induced on Vi,pos from two different trajectories, a) induced charge vs. time, b) normalized current vs. time. Dotted line represents location of the electrode.

It is worth noting that the computational cost of Maxwell is so high because it employs a FEM in solving Gauss’s law in the problem region. Because SIMION utilizes the Shockley-Ramo theorem, it can compute induced image currents in a fraction of the time. We ran the charged-particle simulation using the geometry of figure 1 in SIMION to compare its results with Maxwell. The resulting normalized current vs. position plots are shown in figure 4-6. While there are some differences between the two signals, they both produce current peaks of the same general shape. The purpose of the current work is not to determine which method is more accurate, but to establish a link between the detector geometry, input current signal, and charge sensitive electronics. For the remainder of the work, we continue to use Maxwell because it also has the capability to simulate detector capacitance, which is crucial for minimizing the noise floor of the ICD system.
In order to obtain an accurate reading, it is essential that the full charge from the particle is induced onto the sensing electrodes of the detector. Otherwise, the charge sensitive electronics will underestimate the amount of charge on the particle. The amount of charge that the particle induces on the electrode is wholly determined by the geometry of the conducting electrodes and the trajectory of the charged particle. If we reduce the sensing electrodes to two simple copper squares spaced a very large distance apart, and place a charged particle with charge \( Q \) exactly in between the squares, there would be almost no charge induced on the electrodes. However, as the electrodes move in toward each other, maintaining the charged particle in the middle, then more and more charge from the particle will be induced on the plates until each plate holds a total charge of \( Q/2 \). If we were to then move the particle toward the edge of the electrodes, while maintaining it on a plane parallel to and evenly spaced between the plates, eventually less than the total particle charge would be induced onto the plates. Thus, there is a region on this plane through which if the particle passes, all of its charge will be induced onto the electrodes. I’ll refer to this as the region of complete induction. Figure 4-7 illustrates this concept. Part (a) shows the particle trajectory that was used to obtain the plots. As shown, the particle traverses the detector,
bisecting the first electrode and traveling in the x direction. Figure 4-7b contains the resulting charge vs. position plot for a detector with the same dimensions as figure 4-1. For the given detector geometry, the particle has a 28-mm-wide window through which it can pass and still induce its full charge onto the electrode. This region is depicted in figure 4-1 with a cross-hatched gray rectangle overlaying the bottom electrodes. Maintaining constant all other variables, this region shrinks as the PCBs spread further apart. Figure 4-7c shows that the region of complete induction shrinks to 24 mm when the PCBs are spaced 4 mm apart rather than 2.5. Figure 4-7d shows the result of a case in which the PCBs are so far apart that there is no region of complete induction, only about 76% of the charge is induced at the maximum point. A similar trend occurs if the distance between PCBs is held constant, but the electrode size varies, with the region increasing with increased plate size.

If the charge falls within this region of complete induction, then it can vary in distance from one plate to the other and its full charge will still be induced on the plates collectively. The gray plot of figure 4-8a was derived from a particle traveling .25 mm from the electrode face (trajectory 1 shifted in the z direction by 1mm), I’ll refer to this as trajectory 3. As expected, this plot is nearly identical to that induced by a particle travelling along trajectory 1 (black plot in figure 4-8a). figure 4-8b shows the corresponding current signals, which don’t look identical at all. This is because the charge vs. time plots resulting from trajectory 3 are slightly steeper than trajectory 1 (i.e. when the particle travels closer to one plate, it’s charge is induced onto the detector faster than if it travels exactly between the two plates). This, however, is of little
concern because the output from the preamplifier will be nearly identical for both cases, as will be shown in the following chapter.

Figure 4-7: (a) Diagram of the trajectory used for simulation, (b) 2mm PCB spacing, (c) 4 mm PCB spacing, (d) 15 mm PCB spacing. Dotted line denotes region of complete induction.

The gray waveform in figure 4-5 resulted from simulating a particle that passed through the plates outside of the region of complete induction (trajectory 2). Trajectory 2 is simply trajectory 1 shifted in the x direction to the edge of the electrodes (depicted in figure 4-1). As shown in the figure, this particle induces a little over half of its charge onto the plates, causing the resulting current peaks to be smaller. We can therefore infer that an output signal that
contains peaks of varying heights from a single particle is potentially due to non-ideal particle trajectories, and to a certain extent, we can estimate that trajectory based on the peak heights.

Figure 4-8: (a) Charge vs. position and (b) current vs. time

Figure 4-9a shows an example of such a trajectory. In this situation, the particle takes a straight path between opposing corners of the detector. The resulting current signal of Figure 4-9b was derived using this trajectory. As shown, the first peak in the signal is lower than the second. This is because the particle enters the detector outside the region of complete induction. By the time it leaves the first electrodes, it has fully induced its charge and the current peak is significantly higher. The last peaks mirror this same behavior because of the symmetry of the detector with respect to the trajectory.
Figure 4-9: (a) Diagram of skew trajectory, (b) resulting current-vs.-time plot
CHAPTER 5.  THE AMPLIFIER

5.1  Theory of Operation

Integrator-based charge amplifiers utilize capacitors to accumulate charges to generate voltages according to $V = \frac{Q}{C}$, where $Q$ is the input charge and $C$ the input capacitance. The resulting voltage can then be subsequently amplified, filtered, and digitized for analysis. While a direct realization of this idea entails a single capacitor $C$ with one end connected to ground and the other end acting as the charge target (figure 5-1a), the circuit (usually an amplifier) sensing the voltage $V$ across the capacitor inevitably introduces parasitic capacitance ($C_p$) parallel to $C$. The parasitic capacitance can come from the amplifier’s input device, packaging, PCB trace, cabling, shielding, etc. $C_p$ may vary across different components, temperature, bias voltage, and be nonlinear, creating uncertainties in the effective total capacitance. Accuracy of the charge measurement is paramount in applications such as ours, and this parasitic capacitance makes it difficult to precisely calculate the incident charge for an output voltage. To solve this issue, a practical implementation of the charge amplifier typically assumes the alternative topology shown in figure 5-1b. Owing to the negative feedback, the amplifier maintains a virtual ground at node X. Hence, any charge incident on that node is transferred to the output node of the amplifier, producing $V = -\frac{Q}{C}$. In contrast to the previous topology, the output voltage is much less sensitive to $C_p$ if the amplifier’s open-loop gain is large. In the limit that the open-loop gain is infinity, $C_p$ has no effect on $V$ at all. Since the gain of the charge amplifier is $-1/C$, it is
desirable to minimize \( C \) so as to increase the gain to relax the noise requirements of the subsequent stages, and to improve the overall SNR.

![Figure 5-1: (a) Simple charge amplifier circuit using a shunt capacitor \( C \) and (b) charge amplifier using a feedback capacitor \( C \) with improved sensitivity to \( C_p \).](image)

A differential topology, as opposed to a single-ended, can reduce the circuit’s sensitivity to noise and interference. For example, supply noise and RF interference are typically present in a practical setup. These undesired signals can saturate the amplifier and easily crowd out the low level signals typical in charge sensitive applications like this one. But with a differential amplifier, the common-mode noise is rejected.

### 5.2 Our Amplifier

The amplifier used in our ICD system was designed by Yixin Song and was fabricated in a 180-nm complementary metal-oxide-semiconductor (CMOS) technology. The components referred to here can be found in the schematics of figure 5-2. The programmable feedback capacitors, \( C_{f1} \) and \( C_{f2} \), set the charge-voltage gain of the closed-loop amplifier. Owing to the integrated structure with a metal-insulator-metal (MiM) stack, \( C_{f1} \) is only 10 fF, thus achieving at least an order of magnitude increase in the detector gain compared to a discrete design that must rely on the smallest commercially available discrete capacitor (0.1 pF). The integrated capacitors also enjoy much tighter tolerances (about 5%) compared to discrete capacitors (50%) [15],
making it possible to have a vastly more consistent gain. \( C_{f2} \) (90 fF) can be programmably activated to lower the detector gain to avoid amplifier saturation for large inputs. The feedback resistor \( R_f \) establishes the input bias voltage of the amplifier core. This resistor is realized using pseudo-resistors [32] to obtain a large value of 128 G\( \Omega \) to create a small highpass corner of about 55 Hz for the input. Matching between the two feedback capacitors determines how well the amplifier can reject common-mode noise. Simulations show that even with a mismatch as large as 1%, a conservative estimate for integrated capacitors [33], the amplifier still achieves a good common-mode rejection ratio (CMRR) of over 90 dB.

Figure 5-2: (a) Differential charge amplifier with active reset, (b) core amplifier, and (c) common-mode feedback amplifier
Electrostatic discharge (ESD) events during the handling and assembly process of the charge detector (e.g. wire-bonding the amplifier to a PCB) can blow out transistors and render the amplifier useless. In order to avoid transistor damage, large ac-coupling capacitors $C_{in}$ have been incorporated to decouple the amplifier’s virtual grounds ($V_x$ nodes) to allow for the placement of ESD diodes ($D_1$ and $D_2$) to protect the sensitive elements. The diodes are designed to sense high voltages caused by ESD events and divert the resulting currents to the rail or ground.

An integrated active reset switch was employed in this design and, if activated, shorts the input to the supply voltage at a frequency up to 10 kHz. It is intended for use in applications in which charge is directly accumulated on the feedback capacitors. While this is not necessary for our application, active reset is used in characterizing the charge-to-voltage gain, as will be discussed below.

The amplifier core (figure 5-2b) adopts a differential folded-cascode topology for a large input common-mode range. The noise of the amplifier is dominated by the differential pair ($M_1$ and $M_2$). Therefore, the sizes of $M_1$ and $M_2$ and their bias current have been carefully selected to achieve low noise. Moreover, $M_9$ and $M_{10}$ are degenerated by $R_1$ and $R_2$ resistors to improve the noise performance. The amplifier exhibits an open-loop gain of 93 dB, open-loop bandwidth of 6.3 kHz, and an equivalent noise bandwidth of about 400 MHz. A common-mode feedback (CMFB) circuit (figure 5-2c) senses the output voltages and dynamically adjusts $V_{cmfb}$, which controls the gate voltage of $M_{11}$ and $M_{12}$ to force the output common mode to the reference voltage $V_{CM}$. The CMFB amplifier has degenerated input pairs ($M_{15-18}$) for stability and degenerated current sources ($M_{19-22}$) for low-noise. $V_{CM}$ can be tuned from off-chip for easy debugging. The output buffer increases the driving strength for large off-chip loads. An on-chip
shift register generates the programmable controls, such as gain mode. The amplifier consumes a total of 5.54 mW from a 1.8-V supply, a power consumption far less than the 340 mW originally proposed.

5.3 Verification of Charge-to-Voltage Gain

It’s crucial to have an accurate knowledge of the amplifier’s charge-to-voltage gain because accumulated charge on a collection electrode connected to an amplifier circuit is calculated by taking the voltage change at the amplifier’s output and dividing it by the charge-voltage gain. Typically, charge-voltage gain is measured by applying a known voltage step to a calibration capacitor connected to the amplifier input and calculating the gain by dividing the corresponding detector output voltage by the product of the voltage step and the calibration capacitance [59-61]. Consequently, the accuracy of this gain measurement relies on knowing the absolute value of the capacitor, which is difficult for an integrated design. So, we developed a new technique to determine the charge-voltage gain without a known calibration capacitance.

The technique employs a custom optoelectronic setup as shown in figure 5-3. The idea is to generate an extremely low and adjustable current and inject it into the charge amplifier, then observe the amplifier output to calculate the gain. The setup uses a low-power, single-mode Fabry Perot laser (1 mW) with an output wavelength of 635 nm. The photodiode is an Opto Diode model ODD-1W, a red-light enhanced silicon diode, operating under a reverse bias of 0.9 V. Several different photodiodes of this model were used for testing and each of their parasitic capacitances was measured to be between 6.2 pF and 6.4 pF with leakage currents ranging from 27 pA to 33 pA. The parasitic capacitance was accounted for during data acquisition because it affects the gain of the amplifier circuit.
Figure 5-3: Charge detector gain measurement setup using a custom optoelectronic system. The dotted box represents additional circuitry for photodiode current measurements.

During testing, a standard laser diode driver supplies the laser diode with 50 mA of current. The light produced by the laser diode is then guided through a fiber optic cable and into an optical attenuator. This attenuated light is guided to the photodiode through another fiber optic cable. This cable is connected to the photodiode by a black, 3D-printed, double-sided socket. The socket connects the laser fiber output to the top of the active area of the photodiode, which serves to provide a secure connection as well as to block out ambient light, allowing consistent measurements. The entire experiment is performed in a dark room to further reduce variability.

Obtaining an accurate gain measurement was achieved through a two-step process. First, a picoammeter measured the current through the reverse-biased photodiode. The measurements were taken at various laser attenuation levels and at various times in order to accurately characterize the amount of current flowing from the photodiode. To avoid saturating the amplifier, the current was measured at laser attenuation levels between 30 to 40 dB. At these levels, the measured current ranged from around 100 pA to 775 pA. Once the current had been measured, the picoammeter was replaced with the charge amplifier.
The gain of the amplifier was calculated using equations 1-3, with \( t_{AQU} \) defined as the time duration of the acquisition period, \( I \) as the input current measured by the picoammeter, \( q \) as the elementary charge, and \( n \) as the total number of elementary charges accumulated during acquisition. The minimum amount of charge used was limited by the photodiode’s dark current of 33 pA. With a reset frequency of 10 kHz, and an approximately 50% acquisition duty cycle, the minimum number of charges accumulated at the input was 9,476.

\[
Q_{\text{in}} = t_{AQU} \times I \tag{1}
\]

\[
\frac{n}{q} = \frac{Q_{\text{in}}}{q} \tag{2}
\]

\[
GAIN = \frac{\Delta V}{n} \tag{3}
\]

The gain of the charge detector was measured for a range of input capacitances, allowing us to experimentally verify the simulated gain vs. input capacitance curve, which was calculated using Cadence [58]. We swept the input capacitance by connecting discrete capacitors in parallel with the photodiode. We then measured the gain at each capacitance point using the optoelectronic setup described above. The results are shown in figure 5-4. Due to the parasitic capacitance of the photodiode, as well as the capacitance of the PCB, the minimum input capacitance tested was 11 pF. The highest gain measured was 8.9 \( \mu \text{V}/\text{e}^- \) at 11 pF and 1.7 \( \mu \text{V}/\text{e}^- \) at 94 pF was the lowest.
Figure 5-4: Charge-voltage gain versus detector input capacitance. Simulation results shown as a solid line and measurements as points.

Although the closed-loop amplifier reduces the gain’s sensitivity to the input capacitance, the gain still varies because of the finite open-loop gain of the amplifier and the finite ratio between $C_{in}$ and $C_r$. This variation is more pronounced at lower input capacitances because the $C_{in}$ to $C_r$ ratio is smaller. The maximum difference between measured and simulated gains from this sweep was 11%. Such a small discrepancy may be explained by errors of the feedback capacitors in the detector, as well as system noise and instrumentation errors. We therefore have high confidence in Cadence’s ability to predict an accurate gain vs. input capacitance curve.

## 5.4 Differential Amplifier for ICD

A differential amplifier is well suited for our ICD system because the signals produced by the repeated electrode pattern of the detector are nearly differential. As the charged particle leaves the vicinity of a plate, the induced charge on that plate begins to recede, causing a negative current peak to occur. Charge is simultaneously building on the subsequent plate, producing a positive current peak. These two peaks are identical in shape and are separated by a small time-interval caused by the spacing between the electrodes. This can be seen by comparing
the black and gray plots of figure 5-5, which were obtained by simulating the induced current using the 3-stage geometry of the previous chapter. Because the time-interval between gray and black peaks is small, the signal is effectively doubled when the positive input is subtracted from the negative, enabling all the advantages that come with using a differential amplifier.

![Figure 5-5: Current signals derived from Maxwell simulation, dotted line represents location of the electrodes](image)

The single-ended and differential configurations of the amplifier can be modeled as shown in figures 5-6a and b, respectively. The detector, wire, and PCB parasitic capacitances are lumped together and represented as Cp1 in the single-ended amplifier model. The differential amplifier model lumps the parasitic shunt capacitance as Cp2 and the parasitic coupling capacitance between the two inputs as Cx. The parasitic capacitance is strongly determined by the electrode geometry, as the detector is typically the largest contributor of capacitance. To study the effects of the parasitic capacitance on the charge-voltage gain ($A_{Q,V}$) and input-referred noise (IRN) of the amplifier, we sweep the input capacitance (Cp1 for the single-ended amplifier, Cp2 and Cx are scaled by the same factor and correspond to the differential amplifier) and observe the change in $A_{Q,V}$ and IRN (figure 5-7). These plots were calculated using Cadence. The solid line represents the differential amplifier and the dashed line represents the single-
ended. The differential amplifier exhibits a larger $A_{Q-V}$ and lower IRN than those of the single-ended for the same $C_p$. Both amplifiers show reduced $A_{Q-V}$ and IRN as the input capacitance increases. Because the detector capacitance in the differential configuration adds to the capacitance between input nodes, rather than from one input node to ground, the differential amplifier’s response to higher detector capacitance is less severe than that of the single-ended. This is a major advantage of using a differential amplifier.

Figure 5-6: a) Single-ended charge amplifier and b) Differential charge amplifier
The current signals shown in figure 5-5 were imported into Cadence to simulate the response of our charge amplifier to a charged particle passing through the PCB electrodes. Input signals were derived from particles with assumed speeds of 20, 50, and 70 m/s. The results are shown in figure 5-8. The simulation in Cadence was performed with $C_x$ and $C_p2$ values set to 2 pF each, which is realistic for this type of device. At this input capacitance, $A_{Q-V}$ is expected to be 16.28 $\mu$V/e-. The output of the amplifier in response to a charged particle aligns with this gain. With a charge of 1000 e- on the particle, the output ramp has a peak-to-peak amplitude of roughly 16.3 mV. Figure 5-9 shows the amplifier response to a particle with the same amount of charge, but which followed a trajectory .25 mm from the electrodes (discussed in the previous chapter, labeled Z Low in the figure) compared to a particle with a trajectory down the center of the detector. Although the input current peaks from this signal are higher than those of figure 5-5, their outputs are nearly identical. This is because the amplifier integrates current. Therefore,
the important factor in determining whether or not a particle will be properly interpreted is the percentage of its charge that is induced onto the electrodes.

![Charge Amplifier Output](image)

**Figure 5-8**: Output of charge amplifier with input generated from Maxwell 3D simulation. Input particles are traveling at, a) 70 m/s, b) 50 m/s, and c) 20 m/s

The charged particle simulation paired with Cadence definitively reveals that the peak amplitude of the output waveform, not the area under the curve, is proportional to the charge on the input particle. This remains true regardless of the particle speed. This same simulation technique can be easily employed to predict the response of other amplifier topologies. The detailed knowledge of the output waveform of the first amplifying stage can also be hugely beneficial in designing subsequent shaping electronics and predicting their performance.
Figure 5-9: Amplifier output given inputs from two particle trajectories: trajectory 1 (Z Mid) and trajectory 1 shifted to be .25 mm from the bottom electrodes (Z Low).
CHAPTER 6. TESTING

6.1 Testbench

To physically verify the advantages of using a differential amplifier, along with the accuracy of the discussed simulation method, we designed an experimental setup as shown in figure 6-1. The primary challenge associated with designing such a system is separating charged particles before they pass through the detector, as the presence of multiple particles leads to signal overlap and greatly reduces the likelihood for accurate charge measurement. To combat this problem, we designed a particle intake system in which particles enter the detector through a tube, carried by the flow of air produced by the Venturi vacuum generator. The purpose of this tube is to increase the probability of detecting a single charged particle. This is done through two mechanisms: 1. The tube selects only a small number of particles at a time, and 2. As particles of various surface areas and masses are exposed to roughly the same amount of force (provided by the airflow) for an extended period of time, they naturally separate by mass. The speed of the particle can be adjusted by tuning the output flow from the vacuum generator or by varying the pressure of the compressed air source. A photo of the setup is shown in figure 6-2.
Figure 6-1: Diagram of test apparatus A) high-voltage particle charging and intake, B) Venturi vacuum generator, C) pressurized air intake, D) shielding box, E) PCB detector and F) custom amplifier

Figure 6-2: Photos of the test setup a) with lid off and b) with lid on

6.2 Results

We focus on two comparisons in our tests. First, the widely used Amptek A250 [38,45,46,55] vs. the presented custom amplifier in differential configuration. Both devices function as preamplifiers and thus largely set the noise floor of the charge-sensing system.
Second, we compare the custom amplifier in a single-ended configuration versus a differential configuration in order to show the superiority of the latter in this particular application. Figure 6-3 shows the diagram of the PCB used to take these measurements. As shown in the diagram, the single-ended detector consists of two sensing electrodes separated by grounding electrodes. The differential detector features two negative and two positive input electrodes. By cascading the single-ended and differential sensing electrodes, a comparison can be made between the two amplifiers as they respond to the same particle. The result of the Amptek vs. custom design test is shown in figure 6-4. The gain of Amptek is shown to be .082 $\mu$V/e-, which is expected [59], while the gain of the differential amplifier is 7.96 $\mu$V/e-. Using those gains to refer the noise to the input, we find that the measured input referred noise (IRN) of the custom design outperforms that of Amptek by a factor of 13, with the custom amplifier exhibiting an IRN of 1700 e- and the Amptek 23000 e-. The sensitivity of the custom charge amplifier is so much greater than that of the Amptek, that even charges practically invisible to the Amptek appear distinctively in the custom amplifier output.

![Diagram of detector PCB used in comparison tests](image)

Figure 6-3: Diagram of detector PCB used in comparison tests
We validate our simulation method by comparing the simulation and measurement results. We generated simulated input current signals using the PCB in figure 6-3. Those signals were then input into the custom amplifier in differential and single-ended modes. The particle’s charge and velocity used in the simulation were chosen to match the experimental result in figure 6-5a. The output of the Cadence simulation is shown in figure 6-5b, with the experimental results shown in figure 6-5a. The experimental signals were filtered digitally using a low-pass filter with a cutoff frequency of 5 kHz. Overall, the waveform shape and noise characteristics of the experimental data are in excellent agreement with simulation. For the differential signal, however, there is a slight discrepancy in shape between simulation and experiment. This can be explained by the differences in the amplifier feedback resistance, resulting in a slightly different
leakage rate. The experimental signal also contains some low-frequency noise which is unique to the testbench and not easily simulated. Such noise also has a minor effect on waveform shape.

Figure 6-5: Differential (top plots) vs. single-ended (bottom plots) amplifier output in response to particle with identical charge and velocity, a) experimental and b) simulated results.

In terms of gain, the differential geometry outperforms the single-ended by a factor of roughly 2 and the Amptek amplifier by a factor of 97. This is expected, as the customer amplifier utilizes a much lower feedback capacitance (10 fF) than that of the Amptek (1pF). We estimate a charge of about 115,000 electrons on the particle which induced the signal. The observed noise floor of the single-ended and differential amplifiers at the given input capacitance is 1705 and 1030 e-, respectively. However, we have simulated that if the input capacitance is low enough, we can decrease the noise floor to less than 150 charges. In the given experimental setup, the input capacitance was quite high. This was primarily due to the detector PCB, which was designed to facilitate the measurement of a particle using both a differential and single-ended amplifier simultaneously. In typical applications, only one amplifier is necessary, allowing for the use of a PCB detector with much less parasitic capacitance.
CHAPTER 7. OPTIMIZATION

7.1 Introduction

As stated earlier, one of the primary goals of ICD is to reach a noise floor of one electron. The most common technique for reducing noise in ICD systems is averaging the outputs of repeated measurements, typically done through repeated detecting electrodes lined up along the trajectory of the particle. While this technique is effective, detection limits are dictated by the noise of the electronics. This is true in any system using electronic circuits for signal detection. The most critical component in most ICD detection circuits is a charge preamplifier whose noise limit is largely a function of input capacitance. Significant noise reduction follows a reduction in capacitance. However, for ICD systems, the largest contributor to input capacitance is usually the sensing electrodes connected to the preamplifier. Shrinking the amount of capacitance of these electrodes can have negative consequences, such as diminished signal accuracy. This occurs because electrode size is scaled down to reduce capacitance, which will cause the passing particle to induce less than its full charge if the sensing electrodes fall below a certain size threshold. Incomplete charge induction means that the calculated charge will underestimate the actual charge of the particle. Although this can be calibrated for, it will diminish charge sensitivity.

The link between input capacitance and charge sensitivity illuminates the tradeoff that exists between the number of sensing stages and input capacitance. While signal averaging is
done in an effort to reduce noise, the additional sensing stages add capacitance, reducing the sensitivity of the preamplifier. There must be a point where adding an additional sensing stage actually raises the noise floor rather than lowering it. We seek to understand where the optimum point lies in a design for a multi-electrode ICD system built on a PCB. This optimum point has yet to be studied.

This chapter will be organized in the following way: In order to quantify capacitance for different electrode designs on a PCB, we will compare a theoretical model for capacitance versus predictions made from a commercial modeling software (ANSYS Maxwell 3D) [56]. These results will be compared against measurements on actual PCBs. When we have established confidence in our capacitance predictions, we will use the modeling software to sweep parameters for multi-electrode PCB designs and come up with a minimum possible capacitance for a design of N electrodes. Factoring in the expected noise performance of a preamplifier, we will then provide guidance for minimum-noise designs for a PCB based ICD system.

7.2 PCB Detector Capacitance

7.2.1 Theoretical Model

Our purpose in developing a mathematical model for the capacitance of a PCB detector is twofold: 1. to further verify and increase our confidence in the simulation method we have already developed and 2. to gain greater insight into how certain detector design parameters, such as $g$, $l$, and $L$ (see figure 7-1) affect overall capacitance.
Figure 7-1: Diagram illustrating relevant dimensions for capacitance calculations, a) top view, b) side view, c) resulting current vs. time signal

We begin by defining closed-form equations for capacitance of the detector PCB based on conformal mapping. Coplanar capacitors have been in use since the 1970’s and are found in applications involving chemical sensing [69-72], microwave integrated circuits [73,74], dielectric thin films [75], and surface acoustic waves [76]. Mathematical models for the capacitance of such devices has also been studied since 1970’s, with the earliest equations proposed by Alley [73]. In 1977, a model based on conformal mapping techniques was proposed.
by Wei [77]. This model analyzed a coplanar capacitor with an infinite upper air layer. Since then, various models based on conformal mapping have been proposed to accommodate a wide range of capacitor geometries [64-67].

The current derivation for the capacitance of a PCB detector used for ICD is based on the work by Gevorgian et al. [78] with some original alterations to fit our geometry.

Figure 7-1a shows the top view of a single PCB used for particle detection, figure 7-1b shows a side view of the two PCBs forming a channel along with a charged particle traveling through the channel. As shown in the figure, there are two sets of connected electrodes labeled GND and SIG in the figure. These electrodes are connected to ground and the amplifier input, respectively. The grounded electrodes must always be placed in between adjacent sensing electrodes, as well as at the entrance and exit of the detector [45,43,79]. In a typical sensing application, a particle passes through the detector and induces its charge onto the surface of the sensing electrodes (SIG in the figure). This induced charge generates a small current at the SIG terminal (example shown in figure 7-1c) which is then amplified and analyzed to determine total charge on the particle. Both figure 7-1a and b illustrate the dimensions of the electrodes that are relevant factors in calculating capacitance. We first begin by deriving the capacitance of a single PCB, and then show that the equations can be easily adjusted to account for the second PCB.

In order to derive these equations, it is essential to have an understanding of how the electric field between adjacent electrodes behaves. The electric field distribution for detectors with 4 and 3 coplanar electrodes is shown in figure 7-2a and b respectively. As shown in figure 7-2a, the electric field distribution is identical between the inner-most stages and changes near the outermost stages. This is true for all detectors with more than 3 coplanar electrodes. figure 7-2b illustrates that for electrodes with 3 coplanar electrodes, the electric field distribution is
identical throughout [78]. Therefore, for a PCB with more than three coplanar electrodes, its capacitance can be split into two components: the inner electrode capacitance ($C_n$) and the outer electrode or 3 electrode capacitance ($C_3$), as shown below in equation (1).

\[ C = C_n + C_3 \]  

[1]

Figure 7-2: Electric field distribution for (a) 4 and (b) 3 coplanar electrodes. Electrodes are shown from the side and shown as the flat black lines in the figure.
7.2.2 Calculation of $C_n$ for a Single PCB

To illustrate the conformal mapping transformations, figure 7-3a shows the simplified case of two electrodes placed over a substrate. As shown in the figure, we are concerned with the capacitance between adjacent stages. Only half of the electrode from each stage produces a field that contributes to this capacitance. Because of the symmetry of this field (caused by the symmetry of the inner electrodes), $CC'$ acts as an electric wall, meaning that the capacitance between half-electrodes is equal to the capacitance between one half-electrode and $CC'$. To calculate this capacitance, we utilize the Schwarz-Christoffel conformal mapping to transform the rectangle $0256$ from the $z$-plane to the $t$-plane [63]. This transformation is shown in equation (2) and depicted graphically in figure 7-3a and b. The corresponding points from figure 7-3a and b are shown in equation (3).

\[
T = \cosh^2 \frac{\pi x}{2h} \quad [2]
\]

\[
t_0 = 1, t_1 = \cosh^2 \left( \frac{\pi s}{2h} \right), t_2 = \cosh^2 \left( \frac{\pi (s + g)}{2h} \right),
\]

\[
t_3 = t_4 = \infty, t_5 = -\sinh^2 \left( \frac{\pi (s + g)}{2h} \right), t_6 = 0 \quad [3]
\]
Figure 7-3: Graphical depictions of conformal mapping transformations from the (a) $z$-plane to the (b) $T$-plane to the (c) $W$-plane

We then map the upper half of the $T$-plane onto the interior of a rectangle in the $W$-plane. The mapping function is derived using the technique of approximate transformations [63] and is shown in equation (4). Using the vertices in the $T$ and $W$-planes to determine the constants $A$ and $B$ leads to equation (5), where $K$ represents the modulus of the elliptic integral of the first kind evaluated at $k$ and $k$-prime, which are defined in equation (6).

\[
w = A \int_t^{t_0} \frac{dt}{\sqrt{(1-t_0)(1-t_1)(1-t_2)(1-t_0)}} + B \]  

[4]

\[
C_{n,l} = \frac{1}{2} \varepsilon \varepsilon_0 \frac{K(k_{n,l})}{K(k_{n,l}')} \]  

[5]

\[
k_{n,l} = \frac{\sinh \frac{\pi s}{2h_l}}{\sinh \frac{\pi (s+\theta)}{2h_l}} \times \sqrt{\frac{\cosh^2 \left( \frac{\pi (s+\theta)}{2h_l} \right) + \sinh^2 \left( \frac{\pi (s+\theta)}{2h_l} \right)}{\cosh^2 \left( \frac{\pi s}{2h_l} \right) + \sinh^2 \left( \frac{\pi s}{2h_l} \right)}} \]  

[6]
\[ k' = \sqrt{1 - k^2} \]

In the above equations, \( C_{n,i} \) and \( k_{n,i} \) are calculated for each substrate layer, where \( i = 1, 2, 3, \ldots \). Each value is then combined to form the total capacitance as will be explained shortly. In our case, layer 1 represents the PCB substrate and layer 2 the air between the PCBs. The simple case of capacitance between floating electrodes without a substrate \( (C_{n,0}) \) also factors into the total capacitance and is found in the limiting case where \( \varepsilon = 1 \) and \( h = \infty \) (shown in equation (7)).

\[ C_{n,0} = \frac{1}{2} \varepsilon_0 \frac{K(k_{n,0})}{K(k'_{n,0})}, \quad k_0 = \frac{s}{s+g} \]  

[7]

7.2.3 Full Detector

We can now take the above results and derive an equation for the inner electrode contribution to the complete detector capacitance (both PCBs). Using the partial capacitance technique [64-66], the total capacitance can be represented as the sum of the partial capacitance contributions of each dielectric layer. The equation is shown in (8), where \( C_{n,0} \), \( C_{n,1} \), and \( C_{n,2} \) are capacitances due to the infinite air layer (equation (7)), the FR4 of the PCB, and the air layer between PCBs, respectively. \( N \) is the number of stages. Equation (8) accounts for the capacitance contributed by both PCBs of the detector.

\[ C_n = (N - 3)(C_{n,0} + C_{n,1} + C_{n,2}) \times l \]  

[8]

Figure 7-4 details the electric field distribution of the full detector. As evidenced, the electric field distribution facing outward is identical to that shown in figure 7-2. For the inward facing distribution, the electric field is contained in half the space between PCBs. This is because as the electric field lines emanating from opposing electrodes begin to approach each other, the
field components perpendicular to the electrode faces begin to cancel each other out, leading to a sort of “compression” of the electric field. Because of this, in calculating $C_{n,2}$, $h_2$ is chosen to be half the distance between the two PCBs ($p_2/2$). $C_{n,1}$ is calculated with $h_1$ selected to be the thickness of the FR4 ($\varepsilon_r \sim 4.4$) of an individual PCB. The relative dielectric constants used are $(\varepsilon_{FR4} - 1)$ and 1, for the PCB layer and air layer.

![Electric field distribution](image)

Figure 7-4: Electric field distribution for a full detector. Electrodes are shown from the side and shown as the flat black lines in the figure.

### 7.2.4 Outer Electrode Capacitance ($C_3$)

The formulas used for calculating the outer electrode capacitance are the same employed by Ghione and Naldi [67] and are shown in equations (9) – (13).

\[
C_3 = 4 \varepsilon_3 \varepsilon_0 \frac{K(k_{3,0})}{K(k'_{3,0})} \times l \quad [9]
\]

\[
\varepsilon_3 = 1 + q_{3,1} (\varepsilon_{FR4} - 1) + q_{3,2} \quad [10]
\]
\[ q_{3,t} = \frac{K(k_{3,t}) K(k'_{3,0})}{K(k'_{3,t}) K(k_{3,0})} \]  

[11]

\[ k_{3,0} = \frac{s}{s+2g} \frac{1 - \left( \frac{s+2g}{s+2s} \right)^2}{1 - \left( \frac{s}{s+2s} \right)^2} \]  

[12]

\[ k_{3,t} = \frac{\sinh \frac{\pi s}{2h_t}}{\sinh \frac{\pi (s+g)}{2h_t}} \frac{1 - \left( \frac{\pi (s+2g)}{2h_t} / \sinh \left( \frac{\pi (s+2g+2s)}{2h_t} \right) \right)^2}{1 - \left( \frac{\pi s}{2h_t} / \sinh \left( \frac{\pi (s+2g+2s)}{2h_t} \right) \right)^2} \]  

[13]

7.3 Computer Model

Maxwell 3D uses a finite element method to solve for the electric field in all regions of the defined problem area [56]. For the current application, one set of electrodes are designated sensing, and other grounded. As shown in figure 7-1a, the electrodes alternate from grounded to sensing, with the electrodes from each PCB featuring an identical grouping. To solve for the capacitance between the sensing and grounded plates, the sensing plates are set to a voltage of 1 V and the grounded to 0 V. Once the simulation is completed, the capacitance is easily calculated. This process can be easily automated to allow capacitance to be computed as various geometric parameters of the detector board are swept.

7.4 Comparison of Theory, Computer Model, and Experiment

We compare the results of capacitance sweeps derived from simulation, experiment, and the conformal mapping described above. As the basis for the following geometry sweeps, we use the geometry of figure 7-1, with \( g = 3 \) mm, \( s = 15 \) mm, \( l = 35 \) mm, and \( p_s = 2.5 \) mm. Using Maxwell and the above equations, we swept each one of those variables while holding the others
constant. The results are shown in figure 7-5 along with the specific range that each variable was swept at.

As evidenced by the figure, the mathematical model underestimates the nominal capacitance value (assuming Maxwell 3D has the correct results), and a similar result has been shown in previous work [68]. This error can be approximated very closely by simply multiplying the mathematical model’s calculated capacitance by a constant scaling factor, which has already been done in the lines labeled CM in figure 7-5. For our purposes, we are more concerned with

Figure 7-5: Maxwell 3D (Maxwell) simulation compared with the conformal mapping mathematical model multiplied by a scale factor (CM). a) Sweep of s from 1 to 30 mm, b) sweep of g from 0.5 to 13 mm, c) sweep of ps from 1 to 30 mm, d) sweep of l from 35 to 55 mm.
how capacitance changes as a function of specific geometric parameters. In this sense, the mathematical model matches very closely to the results from Maxwell 3D. As \( g \) increases, the capacitance asymptotically approaches zero. Conversely, it looks to approach infinity as \( g \) approaches zero. This makes sense conceptually, as one would expect the capacitance to diminish as the space between adjacent plates increases, and vice versa. The capacitance behaves as a logarithmic function of \( s \) or \( p \), and a dramatic reduction in capacitance can be achieved with a small shift in either of these parameters if the values of \( s \) or \( p \) are already small. However, typical electrodes are larger and often fall in the region where the capacitance vs. \( s \) curve has begun to level off. Capacitance increases linearly with \( l \), as is expected.

An unexpected result of our analysis is that as the PCBs separate, the total capacitance goes up. Whereas for a parallel plate capacitor, the opposite is true. Because the capacitance is found between coplanar adjacent electrodes, it relies on fringing electric fields. As the PCBs come closer together, the fringing electric fields are compressed, leading to less capacitance.

To verify the increasing capacitance with PCB separation and to determine whether the mathematical model or Maxwell 3D calculations were more accurate, we manufactured two separate PCBs with the following parameters: \( g = 1 \) and \( 1.6 \) mm and \( s = 7.5 \) and \( 17.5 \) mm, respectively, with \( l = 12.5 \) mm for both PCBs. The spacing between PCBs was varied between \( 1.6 \) and \( 8 \) mm. At each PCB spacing, the capacitance was measured using an HP 4280A capacitance meter (photo of the PCBs shown in figure 7-6). Simulations with identical parameters were then run using Maxwell 3D. The results are shown in figure 7-7 (board 1 refers to the first set of parameters listed above and board 2 the second). As evident, the trend of increasing capacitance with increased PCB spacing is confirmed. Additionally, once parasitic capacitance from the test wiring is subtracted out (about \( .8 \) pF), Maxwell 3D simulation and
experiment exhibit excellent agreement. Based on these results, we have high confidence in the absolute capacitance values predicted by Maxwell 3D simulations over a wide range of electrode geometries.

Figure 7-6: Photo of the PCBs

Figure 7-7: Sweeping ps from 1.6 to 8 mm for the geometries of, a) board 1 and b) board 2, crosses represent capacitance values obtained experimentally, solid lines were acquired using Maxwell 3D
7.5 PCB Charge Detector Parameters

As we contemplate outlining the process for designing an optimum PCB charge detector, there are two obvious criteria that any design should satisfy: 1. Accuracy of the charge reading producing as much induced charge as possible and 2. Minimizing capacitance to decrease the amount of noise on the amplifier electronics.

First we address the criterion of full charge induction onto the sensing electrodes. Whether or not a particle’s charge is fully induced is completely determined by the geometry of the electrodes [79]. The specific parameters that affect charge induction are \( s, l, \) and \( p_s \) (see figure 7-1). To study this effect, we ran simulations in Maxwell 3D using the same geometry as figure 7-1. A charged particle was placed equidistant from the two PCBs, and directly in the center of the first sensing stage. A value was assigned to \( p_s \), \( l \) was chosen to be much greater than \( p_s \) and \( s \), and \( s \) was swept from 2 mm to 35 mm, leading to a \( s:p_s \) sweep from 0.5 to 8.75. The total percentage induced charge as a function of \( s/p_s \) is shown in figure 7-8. As evidenced by the figure, an \( s/p_s \) ratio of 2.75 guarantees the full induction of the charge onto the sensing electrodes (the figure actually suggests that more than the full charge is induced, this is simply simulation noise). This simulation was performed using various values for \( p_s \) and the same ratio was found each time.
The $l/p_s$ ratio must also be at least 2.75 in order to ensure complete charge induction. However, if $l/p_s$ is equal to 2.75 there will be an extremely narrow path through which the particle can travel and still induce its complete charge. In practice, $l/p_s$ will be chosen based on the known range of trajectories that the particle can take.

Determining the detector design with the minimum capacitance, given a specific set of parameters, is quite straightforward. The parameters $L$ and $p_s$ are selected based on device constraints, such as the size of the entire detector, and particle trajectory constraints, such as the range of trajectories that the particle is likely to take. Because of this, these parameters will remain constant as the number of stages is increased. Once $p_s$ has been determined, minimum values for $l$ and $s$ are known based on the ratio discussed above. The final detector variables to determine are $N_s$ (number of sensing stages – which is the main subject of this analysis), and $g$.

As shown in figure 7-5b, capacitance decreases as $g$ increases. So the detector that minimizes capacitance will space adjacent electrodes as far apart as possible. Thus for a given $L$ and $s$, $g = \frac{L - N \cdot s}{N - 1}$ ($N$ is the number of electrodes, not stages). Figure 7-9 shows two boards of minimal capacitance, one with $N_s = 1$ ($N = 3$) and the other with $N_s = 2$ ($N = 5$). Because the optimum
detector is the one which maximizes \( g \) for a given \( N_s \), the capacitance of the detector as a function of \( N_s \) can be automatically calculated.

![Diagram](image)

**Figure 7-9:** Minimized capacitance detectors for (a) 1 sensing stage, (b) 2 sensing stages

### 7.6 Multi-Stage Design Optimization

Based on our guidelines for \( s \) and \( g \) based on inducing full charge and minimizing capacitance between stages, we are now ready to determine the optimum number of stages for minimizing detector noise. For an ideal pre-amplifier, the noise vs. input capacitance curve is a straight line through the origin, an example of which is illustrated with the solid line in figure 7-10a [80]. In order to determine the noise when repeated stages are attached to the pre-amplifier, we begin with a detector consisting of one sensing stage (flanked by two grounding electrodes). For this detector, the noise is simply found by calculating the capacitance of the PCB and using the line shown in figure 7-10a. This calculated noise value for a single stage is denoted by the first point in figure 7-10a (specific detector parameters are \( s = 15 \) mm, \( L = 170 \) mm, \( l = 25 \) mm, and \( p_s = 2.5 \) mm). Adding another sensing stage means the addition of 2 more electrodes: one for sensing and one for grounding. \( N \) and \( g \) are adjusted accordingly and the new capacitance is
calculated. Again we use the plot of figure 7-10a to determine the noise at this new capacitance. However, since we are now taking 2 measurements, we can divide this value by $\sqrt{2}$ to account for possible signal averaging. We repeat this process as we add more sensing stages, dividing each noise floor value by $\sqrt{N_s}$. The noise floors of detectors with up to 9 repeated stages are shown with the points in figure 7-10a.

![Figure 7-10: Input referred noise vs. input capacitance for (a) ideal amplifier and (b) non-ideal amplifier with 5 pF of parasitic capacitance, and (c) with 18 pF of parasitic capacitance. The solid line represents the noise performance of an individual amplifier with one sensing stage, the points show the noise characteristics of a system which uses signal averaging from multiple sensing stages.](image)

As shown in the figure, adding additional stages does not actually improve noise performance. This makes sense intuitively because going from one to two stages more than
doubles input capacitance, causing the noise floor of the amplifier to rise by the same rate, while only improving the noise by a factor of $\sqrt{2}$ through measurement averaging. However, this is only true for an ideal amplifier that exhibits zero parasitic capacitance. In practice, sources of parasitic capacitance can never be fully eliminated and are found in the amplifier chip itself, the PCB which houses the amplifier and discrete components, and any extra wiring in the system.

Figure 7-10b depicts an example of the noise vs. capacitance plot of a non-ideal amplifier in which the parasitic capacitance manifests itself as a vertical offset in the plot. Along with the line representing amplifier noise are calculations for a detector system with a varying numbers of stages (shown as asterisks). As shown in the figure, there is indeed a point where repeated sensing stages offers improved noise performance over a single stage. In figure 7-10b, the optimum noise performance is observed at 3 sensing stages. Figure 7-10c shows the noise performance plot for an amplifier which has 18 pF of parasitic capacitance. In this case, the optimum occurs at 5 stages. There is, however, a small difference in noise floor between detectors with 4, 5, and 6 repeated stages. The minimum in this case (5 stages) only performs about 4% better than a 6 stage detector and only about .5% better than a 4 stage detector. However, as the number of stages increases much beyond this optimum point, the input noise floor does as well. We will demonstrate how to find the minimum point, but in practice if the detector is off from that point by one or two stages the noise performance will not suffer greatly.

With the understanding gained from analyzing amplifier noise models, we can develop more general guidelines for designing PCB detectors with near optimum noise performance. Equations (14) and (15) show the noise floors of the single and multiple sensing stage detectors, respectively.

$$n_1 = m(C_{d1} + C_p)$$  \[14\]
\[ n_N = \frac{m}{\sqrt{N_s}} (C_{dN} + C_p) \]  \[ \text{[15]} \]

Where \( m \) is determined by the amplifier, \( C_{d1} \) and \( C_{dN} \) are the capacitances of the single and \( N \)-stage detectors, respectively, and \( C_p \) is the parasitic capacitance of the amplifier. We can eliminate the \( C_{d1} \) term in (14) because \( C_p \) (typically around 10 pF) is often at least 10 times greater than \( C_{d1} \) (typically less than 1 pF) \[79\]. We wish to know at what points \( n_1 > n_N \). Once this is determined, we then pick from these points the value of \( N_s \) which has the lowest noise floor. We combine (14) and (15) in equation (16).

\[ mC_p > \frac{m}{\sqrt{N_s}} (C_{dN} + C_p) \]  \[ \text{[16]} \]

Which simplifies to equation (17).

\[ C_p > \frac{1}{\sqrt{N_s}} (C_{dN} + C_p) \]  \[ \text{[17]} \]

To frame (17) in terms of how detector capacitance increases with an increase in sensing stages, we define the following ratios: \( \sigma = \frac{C_{dN}}{C_{d1}} \) and \( \rho = \frac{C_p}{C_{d1}} \). Substituting these into (17) and simplifying leads to equation (18).

\[ \rho > \frac{1}{\sqrt{N_s}} (\sigma + \rho) \]  \[ \text{[18]} \]

Where \( N_s > 1 \). Since \( \rho \) is fixed our focus will be on \( \sigma \) and how detector capacitance increases with the number of stages.

The problem with studying \( \sigma \) as a function of number of stages is that with each added stage, \( N \) increases and \( g \) decreases. Based on the equations that we’ve described, capacitance
increases linearly with $N$. As $g$ decreases, capacitance follows the trend shown in figure 7-5b. How these two variables combine to affect capacitance is not clear on an intuitive level, but it can be plotted to reveal a general trend. Figure 7-11 shows the capacitance as the number of sensing stages increases. As evidenced, the plot appears to follow an exponential trajectory. The problem with this sweep is that it requires a specific set of parameters, leading to a loss in generality. However, some of that generality can be recaptured by normalizing the plot by the capacitance of the single-stage detector (as was done for figure 7-11), which removes the curve’s dependence on the PCB parameters $l$ and $p_s$.

![Figure 7-11: Capacitance as a function of number of stages](image)

Finally, we are able to provide guidance for optimizing the PCB detector for noise performance. Once $L$ and $p_s$ are chosen, $C_{d1}$ can be calculated along with $C_{dN}$ for $N > 1$, revealing for which stages equation (18) is true (see figure 7-10b and c). Out of these data points, the number of stages which has the least amount of input referred noise is then selected. Figure 7-12 was derived using this method, with figure 7-12a showing the number of optimum stages as a function of $L$, all other detector parameters held constant (except for $g$, which shrinks with increased stages as described above). The gray plot represents an amplifier with 20 pF of
parasitic capacitance and the black one of 10 pF. As shown, for a higher parasitic capacitance (greater value of $\rho$), the optimum number of stages tends to be greater, which is expected given equation (18) and figure 7-10. The greater the vertical offset in the plot, the more room there will be for improvements to be made through repeated stages. As $L$ increases, the optimum number of stages increases as well. Again this is also expected, because with a larger $L$ comes a much greater initial value for $g$, putting the contribution of a shrinking $g$ to the overall capacitance at a much more gradual location on the curve shown in figure 7-5b and figure 7-11. Figure 7-12b shows a similar plot but as a function of $s$. As shown, as $s$ increases, the number of optimum stages decreases. A larger $s$ means smaller initial $g$, which places the detector closer to the quickly increasing portion of the curve in figure 7-11. As the number of stages goes up, capacitance increases quickly and equation (18) is invalidated.

![Figure 7-12: Optimum stages as a function of (a) L and (b) s. Dotted gray lines represent a parasitic capacitance of 20 pF, black 10 pF](image)

This method of noise reduction can also inform the use of other noise reduction techniques. For example, the output from an ICD can be analyzed in the Fourier domain. In this
case, noise level is inversely proportional with time-of-flight (which can be shortened or lengthened by altering $L$) [43]. However, $L$ cannot be increased arbitrarily as with longer flight times comes greater probability that the particle will collide with the electrodes or leave the detector. Thus when the desired time-of-flight and corresponding $L$ are selected, this analysis can be performed to find the optimum number of stages and further improve noise performance.
CHAPTER 8.  FUTURE WORK

8.1 Charge Detection Mass Spectrometry

Charge detection mass spectrometry (CD-MS) requires that the particle’s charge and mass be measured. We have successfully demonstrated charge measurement, and while mass measurement has been performed for a similar design [45], we have not demonstrated it in our lab. The current methods for particle acceleration (discussed in chapter 3) rely on fringing electric fields between adjacent electrodes. These fields are often difficult to model, leading to inaccurate mass readings. They are also quite weak and require large voltages. Such voltage sources can require extra equipment and also serve as a burdensome noise source in the detection system.

For these reasons, we propose a novel acceleration method shown in figure 8-1. In this architecture, the particle’s charge is first sensed in an array of electrodes, using methods identical to what has already been discussed. Then, the channel opens up where the particle is subjected to an electric field. This field attracts the particle to the bottom plate, which is connected to the amplifier input, eventually resulting in a collision with the plate. This event is recorded by the amplifier and can then be used to obtain time-of-flight information, revealing the particle’s mass. This method will provide more accurate mass readings and reduce the voltage necessary to accelerate the particle.
One of the central advantages of using a PCB sensing architecture is that the charge-sensitive electronics may be integrated directly onto the detecting PCB. This reduces the complexity and weight of the device, which is extremely desirable for space applications. It also eliminates the large parasitic capacitance caused by cables used to connect sensing electrodes to electronics.

While this idea has been proposed, it has never been demonstrated. Since our experimental setup is built and well-functioning, we simply need to design, manufacture, and test the new PCB. The PCB will need to be designed to minimize parasitic capacitance. We will need to be cautious with ground planes, traces, etc.

### 8.3 Channel Multiplexing

The more dust measurements we take, the more accurate our models of Martian dust will be. Increasing the number of detection channels is an efficient way to achieve a higher volume of measurements. A diagram of a multiplexed detector is shown in figure 8-2. Another benefit of such a multiplexing system is that the channels can be designed in such a way as to filter out particles based on mass.
The challenges associated with designing such a multi-channel system include: producing the necessary laminar flow in each channel, creating mass selective channels, integrating electronics directly on the detecting PCB.

8.4 Digital Filtering

Because of the weight and power restrictions associated with a mission to Mars, it is likely that any signal shaping will need to be done digitally. An efficient, digital bandpass filter will need to be designed to extract peaks from the voltage amplitude of the preamplifier signal. We will also need to design software to automatically process this data so that the quality of the measurements can be determined in real time.
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