PVT-Tolerant Stochastic Time-to-Digital Converter

Khalil Jacob Gammoh

Brigham Young University

Follow this and additional works at: https://scholarsarchive.byu.edu/etd

Part of the Engineering Commons

BYU ScholarsArchive Citation
https://scholarsarchive.byu.edu/etd/7692

This Thesis is brought to you for free and open access by BYU ScholarsArchive. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of BYU ScholarsArchive. For more information, please contact scholarsarchive@byu.edu, ellen_amatangelo@byu.edu.
ABSTRACT

PVT-Tolerant Stochastic Time-to-Digital Converters

Khalil Jacob Gammoh
Department of Electrical and Computer Engineering, BYU
Master of Science

Time-to-digital converters (TDC) are widely used in light-detection-and-ranging (LIDAR) systems to measure the time-of-flight. Conventional TDCs are sensitivity to process, voltage, and temperature (PVT) variations. Recent work utilizing the stochastic delay-line TDC architecture has demonstrated excellent robustness against PVT variations. But important issues affecting the linearity of a stochastic delay-line TDC has yet to be recognized and addressed.

This thesis rigorously analyzes the problem of linearity of a stochastic delay-line TDC and formulates an intuitive theory to predict the linearity performance. A polar visualization of the phase distribution of a delay line is proposed to aid the analysis. Based on the results of this study, this thesis proposes a stochastic delay-line TDC employing a delay-locked loop (DLL) to guarantee linearity over PVT variations and to reduce the number of redundant bits. The proposed TDC is implemented in a 0.18 µm CMOS process to validate the linearity theory and the proposed solution. The 8-bit TDC samples at 60 MHz and demonstrates a linear-number-of-bit of 6.36 with only 2-bit redundancy. Consuming 25 mW from a 1.8 V supply, the TDC yields a figure-of-merit of 5.04 pJ/conversion-step. With the DLL turned off, the integral nonlinearity (INL) degrades by about a factor of two, verifying the effectiveness of the proposed solution. The TDC is measured at different temperatures and supply voltages to demonstrate robustness against PVT variations. The measurement results show excellent agreement with the behavioral simulations.

Keywords: Time-to-digital converter, TDC, stochastic, PVT tolerance, delay-locked loop, DLL, LIDAR
ACKNOWLEDGMENTS

I would like to express my sincere gratitude to Professor Shiuh-hua Wood Chiang for all the things he taught me and for his constant support, patience, motivation, and technical insight during my master's degree. His guidance helped me throughout my research and writing this thesis. I could not have completed my master's degree successfully without his feedback. I would like to sincerely thank Professor Doran Wilde for his advice, insightful feedback and encouragement.

I would like to thank Professor David Penry for his contribution to this work and for his insightful feedback, I also would like to express my gratitude to Professor Armin Tajalli at the University of Utah for his insights and guidance, Professor Aaron Hawkins for his help in testing this design, and Professor Stephen Schultz for being on my committee.

I would like to thank Dr. Kent Layton and Rishi Singh at ON Semiconductor for their advice, guidance and practical solutions. I would like to thank my fellow lab-mates and my friends for all their encouragement and support during my masters. I thank Andres, Eric, Danilo, Pouria, Alex, Nate, Yixin, Andy, Mark, Jeff, Munther, Ala’a, Laith and Ghassan for all the support and help that led to the success in this endeavor.

Finally, I thank my parents and my dear brothers Sharif and Ramez for their encouragement, support and sacrifices. They have always taken great interest in my education and all other aspects of my life.
# TABLE OF CONTENTS

List of Tables ......................................................................................... vi

List of Figures ......................................................................................... vii

Chapter 1 Introduction ........................................................................... 1
  1.1 Motivation ....................................................................................... 1
  1.2 Prior Work ...................................................................................... 2
    1.2.1 Stochastic TDCs .................................................................... 5
  1.3 Outline ........................................................................................... 9

Chapter 2 TDC Analysis ......................................................................... 10
  2.1 Problem of Non-Integer Wrap-Around ........................................... 10
  2.2 Integer Wrap-Around ..................................................................... 15
  2.3 Effect of Nonidealities .................................................................. 18
    2.3.1 Jitter ..................................................................................... 20
    2.3.2 Mismatch ............................................................................... 21
    2.3.3 Supply Voltage Variation ....................................................... 23
    2.3.4 Temperature Variation ........................................................... 25

Chapter 3 TDC Architecture ................................................................. 28
  3.1 Overview ....................................................................................... 28
  3.2 Delay-Locked Loop ...................................................................... 31
    3.2.1 Voltage-Controlled Delay Line ............................................. 31
    3.2.2 Phase Detector ...................................................................... 32
    3.2.3 Charge Pump and Loop Filter .............................................. 34
    PD/CP/LF Transfer Function .......................................................... 36
    3.2.4 DLL with Actual LF Implementation ..................................... 37
    3.2.5 DLL locking .......................................................................... 38

Chapter 4 Circuit Implementation .......................................................... 40
  4.1 Overview ....................................................................................... 40
  4.2 Core Design ................................................................................... 40
    4.2.1 Delay Cell ............................................................................. 40
    4.2.2 True Single-Phase Clock Register ........................................ 42
    4.2.3 Static Register ....................................................................... 43
    4.2.4 Core Layout .......................................................................... 46
  4.3 Phase Detector ............................................................................... 47
  4.4 Charge Pump and Loop Filter ....................................................... 50
    4.4.1 Charge Pump ........................................................................ 50
    4.4.2 Loop Filter ............................................................................ 53
  4.5 Wallace-Tree Encoder Circuit ......................................................... 56
LIST OF TABLES

3.1 CP operation states ................................................................. 35
4.1 Delay Stage Sizing ................................................................. 41
4.2 TSPC Register Sizing ............................................................. 43
4.3 CP Transistor Sizing ............................................................... 51
4.4 Loop Filter Resistance Value .................................................... 53
4.5 Switch Sizing ........................................................................... 54
5.1 Simulated static nonlinearities .................................................... 67
5.2 Measured static nonlinearities ..................................................... 68
5.3 Power Consumption, circuit inputs active .................................... 70
5.4 Power Consumption, circuit inputs inactive ............................... 71
5.5 Simulated static linearties, Fractional $N_o=0.32$ ....................... 72
5.6 Measured static linearties, Fractional $N_o=0.32$ ....................... 72
5.7 Simulated static linearties, Fractional $N_o=0.69$ ....................... 72
5.8 Measured static linearties, Fractional $N_o=0.69$ ....................... 73
5.9 Simulated static linearties, Fractional $N_o=0.81$ ....................... 73
5.10 Measured static linearties, Fractional $N_o=0.81$ ...................... 73
5.11 $N_{linear}$ and FoM ................................................................. 76
5.12 Performance summary and comparison .................................... 77
LIST OF FIGURES

1.1 Basic delay-line TDC .................................................. 3
1.2 Vernier delay-line TDC ............................................... 4
1.3 1-bit TDC ............................................................... 5
1.4 Latch-based stochastic TDC .......................................... 6
1.5 VDL stochastic TDC .................................................. 7
1.6 Delay-line stochastic TDC ........................................... 8
1.7 Delay-line stochastic TDC ........................................... 9
1.8 Delay-line stochastic TDC ........................................... 10
1.9 Delay-line stochastic TDC ........................................... 11
1.10 Delay-line stochastic TDC .......................................... 12
1.11 Delay-line stochastic TDC .......................................... 13
1.12 Delay-line stochastic TDC .......................................... 14
1.13 Delay-line stochastic TDC .......................................... 15
1.14 Delay-line stochastic TDC .......................................... 16
1.15 Delay-line stochastic TDC .......................................... 17
1.16 Delay-line stochastic TDC .......................................... 18
1.17 Delay-line stochastic TDC .......................................... 19
1.18 Delay-line stochastic TDC .......................................... 20
1.19 Delay-line stochastic TDC .......................................... 21
1.20 Delay-line stochastic TDC .......................................... 22
1.21 Delay-line stochastic TDC .......................................... 23
1.22 Delay-line stochastic TDC .......................................... 24
1.23 Delay-line stochastic TDC .......................................... 25
1.24 Delay-line stochastic TDC .......................................... 26
1.25 Delay-line stochastic TDC .......................................... 27
1.26 Delay-line stochastic TDC .......................................... 28
1.27 Delay-line stochastic TDC .......................................... 29
1.28 Delay-line stochastic TDC .......................................... 30
1.29 Delay-line stochastic TDC .......................................... 31
1.30 Delay-line stochastic TDC .......................................... 32
1.31 Delay-line stochastic TDC .......................................... 33
1.32 Delay-line stochastic TDC .......................................... 34
1.33 Delay-line stochastic TDC .......................................... 35
1.34 Delay-line stochastic TDC .......................................... 36
1.35 Delay-line stochastic TDC .......................................... 37
1.36 Delay-line stochastic TDC .......................................... 38
1.37 Delay-line stochastic TDC .......................................... 39
1.38 Delay-line stochastic TDC .......................................... 40
1.39 Delay-line stochastic TDC .......................................... 41
1.40 Delay-line stochastic TDC .......................................... 42
1.41 Delay-line stochastic TDC .......................................... 43
1.42 Delay-line stochastic TDC .......................................... 44
1.43 Delay-line stochastic TDC .......................................... 45
1.44 Delay-line stochastic TDC .......................................... 46
1.45 Delay-line stochastic TDC .......................................... 47
1.46 Delay-line stochastic TDC .......................................... 48
1.47 Delay-line stochastic TDC .......................................... 49
1.48 Delay-line stochastic TDC .......................................... 50
1.49 Delay-line stochastic TDC .......................................... 51
1.50 Delay-line stochastic TDC .......................................... 52
1.51 Delay-line stochastic TDC .......................................... 53
1.52 Delay-line stochastic TDC .......................................... 54
1.53 Delay-line stochastic TDC .......................................... 55
1.54 Delay-line stochastic TDC .......................................... 56
1.55 Delay-line stochastic TDC .......................................... 57
1.56 Delay-line stochastic TDC .......................................... 58
1.57 Delay-line stochastic TDC .......................................... 59
1.58 Delay-line stochastic TDC .......................................... 60
1.59 Delay-line stochastic TDC .......................................... 61
1.60 Delay-line stochastic TDC .......................................... 62
1.61 Delay-line stochastic TDC .......................................... 63
1.62 Delay-line stochastic TDC .......................................... 64
1.63 Delay-line stochastic TDC .......................................... 65
1.64 Delay-line stochastic TDC .......................................... 66
1.65 Delay-line stochastic TDC .......................................... 67
1.66 Delay-line stochastic TDC .......................................... 68
1.67 Delay-line stochastic TDC .......................................... 69
1.68 Delay-line stochastic TDC .......................................... 70
1.69 Delay-line stochastic TDC .......................................... 71
1.70 Delay-line stochastic TDC .......................................... 72
1.71 Delay-line stochastic TDC .......................................... 73
1.72 Delay-line stochastic TDC .......................................... 74
1.73 Delay-line stochastic TDC .......................................... 75
1.74 Delay-line stochastic TDC .......................................... 76
1.75 Delay-line stochastic TDC .......................................... 77
1.76 Delay-line stochastic TDC .......................................... 78
1.77 Delay-line stochastic TDC .......................................... 79
1.78 Delay-line stochastic TDC .......................................... 80
1.79 Delay-line stochastic TDC .......................................... 81
1.80 Delay-line stochastic TDC .......................................... 82
1.81 Delay-line stochastic TDC .......................................... 83
1.82 Delay-line stochastic TDC .......................................... 84
1.83 Delay-line stochastic TDC .......................................... 85
1.84 Delay-line stochastic TDC .......................................... 86
1.85 Delay-line stochastic TDC .......................................... 87
1.86 Delay-line stochastic TDC .......................................... 88
1.87 Delay-line stochastic TDC .......................................... 89
1.88 Delay-line stochastic TDC .......................................... 90
1.89 Delay-line stochastic TDC .......................................... 91
1.90 Delay-line stochastic TDC .......................................... 92
1.91 Delay-line stochastic TDC .......................................... 93
1.92 Delay-line stochastic TDC .......................................... 94
1.93 Delay-line stochastic TDC .......................................... 95
1.94 Delay-line stochastic TDC .......................................... 96
1.95 Delay-line stochastic TDC .......................................... 97
1.96 Delay-line stochastic TDC .......................................... 98
1.97 Delay-line stochastic TDC .......................................... 99
1.98 Delay-line stochastic TDC ......................................... 100
1.99 Delay-line stochastic TDC ......................................... 101
2.1 Concept of wrap-around ............................................. 11
2.2 Single cycle helicoid .................................................. 12
2.3 Non-integer wrap-around helicoid ................................ 13
2.4 Non-integer wrap-around polar histogram view .......... 13
2.5 Non-integer wrap-around density distribution histogram 14
2.6 Non-integer wrap-around input-output characteristic .. 14
2.7 Non-integer wrap-around output code linearity .......... 15
2.8 Integer \( N \) helicoid graphical model ......................... 16
2.9 Integer \( N \) polar histogram view ................................. 16
2.10 Integer \( N \) density distribution histogram ................... 17
2.11 Integer wrap-around input-output characteristic ....... 17
2.12 Integer wrap-around output code linearity ................. 17
2.13 Non-integer \( N \) histogram without mismatch and jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 18
2.14 Non-integer \( N \) output code linearity without mismatch and jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 18
2.15 Integer \( N \) histogram without mismatch and jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 19
2.16 Integer \( N \) output code linearity without mismatch and jitter effect, \( V_{DD} = 27^\circ C \) 19
2.17 Non-integer \( N \) histogram with jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 20
2.18 Non-integer \( N \) output code linearity with jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 20
2.19 Integer \( N \) histogram with jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 21
2.20 Integer \( N \) output code linearity with jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 21
2.21 Non-integer \( N \) histogram with mismatch and jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 22
2.22 Non-integer \( N \) output code linearity showing mismatch and jitter effect \( V_{DD} = 1.8V,T = 27^\circ C \) 22
2.23 Integer \( N \) histogram with mismatch and jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 23
2.24 Integer \( N \) output code linearity showing mismatch and jitter effect, \( V_{DD} = 1.8V,T = 27^\circ C \) 23
2.25 Non-integer \( N \) histogram \( V_{DD} = 1.98V,T = 27^\circ C \) 24
2.26 Non-integer \( N \) output code linearity \( V_{DD} = 1.98V,T = 27^\circ C \) 24
2.27 Non-integer \( N \) histogram \( V_{DD} = 1.62V,T = 27^\circ C \) 25
2.28 Non-integer \( N \) output code linearity \( V_{DD} = 1.62V,T = 27^\circ C \) 25
2.29 Non-integer \( N \) histogram, \( V_{DD} = 1.8V,T = -10^\circ C \) 26
2.30 Non-integer \( N \) output code linearity \( V_{DD} = 1.8V,T = -10^\circ C \) 26
2.31 Non-integer \( N \) histogram, \( V_{DD} = 1.8V,T = 60^\circ C \) 27
2.32 Non-integer \( N \) output code linearity \( V_{DD} = 1.8V,T = 60^\circ C \) 27
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Stochastic TDC</td>
<td>29</td>
</tr>
<tr>
<td>3.2</td>
<td>TDC timing diagram</td>
<td>30</td>
</tr>
<tr>
<td>3.3</td>
<td>Output clock phases of an inverter based delay-line</td>
<td>31</td>
</tr>
<tr>
<td>3.4</td>
<td>Delay vs control voltage transfer characteristic</td>
<td>32</td>
</tr>
<tr>
<td>3.5</td>
<td>PD outputs behavior when (a) A leading B (b) B leading A</td>
<td>33</td>
</tr>
<tr>
<td>3.6</td>
<td>PD outputs behavior when (a) A out of phase with B (b) B out of phase with A</td>
<td>33</td>
</tr>
<tr>
<td>3.7</td>
<td>PD with charge pump and loop filter</td>
<td>34</td>
</tr>
<tr>
<td>3.8</td>
<td>$V_{ctrl}$ behavior when (a) A leading B (b) B leading A</td>
<td>35</td>
</tr>
<tr>
<td>3.9</td>
<td>Delay-Locked Loop</td>
<td>37</td>
</tr>
<tr>
<td>3.10</td>
<td>$\Delta T$ vs $V_{ctrl}$ Relationship</td>
<td>39</td>
</tr>
<tr>
<td>3.11</td>
<td>Simulated DLL Locking points</td>
<td>39</td>
</tr>
<tr>
<td>4.1</td>
<td>Current-Starved Inverter Schematic</td>
<td>40</td>
</tr>
<tr>
<td>4.2</td>
<td>Current-Starved Inverter Layout</td>
<td>41</td>
</tr>
<tr>
<td>4.3</td>
<td>Positive edge-triggered TSPC Register with reset Schematic</td>
<td>42</td>
</tr>
<tr>
<td>4.4</td>
<td>TSPC Register Schematic</td>
<td>43</td>
</tr>
<tr>
<td>4.5</td>
<td>Static register design</td>
<td>44</td>
</tr>
<tr>
<td>4.6</td>
<td>Implementation of the shift register</td>
<td>44</td>
</tr>
<tr>
<td>4.7</td>
<td>Static register schematic</td>
<td>45</td>
</tr>
<tr>
<td>4.8</td>
<td>Static register layout</td>
<td>46</td>
</tr>
<tr>
<td>4.9</td>
<td>One slice of TDC</td>
<td>47</td>
</tr>
<tr>
<td>4.10</td>
<td>Core Layout</td>
<td>47</td>
</tr>
<tr>
<td>4.11</td>
<td>Implementation of PD</td>
<td>48</td>
</tr>
<tr>
<td>4.12</td>
<td>Implementation of D flipflop</td>
<td>49</td>
</tr>
<tr>
<td>4.13</td>
<td>PD Layout</td>
<td>49</td>
</tr>
<tr>
<td>4.14</td>
<td>CP schematic</td>
<td>50</td>
</tr>
<tr>
<td>4.15</td>
<td>CP Layout</td>
<td>52</td>
</tr>
<tr>
<td>4.16</td>
<td>LF schematic</td>
<td>53</td>
</tr>
<tr>
<td>4.17</td>
<td>Switch Schematic</td>
<td>54</td>
</tr>
<tr>
<td>4.18</td>
<td>Switch Layout</td>
<td>54</td>
</tr>
<tr>
<td>4.19</td>
<td>Loopfilter Layout</td>
<td>55</td>
</tr>
<tr>
<td>4.20</td>
<td>7x3 Wallace-Tree encoder</td>
<td>56</td>
</tr>
<tr>
<td>4.21</td>
<td>31x5 sub-section of the Wallace-tree encoder</td>
<td>58</td>
</tr>
<tr>
<td>5.1</td>
<td>Microphotograph of the chip</td>
<td>59</td>
</tr>
<tr>
<td>5.2</td>
<td>Testbench setup block biagram</td>
<td>60</td>
</tr>
<tr>
<td>5.3</td>
<td>Custom PCB top layer</td>
<td>61</td>
</tr>
<tr>
<td>5.4</td>
<td>Custom PCB bottom layer</td>
<td>61</td>
</tr>
<tr>
<td>5.5</td>
<td>PCB with external connections</td>
<td>62</td>
</tr>
<tr>
<td>5.6</td>
<td>Complete Testbench</td>
<td>63</td>
</tr>
<tr>
<td>5.7</td>
<td>Filter network</td>
<td>63</td>
</tr>
<tr>
<td>5.8</td>
<td>TDC in oven to test at 60°C</td>
<td>64</td>
</tr>
<tr>
<td>5.9</td>
<td>TDC in freezer to test at -10°C</td>
<td>65</td>
</tr>
<tr>
<td>5.10</td>
<td>8-bit Stochastic TDC transfer characteristic</td>
<td>66</td>
</tr>
<tr>
<td>5.11</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.8 V, T = 27^\circ C$</td>
<td>68</td>
</tr>
<tr>
<td>Section</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>5.12</td>
<td>Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>5.13</td>
<td>Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>5.14</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>5.15</td>
<td>Measured DNL, $V_{DD} = 1.8V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>5.16</td>
<td>Measured INL, $V_{DD} = 1.8V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>5.17</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$</td>
<td></td>
</tr>
<tr>
<td>5.18</td>
<td>Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$</td>
<td></td>
</tr>
<tr>
<td>5.19</td>
<td>Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$</td>
<td></td>
</tr>
<tr>
<td>5.20</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$</td>
<td></td>
</tr>
<tr>
<td>5.21</td>
<td>Measured DNL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$</td>
<td></td>
</tr>
<tr>
<td>5.22</td>
<td>Measured INL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$</td>
<td></td>
</tr>
<tr>
<td>B.1</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.2</td>
<td>Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.3</td>
<td>Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.4</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.5</td>
<td>Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.6</td>
<td>Measured INL, $V_{DD} = 1.62V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.7</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.8</td>
<td>Simulated DNL, $V_{DD} = 1.98V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.9</td>
<td>Simulated INL, $V_{DD} = 1.98V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.10</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.11</td>
<td>Measured DNL, $V_{DD} = 1.98V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.12</td>
<td>Measured INL, $V_{DD} = 1.98V, T = 27^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.13</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 10^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.14</td>
<td>Simulated DNL, $V_{DD} = 1.8V, T = 10^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.15</td>
<td>Simulated INL, $V_{DD} = 1.8V, T = 10^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.16</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 10^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.17</td>
<td>Measured DNL, $V_{DD} = 1.8V, T = 10^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.18</td>
<td>Measured INL, $V_{DD} = 1.8V, T = 10^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.19</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.20</td>
<td>Simulated DNL, $V_{DD} = 1.8V, T = 60^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.21</td>
<td>Simulated INL, $V_{DD} = 1.8V, T = 60^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.22</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.23</td>
<td>Measured DNL, $V_{DD} = 1.8V, T = 60^\circ C$</td>
<td></td>
</tr>
<tr>
<td>B.24</td>
<td>Measured INL, $V_{DD} = 1.8V, T = 60^\circ C$</td>
<td></td>
</tr>
<tr>
<td>C.1</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.32, N_{act}=0.57$</td>
<td></td>
</tr>
<tr>
<td>C.2</td>
<td>Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.32, N_{act}=0.57$</td>
<td></td>
</tr>
<tr>
<td>C.3</td>
<td>Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.32, N_{act}=0.57$</td>
<td></td>
</tr>
<tr>
<td>C.4</td>
<td>Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.32, N_{act}=0.57$</td>
<td></td>
</tr>
<tr>
<td>C.5</td>
<td>Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.32, N_{act}=0.57$</td>
<td></td>
</tr>
<tr>
<td>C.6</td>
<td>Measured INL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.32, N_{act}=0.57$</td>
<td></td>
</tr>
<tr>
<td>C.7</td>
<td>Simulated Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62$</td>
<td></td>
</tr>
<tr>
<td>C.8</td>
<td>Simulated DNL, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62$</td>
<td></td>
</tr>
</tbody>
</table>
C.9 Simulated INL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62 \) 
C.10 Measured Transfer Characteristic, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62 \) 
C.11 Measured DNL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62 \) 
C.12 Measured INL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62 \) 
C.13 Simulated Transfer Characteristic, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35 \) 
C.14 Simulated DNL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35 \) 
C.15 Simulated INL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35 \) 
C.16 Measured Transfer Characteristic, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35 \) 
C.17 Measured DNL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35 \) 
C.18 Measured INL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35 \) 
C.19 Simulated Transfer Characteristic, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34 \) 
C.20 Simulated DNL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34 \) 
C.21 Simulated INL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34 \) 
C.22 Measured Transfer Characteristic, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34 \) 
C.23 Measured DNL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34 \) 
C.24 Measured INL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34 \) 
C.25 Simulated Transfer Characteristic, \( V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69, N_{act}=0.69 \) 
C.26 Simulated DNL, \( V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69, N_{act}=0.69 \) 
C.27 Simulated INL, \( V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69, N_{act}=0.69 \) 
C.28 Measured Transfer Characteristic, \( V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69, N_{act}=0.69 \) 
C.29 Measured DNL, \( V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69, N_{act}=0.69 \) 
C.30 Measured INL, \( V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69, N_{act}=0.69 \) 
C.31 Simulated Transfer Characteristic, \( V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89 \) 
C.32 Simulated DNL, \( V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89 \) 
C.33 Simulated INL, \( V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89 \) 
C.34 Measured Transfer Characteristic, \( V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89 \) 
C.35 Measured DNL, \( V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89 \) 
C.36 Measured INL, \( V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89 \) 
C.37 Simulated Transfer Characteristic, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}106 \) 
C.38 Simulated DNL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}106 \) 
C.39 Simulated INL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}107 \) 
C.40 Measured Transfer Characteristic, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}107 \) 
C.41 Measured DNL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}107 \) 
C.42 Measured INL, \( V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}108 \) 
C.43 Simulated Transfer Characteristic, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714 \) 
C.44 Simulated DNL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714 \) 
C.45 Simulated INL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714 \) 
C.46 Measured Transfer Characteristic, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714 \) 
C.47 Measured DNL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714 \) 
C.48 Measured INL, \( V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714 \) 
C.49 Simulated Transfer Characteristic, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70 \) 
C.50 Simulated DNL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70 \) 
C.51 Simulated INL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70 \) 
C.52 Measured Transfer Characteristic, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70 \) 
C.53 Measured DNL, \( V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70 \)
| C.54 | Measured INL, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.69$, $N_{act}=0.70$ | 112 |
| C.55 | Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.81$ | 112 |
| C.56 | Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.81$ | 112 |
| C.57 | Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.81$ | 113 |
| C.58 | Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.81$ | 113 |
| C.59 | Measured DNL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.81$ | 113 |
| C.60 | Measured INL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.81$ | 114 |
| C.61 | Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$ | 114 |
| C.62 | Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$ | 114 |
| C.63 | Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$ | 115 |
| C.64 | Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$ | 115 |
| C.65 | Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$ | 115 |
| C.66 | Measured INL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$ | 116 |
| C.67 | Simulated Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$ | 116 |
| C.68 | Simulated DNL, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$ | 116 |
| C.69 | Simulated INL, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$ | 117 |
| C.70 | Measured Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$ | 117 |
| C.71 | Measured DNL, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$ | 117 |
| C.72 | Measured INL, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$ | 118 |
| C.73 | Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.81$, $N_{act}=0.84$ | 118 |
| C.74 | Simulated DNL, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.81$, $N_{act}=0.84$ | 118 |
| C.75 | Simulated INL, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.81$, $N_{act}=0.84$ | 119 |
| C.76 | Measured Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.81$, $N_{act}=0.84$ | 119 |
| C.77 | Measured DNL, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.81$, $N_{act}=0.84$ | 119 |
| C.78 | Measured INL, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.81$, $N_{act}=0.84$ | 120 |
| C.79 | Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.81$, $N_{act}=0.82$ | 120 |
| C.80 | Simulated DNL, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.81$, $N_{act}=0.82$ | 120 |
| C.81 | Simulated INL, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.81$, $N_{act}=0.82$ | 121 |
| C.82 | Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.81$, $N_{act}=0.82$ | 121 |
| C.83 | Measured DNL, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.81$, $N_{act}=0.82$ | 121 |
| C.84 | Measured INL, $V_{DD} = 1.8V, T = 60^\circ C$, $N_o=0.81$, $N_{act}=0.82$ | 122 |
CHAPTER 1. INTRODUCTION

1.1 Motivation

Advanced driver-assistance systems (ADAS) and autonomous vehicles (AVs) promise to revolutionize transportation and society. Various sensor modalities are being actively investigated to provide spatial awareness to the vehicle, including cameras and radars. While cameras offer high-definition and textual data, the image processing is highly complex and challenging. Radars detect position and speed without the need of complex signal processing, but suffer from poor angular resolution [1]. Light-detection-and-ranging (LIDAR) is yet another sensing modality that [2] [3] measures the time-of-flight (ToF) of laser pulses to provide highly accurate distance and angular measurements, and requires relatively simple signal processing. However, LIDARs cannot operate in inclement weather such as rain and snow. Therefore, a sensor fusion consisting of two or more modalities is likely necessary to realize robust sensing systems for ADAS and AVs.

This thesis focuses on the time-to-digital converter (TDC) that is responsible for highly precise measurements of the time-of-flight in LIDARs. In particular, the thesis investigates the hitherto unaddressed error mechanisms affecting the linearity and robustness of the "stochastic" TDC and develops a rigorous theory describing the errors. Based on the results of the study, the thesis proposes a solution utilizing the delay-locked loop (DLL) in the TDC to improve the linearity and tolerate process, voltage and temperature (PVT) variations. A TDC fabricated in the 180-nm CMOS process employing the proposed technique demonstrates the effectiveness of the proposed solution and verifies the error theory. Operating at a sampling rate of 60 MHz, the TDC achieves 65 ps of time resolution, 16 ns of range, and 2.1 least-significant bits (LSBs) of integral nonlinearity (INL) while consuming 25 mW. The INL remains within 2 LSBs across −10°C to 60°C and supply variations of ±10%. 
When the DLL is turned off, the INL degrades to 5.87 LSBs across the same variations, validating the analysis and the effectiveness of the proposed technique.

1.2 Prior Work

Time-to-digital converters (TDC) are widely employed within various industrial, automotive and biomedical applications. TDCs were originally developed for applications such as laser range finders [4] [5], ToF particle detectors, and timing jitter measurement [6] [7]. They were then used in measurement instruments such as oscilloscopes and logic analyzers and in other fields such as positron emission tomography (PET) [8], telecommunications and frequency synthesis such as FM and PM modulators [9].

Various TDC architectures were developed over time with the task of quantizing a time interval bounded by the start and stop signals, and producing a digital output that represents the time duration between the two. TDCs can be classified into direct and indirect conversion techniques. Indirect or two-step conversion schemes were developed by mapping time-to-analog then converting analog-to-digital. Examples of this type are ramp TDCs [10], dual-slope TDCs [11] and time-amplifier (TA)-based TDCs [12]. In two-step schemes such as TA-based TDCs; the time difference between the inputs is amplified by a certain gain then digitized by a conventional flash TDC. The error introduced from the analog-to-time step due to non-linearity of the capacitors, leakage current in dual-slope TDC, and gain inaccuracy in TA based TDC present a disadvantage for the indirect conversion methods [13]. Another disadvantage of indirect conversion circuit is its sensitivity to PVT variations, making it incompatible for applications that require stability over these parameters such as in automotive applications.

The simplest way of implementing a direct TDC is by counting the number of reference clock cycles in the measurement interval. However, to achieve a higher resolution, the reference clock can be divided into smaller intervals using a delay line (DL), which can be made up of inverters or buffers as shown in Fig. 1.1. Unfortunately, the time resolution
is still limited to the propagation delay of a single delay stage for a given CMOS process. To achieve a finer time resolution, the vernier delay line (VDL) topology can be adopted, as shown in Fig. 1.2. The upper delay line propagation delay, $t_{d1}$, and the lower delay line propagation delay, $t_{d2}$, are slightly different, thus the resolution is determined by the time difference between two delays, $t_R = (t_{d1} - t_{d2})$. For example, if $t_{d1} = 50$ ps and $t_{d2} = 40$ ps, the TDC achieves a resolution of 10 ps, which is smaller than $t_d$ of a single stage. Despite the popularity of VDL and its ability to achieve sub-gate resolution, it suffers from sensitivity to PVT variations, low conversion rate, and large chip area [14]. Other VDL-TDC techniques were developed to achieve higher resolutions with fewer number of gates such as 2D-VDL [15], 3D-VDL [16], Vernier-ring [17], Vernier-GRO [18], and cyclic vernier delay lines [19]. However, these techniques increase complexity, often require calibration, and suffer from PVT sensitivity.

Figure 1.1: Basic delay-line TDC
To overcome the PVT sensitivity in DL and VDL techniques, one popular approach uses a DLL or a Phase-Locked Loop (PLL) in feedback to stabilize the propagation delay in a DL against PVT variations [20]. In [21], two VDLs were implemented with one of them calibrated against accuracy problems caused by PVT variations using a DLL and the other externally biased. Enabling the DLL to operate continuously improved the overall accuracy to ±1 LSB for resolutions down to 60 ps while the VDL with external biasing can achieve a time resolution as high as 5 ps with the accuracy limited by the systematic nonlinearity and random error due to time jitter. However, the chip size increased to 10 mm$^2$ in 0.7 µm CMOS process. It also has to be noted that error in performance characteristics such as resolution, conversion time, dynamic range, integral nonlinearity (INL) and differential nonlinearity (DNL) may appear due to mismatch between VDLs due to coupling between signals [13].

Chen et.al. [22] proposed a PVT-insensitive Vernier-based dual PLL architecture with triggerable voltage controlled oscillator in order to eliminate mismatch effect. The perfor-
mance metrics for this design were reported for a short and long readout interval, for the short readout interval the INL and DNL are within \( \pm 0.5 \) LSB for a 5-bit output. The design suffers from a high power consumption of 150 mW and a low output resolution.

1.2.1 Stochastic TDCs

Stochastic TDCs exploit the stochastic properties of a set of stages such as mismatch and jitter. Stochastic TDCs are introduced due to their implementation simplicity, extension of dynamic range and the possibility of achieving higher resolution. The penalty is larger area and higher power consumption depending on the number of stages and frequency of operation.

In [23] and [24], a stochastic TDC composed of arbiters or latches was introduced as a part of a digital PLL design. A single latch acts as a 1-bit TDC comparing two inputs, if input 1 crosses the voltage threshold \( V_{TH} \) (corresponds \( t_{TH} \) on the time axis) of the latch before input 2 the latch produces "+1", otherwise the output is "-1", as shown in Fig. 1.3. Therefore, an N-bit TDC could be created by using a set of latches and summing their outputs to evaluate the phase difference between two inputs in parallel, as shown in Fig. 1.4.

![Figure 1.3: 1-bit TDC](image)

Latches in an N-bit latch-based TDC have different input voltage offsets \( V_{OS} \) due to process variations. Thus, each latch has a different \( V_{TH} \). Assuming all latches are identical, the cumulative summation of all offset voltages has a normal or Gaussian distribution with a
The resolution mean could be expressed by \( \text{LSB} = \sqrt{\frac{2\pi \times \sigma_T}{2^N - 1}} \), where the denominator is the number of latches. The resolution could be changed by truncating the digital output of the TDC or by controlling the latch voltage offset. This also affects the conversion range of the TDC.

![Figure 1.4: Latch-based stochastic TDC](image)

The latch was implemented using set-reset flip-flops based on cross-coupled NAND gates followed by a D flip-flop to hold the data. Unfortunately, this stochastic architecture is vulnerable against PVT variations and requires calibration.

A stochastic TDC architecture with self-calibration is introduced in [25]. The TDC is composed of a monotonic encoder circuit, a linearity improving self-calibration circuit and a self-testing circuit. This stochastic approach is based on the VDL architecture that utilizes two ring oscillators. The outputs from the upper ring and lower ring are connected to the data input and clock of the flip-flops, respectively (Fig. 1.5). For each output, multiple flip-flops are connected in parallel. The design is based on VDL architecture with plurality D flip-flops which exhibit process mismatch variations. Therefore, the time threshold that determines the edge transition from 0 to 1 and from 1 to 0 differs between flip-flops. This stochastic implementation depends on the set-up and hold times to determine the resolution.
of the TDC. A drawback in this architecture is that the output code might be highly non-linear and requires external self-calibration to improve its linearity.

Figure 1.5: VDL stochastic TDC

This thesis focuses on the stochastic delay line TDC architecture first introduced in [20] (Fig. 1.6). This TDC architecture employs an extremely long delay line to generate a large number of clock phases. The random mismatch and jitter spreads the clock edges uniformly in time. AND gates and latches count the number edges that occur between the start and stop signals. The latch outputs are then encoded to a binary code using a Wallace-tree adder. PVT variations change the unit delay of the delay chain but not the distribution of the edges. Therefore, this architecture is immune to PVT variations.
While the stochastic delay-line TDC has demonstrated excellent PVT tolerance and it is fully digital synthesizable, it requires an extremely long delay line ($2^{14}$ units) to produce a 10-bit output. As explained in this prior work, the reason for the long delay line is to allow the truncation of the Wallace-tree output (from 14 bits to 10 bits) to smooth out irregularities, but this was stated without rigorous theoretical analysis.

This thesis explores the intriguing issue of the need for an extremely long delay line in a stochastic delay-line TDC first reported in [20], formulates a rigorous theory on the edge distribution and its effect on the TDC linearity, proposes a DLL-based solution to improve the linearity and to relax the requirement on the length of the delay line, and demonstrates the validity of the new theory and the effectiveness of the proposed technique in actual silicon.

![Figure 1.6: Delay-line stochastic TDC](image-url)
1.3 Outline

This thesis is organized as follows: Chapter 2 presents TDC analysis. Chapter 3 presents the TDC architecture. Chapter 4 explains the circuit implementation. Chapter 5 shows the experimental results, Chapter 6 lists my thesis contributions, summarizes this work and proposes future work.
CHAPTER 2. TDC ANALYSIS

2.1 Problem of Non-Integer Wrap-Around

The stochastic TDC utilizes distributed edges to quantize the input. However, as will be shown shortly, the TDC must meet certain conditions imposed by the clock period, unit delay, and number of delays for the edges to be uniformly distributed over the sampling period, i.e. a systematic TDC nonlinearity results if these conditions are violated. This fundamental design consideration evidently has not been recognized and analyzed in prior work [20].

Consider a delay chain of \( m \) elements and a unit delay of \( t_d \). The clock injects a new edge every \( T_{CK} \) seconds and each clock edge propagates through the entire delay chain in \( m \times t_d \) seconds. The maximum input amplitude is bounded by the clock period \( T_{CK} \) because all taps of the chain will have experienced one clock transition on average in \( T_{CK} \), i.e. the maximum sampling period is \( T_{CK} \). Focusing on a single clock edge, it can be observed that the edge traverses through multiple \( T_{CK} \) periods for \( m \times t_d > T_{CK} \). In other words, each \( T_{CK} \) period sees multiple traversals by different clock edges. This phenomenon can also be equivalently viewed as an edge traversing through a \( T_{CK} \) period and "wrapping around" the period when the edge reaches the end of the period (in reality, the next traversal is created by the next clock edge, but the two views are equivalent). An example of a delay chain demonstrating the warp-around in \( T_{CK} \) is shown in Fig. 2.1.
Figure 2.1: Concept of wrap-around
A polar plot of the edge traversing through the period can provide important additional insight. Plotting an edge’s phase, defined as $t_d/(2\pi T_{CK})$, in the xy-plane and time in the z-axis, a traversing edge draws a surface in the shape of a helicoid (Fig. 2.2). Utilizing the wrap-around property, the edge repeats the helicoid every $T_{CK}$. The total length of the helicoid along the z-axis is precisely $m \times t_d$ (Fig. 2.3). The edge distribution density at any given phase in the sampling period can be found graphically by drawing a line parallel to the z-axis at a certain phase.

Figure 2.2: Single cycle helicoid

In this particular example, line $L_1$ intersects the helicoid surface four times and $L_2$ five times. This indicates that the edge density is lower at the phase of $L_1$ than that at the phase of $L_2$. Fig. 2.4 shows the number of intersects throughout the entire sampling period. For phases greater than $\phi_1$ but less than $\phi_n$, the number of intersects is five, and four otherwise.
Figure 2.3: Non-integer wrap-around helicoid

Figure 2.4: Non-integer wrap-around polar histogram view
Fig. 2.4 can be equivalently drawn as a histogram (Fig. 2.5), where the bin count is higher between $\phi_n$ and $\phi_1$ and is lower between $\phi_1$ and $\phi_n$. This non-uniform edge distribution inevitably leads to TDC nonlinearity. Simulations show that a TDC with this histogram exhibits a 'kink' at the location where the edge density changes, producing a peak in the INL (Fig. 2.7).

Figure 2.5: Non-integer wrap-around density distribution histogram

Figure 2.6: Non-integer wrap-around input-output characteristic
2.2 Integer Wrap-Around

The foregoing analysis suggests that, in order to achieve a uniform edge distribution and thus good INL, $\phi_1$ must equal $\phi_n$. This is equivalent to the condition that $m \times t_d/T_{CK} = N$, $N \in I$, i.e. the total delay of the chain must be equal to an integer multiple of the clock period (the number of wrap arounds must be an integer). Since the clock period and the total delay are independent design variables, they must be carefully chosen to satisfy this condition. Furthermore, it is desirable to maintain this condition across variations such as process, supply voltage, and temperature. Depicted in Fig. 2.1, to have an integer number of wrap-arounds, the phase of the edge of the last tap must be exactly $2\pi$. Viewed in the polar domain, this is equivalent to having an integer number of turns in the helicoid (Fig. 2.8). The uniform edge distribution can be verified by drawing a line parallel to the z-axis and counting the number of intersects of the helicoid. In this particular example, a line at any phase intersects the helicoid exactly four times, indicating a uniform edge distribution (Fig. 2.9). Simulation verifies the uniformity of this example (Fig. 2.10), resulting in a ramp containing no kinks (Fig. 2.11) and good INL (Fig. 2.12). The above analysis assumes that the beginning of the sampling period (the reference phase) coincides with the edge of the first tap. But this condition is not necessary. It can be shown that the sampling period can begin at any time and all of the analysis still holds.
Figure 2.8: Integer $N$ helicoid graphical model

Figure 2.9: Integer $N$ polar histogram view
Figure 2.10: Integer $N$ density distribution histogram

Figure 2.11: Integer wrap-around input-output characteristic

Figure 2.12: Integer wrap-around output code linearity
2.3 Effect of Nonidealities

The effect of nonidealities on the TDC linearity for the integer and non-integer $N$ cases will now be examined. Nominal operating conditions for the proposed TDC design are set to a voltage supply of 1.8 V and room temperature of 27°C. Figs. 2.13 and 2.14 show the simulated output phases histograms and INL respectively, under nominal operating conditions and without jitter and delay mismatch.

Figure 2.13: Non-integer $N$ histogram without mismatch and jitter effect, $V_{DD} = 1.8V, T = 27°C$

Figure 2.14: Non-integer $N$ output code linearity without mismatch and jitter effect, $V_{DD} = 1.8V, T = 27°C$
The shown histograms are based on the actual $t_d$ values extracted from Cadence tools ($t_d = 283.1$ ps) and the length of the inverter chain is 1020. The clock frequency is set to 60 MHz, yielding an $N$ of 17.32. Fig. 2.13, shows that when the histogram changes experiences a density change the INL suffers a peak. Figs. 2.15 and 2.16 show the phase histogram and the INL, respectively, for a TDC with integer $N$ case.

Figure 2.15: Integer $N$ histogram without mismatch and jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$

Figure 2.16: Integer $N$ output code linearity without mismatch and jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$
2.3.1 Jitter

Random noise from the transistors changes the clock delay through each delay cell. This introduces jitter in the edges of the delay chain. To study the effect of jitter on the TDC’s linearity, the standard deviation of the jitter of a delay cell is extracted from transistor-level transient simulations ($0.5\% \times t_d$). Next, this jitter is added as a Gaussian noise to the nominal delay of each delay cell in the behavioral simulations. Figs. 2.17 and fig.2.18 show the output phases density distribution histogram and INL, respectively, for a TDC with a non-integer $N$ and jitter.

<table>
<thead>
<tr>
<th>Occurrences</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
</tr>
<tr>
<td>40</td>
</tr>
<tr>
<td>30</td>
</tr>
<tr>
<td>20</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

Figure 2.17: Non-integer $N$ histogram with jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$

<table>
<thead>
<tr>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>-1</td>
</tr>
<tr>
<td>-2</td>
</tr>
</tbody>
</table>

Figure 2.18: Non-integer $N$ output code linearity with jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$
Figs. 2.19 and 2.20 show the phase histogram and INL, respectively, for a TDC with an integer-$N$ and jitter. Comparing Figs. 2.17, 2.18 to Figs. 2.13, 2.14 and Figs. 2.19, 2.20 to Figs. 2.15, 2.16, it can be observed that jitter has a little effect on the linearity of the TDC.

![Figure 2.19: Integer $N$ histogram with jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$](image1)

![Figure 2.20: Integer $N$ output code linearity with jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$](image2)

### 2.3.2 Mismatch

The delay through each delay cell is not identical in an actual chip due to mismatch. This effect can be modeled by adding a normally distributed delay error to the nominal delay
for each delay cell. The delay error’s standard deviation is extracted from Monte Carlo simu-
lations. The mismatch ($\sigma=24.2$ ps) is added to the delay of each delay cell in the behavioral
simulations. Figs. 2.20 and 2.21 show the phase histogram and INL, respectively, for a TDC
with a non-integer $N$ and mismatch. Figs. 2.22 and 2.23 show the phase histogram and INL,
respectively, for a TDC with an integer-$N$ and mismatch. Comparing Figs. 2.21, 2.22 to
Figs. 2.13, 2.14 and Figs. 2.23, 2.24 to Figs. 2.15, 2.16, it can be observed that mismatch
lightly increased INL on the linearity of the TDC.

Figure 2.21: Non-integer $N$ histogram with mismatch and jitter effect, $V_{DD} = 1.8V, T = 27^\circ C$

Figure 2.22: Non-integer $N$ output code linearity showing mismatch and jitter effect $V_{DD} = 1.8V, T = 27^\circ C$
2.3.3 Supply Voltage Variation

To study the effect of the supply voltage variations on the linearity of the TDC, the nominal supply voltage (1.8 V) is varied by ±10% and the resulting phase histogram and INL simulated. The supply voltage systematically increases/decreases the nominal delay of the delay cell, thus changing the $N$. The $t_d$ values at ±10% of the nominal supply voltage are extracted from transistor-level simulations ($t_d = 283.4$ ps at +10% supply, $t_d = 298.6$ ps at -10% supply). No jitter or mismatch are included in the simulations. Figs. 2.25 and
2.26 show the phase histogram and INL, respectively, for a TDC with a non-integer $N$ and a 10% increase in the supply voltage.

![Phase Histogram and INL](image)

Figure 2.25: Non-integer $N$ histogram $V_{DD} = 1.98V, T = 27^\circ C$

![INL Graph](image)

Figure 2.26: Non-integer $N$ output code linearity $V_{DD} = 1.98V, T = 27^\circ C$

Figs. 2.27 and 2.28 show the phase histogram and INL, respectively, for a TDC with a non-integer $N$ and a 10% decrease in the supply voltage. Comparing Figs. 2.25 through 2.28 to Figs. 2.13, and 2.14, it can be observed that supply variation shifts the location of the histogram density jump, thus changing the location of the INL peak. The peak INL is little affected by the supply variations.
2.3.4 Temperature Variation

To study the effect of the temperature variations on the linearity of the TDC, the temperature is changed from 27°C to -10°C and 60°C and the resulting phase histogram and INL simulated. The temperature, similar to the supply voltage, systematically increases/decreases the nominal delay of the delay cell, thus changing the $N$. The $t_d$ values at -10°C and 60°C are extracted from transistor-level simulations ($t_d = 267.1$ ps at -10°C, $t_d = 299.7$ ps at 60°C). No jitter or mismatch are included in the simulations. Figs. 2.29 and 2.30 show the phase histogram and INL, respectively, for a TDC with a non-integer $N$ and at -10°C.
Figs. 2.31 and 2.32 show the phase histogram and INL, respectively, for a TDC with a non-integer $N$ at 60°C. Comparing Figs. 2.29 through 2.32 to Figs. 2.13, and 2.14, it can be observed that supply variation shifts the location of the histogram density jump, thus changing the location of the INL peak. The peak INL is little affected by the supply variations.
Figure 2.31: Non-integer $N$ histogram, $V_{DD} = 1.8V, T = 60^\circ C$

Figure 2.32: Non-integer $N$ output code linearity $V_{DD} = 1.8V, T = 60^\circ C$
CHAPTER 3. TDC ARCHITECTURE

3.1 Overview

The foregoing analysis suggests that, in order to achieve good linearity for a stochastic delay-line TDC, it is desirable to have an integer number (integer $N$) of wrap-arounds of the clock phase over the clock period. Furthermore, $N$ must kept constant over PVT variations for robust linearity performance. To guarantee an integer value for $N$ and subsequently maintain its value across PVT variations, this thesis proposes the use of a DLL in the TDC. The idea is to lock the phase of the first tap of the inverter to that of the last tap using negative feedback and dynamically maintain the lock across variations. In other words, the DLL ensures that $m \times t_d = N \times T_{CK}$, $N \in I$, where $m$ is the number of delay cells, $t_d$ the unit delay, and $T_{CK}$ the clock period. The DLL in the proposed TDC serves an entirely different purpose than those in conventional vernier delay-line TDCs. Whereas the former employs the DLL for a constant number of wrap-arounds, the latter uses the DLL to maintain a constant unit delay across PVT variations. Because jitter does not affect the linearity of the proposed TDC as shown in the previous chapter, the requirements of the proposed DLL is relaxed from those of the conventional vernier TDC, a point that will be discussed shortly.

A block diagram of the proposed TDC architecture is shown in Fig. 3.1. It consists of a delay-locked loop (DLL), true single-phase clock (TSPC) registers, static register and a synchronous encoder circuit. The DLL is comprised of a phase detector (PD), charge pump (CP), loop filter (LF) and voltage-controlled delay line (VCDL). The operation of the DLL is as follows: a reference input clock is applied to the delay line and to one of the inputs of the PD. The clock passes through the delay line and the last delay cell’s output is connected to the second input of the PD. The PD compares the two inputs and produces two pulses that represent the phase difference between the inputs. These pulses control switched current...
sources in the CP which charge or discharge the loop filter. The output voltage from the loop filter is $V_{ctrl}$ which is fed to the VCDL to adjust the delay until the input phase and the VCDL output phase align. This phase locking guarantees integer $N$ of the TDC.

![Figure 3.1: Stochastic TDC](image)

The operation of the TDC is as follows: After the DLL locks, each delay cell in the VCDL generates a clock signal $X$ to a TSPC register. If the clock $X$ transitions while the input $T_{IN}$ is high, a ‘1’ is registered. Since the edges of $X$ of the entire DLL are uniformly distributed in time, a large input, i.e. a longer $T_{IN}$ pulse, results in more ‘1’s’ registered. The number of ‘1’s’ registered is linearly proportional to the time that the input is high. In the limit when the logic high time of $T_{IN} = T_{CK}$, 1020 ‘1’s’ are registered on average, yielding the maximum output code. The TSPC registers’ outputs, $Y$, are stored by a second rank of static registers.

29
Figure 3.2: TDC timing diagram
Then, a reset pulse \( RST \) is asserted to reset the TSPC registers for the next sample cycle. The 1020 outputs, \( D \), are converted to a 10-bit binary code by means of a Wallace-tree encoder, which counts the number of ‘1’s’ in \( D \). The 10-bit output \( D_{\text{out}} \) is truncated to 8 bits to reduce differential nonlinearity (DNL) off-chip. Fig. 3.2 illustrates the timing diagram of the TDC.

### 3.2 Delay-Locked Loop

#### 3.2.1 Voltage-Controlled Delay Line

A VCDL consists of a chain of delay elements whose delay is controlled by a voltage. The circuit implementation will be discussed in the next chapter. Fig. 3.3 show a delay line with the tap waveforms. Denoting the high-to-low and low-to-high delays as \( t_{\text{dhl}} \) and \( t_{\text{dth}} \), respectively, the average delay \( t_d \) is defined as

\[
t_d = \frac{t_{\text{dhl}} + t_{\text{dth}}}{2}.
\]  

\( (3.1) \)

![Figure 3.3: Output clock phases of an inverter based delay-line](image-url)
Since $t_d$ of voltage-controlled delay element depends on the RC time constant. The delay of delay element can be capacitively-controlled or resistively-controlled. A capacitively-controlled VCDL is not feasible since it requires a larger area for a longer delay chain. Hence, a resistively-controlled VCDL would address the previously mentioned design issue (the design of an individual delay stage is discussed in detail in the next chapter). This $t_d$ value is used in the calculations in the previous chapter.

The relationship between $V_{ctrl}$ and $t_d$ for a single delay cell is simulated and shown in Fig. 3.4. The delay decreases as $V_{ctrl}$ is swept from 0 V to 1.8 V. When $V_{ctrl}$ is below 0.4 V the delay remains relatively constant and independent from $V_{ctrl}$. This region is known as the dead-band region [26]. The DLL is designed to operate in the operational region where the delay varies almost linearly with $V_{ctrl}$. The slope in this region is denoted by $K_{VCDL}$, a parameter that will be utilized to analyze the dynamics of the DLL in the next section.

![Figure 3.4: Delay vs control voltage transfer characteristic](image)

### 3.2.2 Phase Detector

A phase detector is a sequential logic circuit that compares the phase difference between two signals. The PD in the TDC detects the phase difference between the falling edges
of the two inputs. Inputs to the PD can be labeled by A and B and the outputs labeled by QA and QB, as shown in fig. 3.7. Fig. 3.5 illustrates the behavior of QA and QB in two cases: the phase of A leading that of B and vice versa. Fig. 3.6 illustrates the behavior of QA and QB when the input phases are nearly 180° apart. When A and B are not in phase, the PD generates an output that is proportional to the phase difference.

Figure 3.5: PD outputs behavior when (a) A leading B (b) B leading A

Figure 3.6: PD outputs behavior when (a) A out of phase with B (b) B out of phase with A
3.2.3 Charge Pump and Loop Filter

The CP consists of two switched current sources that converts the digital pulses into an analog current. The LF at its simple form can be considered to be just a capacitor that converts the analog current into voltage, as shown in Fig. 3.7. According to the phase difference between the PD inputs, the CP switches the current sources \( I_1 \) and \( I_2 \) thus charging and discharging the LF. The currents \( I_1 \) and \( I_2 \) are also known as UP and DOWN currents and are nominally equal [27].

![Figure 3.7: PD with charge pump and loop filter](image-url)
Table 3.1 summarizes the CP operation and its effect on $V_{ctrl}$ based on the CP inputs. In the case of $S_1$ and $S_2$ both closed, the current passes from the voltage supply to the ground thereby $V_{ctrl}$ doesn’t change.

Table 3.1: CP operation states

<table>
<thead>
<tr>
<th>QA</th>
<th>QB</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$V_{ctrl}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>On</td>
<td>On</td>
<td>No Change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>On</td>
<td>Off</td>
<td>Increase</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
<td>On</td>
<td>Decrease</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
<td>Off</td>
<td>No Change</td>
</tr>
</tbody>
</table>

To demonstrate the effect of the phase difference between the PD inputs on $V_{ctrl}$, two cases are shown in Fig. 3.8 where in the first case input A leads input B which showed an increase in $V_{ctrl}$ and vice versa when B leads A. The phase difference between the PD inputs is denoted by $\Delta T$. In the case of A leading B, $\Delta T$ is considered positive and when B is leading A, $\Delta T$ is considered to be negative.

(a) A leading B

(b) B leading A

Figure 3.8: $V_{ctrl}$ behavior when (a) A leading B (b) B leading A
PD/CP/LF Transfer Function

To approximate the relationship between $V_{ctrl}$ and the time difference $\Delta T$, some assumptions are taken into consideration: The clock period for both inputs is denoted by $T_{CK}$, $I_1$ and $I_2$ equal to $I_p$ and $\Delta T$ is positive (Fig 3.7).

Assuming that both PD inputs are in-phase starting at $t = 0$, a time difference step is applied between the two inputs given by $\Delta T = T_o \times u(t)$, thus QA and QB start producing pulses representing the abrupt change in phase which will start changing $V_{ctrl}$, using the following equation as a starting point which represent the change in voltage over change in time for a capacitor

\[
I_p = C_p \frac{dv}{dt}. \tag{3.2}
\]

Rearranging equation (3.2) to make the change in voltage $dv$ the variable of interest and by taking the integral for both sides between the time right before the applying phase step at lower limit of zero and till the time that represent the time difference at an upper limit of $(\Delta T \times t)/T_{CK}$ expressed by the following equation

\[
\int_0^{\Delta T \times t / T_{CK}} dv = \int_0^{\Delta T \times t / T_{CK}} \frac{I_p}{C_p} dt. \tag{3.3}
\]

Thereby the result of the integral on left-hand side of the equality is $V_{ctrl}$ as a function of time and can be expressed by the following equation

\[
V_{ctrl}(t) = \frac{I_p}{T_{CK} C_p} \times t \times \Delta T, \tag{3.4}
\]

assuming that $V_{ctrl}$ initial condition equals zero. Therefor, by moving $T_o \times t$ to the left-hand side and taking the Laplace Transform, a relationship between the change in voltage over the change in phase can be expressed by the following equation

\[
\frac{V_{ctrl}}{\Delta T}(s) = \frac{I_p}{T_{CK} C_p} \times \frac{1}{s}. \tag{3.5}
\]
3.2.4 DLL with Actual LF Implementation

Fig. 3.9 shows the DLL with the actual implementation of the LF. A resistor $R_p$ is added in series with capacitor $C_p$ which increases the voltage swing on $V_{ctrl}$ and sets a time constant for the charge and discharge of the LF. However, after the DLL locks the resistor still causes a periodic ripple of value $I_p R_p$ on the control voltage at the beginning of each PD pulse, where the ripple is proportional to the switching of the CP switches. This ripple introduces excessive jitter to the VCDL outputs. To protect $V_{ctrl}$ from any large ripples in voltage due to the mismatch between the two switched current source in the CP, another capacitor $C_2$ is added in parallel with $R_p$ and $C_p$. The capacitor $C_2$ softens the ripple on $V_{ctrl}$ and insures that the DLL locks and maintains lock [27].

![Figure 3.9: Delay-Locked Loop](image)

As previously discussed, The PD/CP/LF transfer functions was modeled in equation (3.5), and it can be rewritten taking into consideration the actual LF implementation as the following

$$\frac{V_{ctrl}(s)}{\Delta T(s)} = \frac{I_p}{T_{CK}} \frac{R_p C_p s + 1}{R_p C_p C_2 s^2 + s(C_p + C_2)}.$$ (3.6)
3.2.5 DLL locking

The PD capture range is between \((-T_{CK}/2, +T_{CK}/2\) time difference or within half clock period leading to half clock period lagging with respect to the reference clock. Thus, if \(\Delta T\) is within \(T_{CK}/2\) leading or lagging from the reference clock, then the PD/CP/LF combination will adjust the delay in the VCDL until \(\Delta T\) becomes zero. However, it is difficult to design a VCDL with an adjustable range exactly from \(-T_{CK}/2\) to \(+T_{CK}/2\) across PVT variations. If \(\Delta T\) is more than \(T_{CK}\) an issue of "false-locking" occurs such that the last stage output in the VCDL doesn’t align with the designated clock cycle in the reference clock. There can be several secondary locking points that repeat every \(T_{CK}\). Since the PD is periodic, if \(\Delta T\) is within \(T_{CK}/2\) from the any locking point, the PD/CP/LF adjust the delay in the VCDL until it locks to nearest locking point [26]. Therefore, in order for the DLL to lock to one clock cycle of the reference clock, the initial delay in the VCDL must be within \(0.5 \times T_{CK}\) to \(1.5 \times T_{CK}\), regardless of the initial value of \(V_{ctrl}\). The following inequality represents the condition for the DLL to lock without 'false-locking' assuming that the maximum and minimum delay in the VCDL are \(T_{VCDL_{\text{max}}}\) and \(T_{VCDL_{\text{min}}}\), respectively [28]. Fig. 3.10 illustrates the relationship between the \(\Delta T\) and \(V_{ctrl}\).

\[
\text{Max}(T_{VCDL_{\text{min}}}, \frac{2}{3} \times T_{VCDL_{\text{max}}}) < T_{CK} < \text{Min}(T_{VCDL_{\text{max}}}, 2 \times T_{VCDL_{\text{min}}}).
\]  \hspace{1cm} (3.7)

Multiple solutions were reported for the "false-locking" issue in [28], [29] and [30]. However, the ultimate application of the DLL in this data converter is to set the dynamic range of the VCDL to the input clock period \(T_{CK} = t_{DR}\), thus the time resolution \(t_{d}\) is set to \(T_{CK}/m\) where \(m\) is the number of delay stages. Therefore, the DLL provides an automatic calibration against PVT variations and stabilizes \(t_{d}\), thus the VCDL can give finer timing information [21]. The simulated locking points for the designed DLL under normal operating conditions in the effective range of \(V_{ctrl}\) is shown in Fig. 3.11. The designed DLL has six locking points within the effective range of \(V_{ctrl}\), as shown in Fig. 3.11 with comparison to Fig. 3.10.
Figure 3.10: $\Delta T$ vs $V_{ctrl}$ Relationship

Figure 3.11: Simulated DLL Locking points
CHAPTER 4. CIRCUIT IMPLEMENTATION

4.1 Overview

This chapter presents the schematics and layout of each part of the proposed design.

4.2 Core Design

4.2.1 Delay Cell

The delay cell is implemented by a current-starved inverter. The schematic of the current-starved inverter is shown in Fig. 4.1. The design shows two control voltages $V_{ctrl1}$ and $V_{ctrl2}$. $V_{ctrl1}$ is controlled by the DLL; $V_{ctrl2}$ is provided from an external voltage source set to 900 mV for debugging.

Equation (4.1) shows the on resistance of a MOSFET. According to this equation, by changing $V_{GS} - V_{TH}$ the on resistance of MOS transistor changes thus changing the delay.
\[ R_{DS(on)} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}. \] (4.1)

The delay chain consists of 1020 identical copies of the delay cell. Fig. 4.2 shows the layout. Table 4.1 summarizes the sizing of the transistors shown in Fig. 4.1. Minimum sizing was used to reduce area and power consumption.

<table>
<thead>
<tr>
<th>MOS Number</th>
<th>W((\mu m))</th>
<th>L((\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>0.22</td>
<td>0.18</td>
</tr>
<tr>
<td>M2,M3</td>
<td>0.22</td>
<td>0.18</td>
</tr>
<tr>
<td>M4</td>
<td>0.22</td>
<td>0.18</td>
</tr>
</tbody>
</table>

Figure 4.2: Current-Starved Inverter Layout
4.2.2 True Single-Phase Clock Register

Most common problems in CMOS circuits involves overlapping and skew between clock signals. Common clocking strategies include the clocked CMOS logic (C\(^2\)MOS) and the NORA dynamic CMOS technique. C\(^2\)MOS uses a nonoverlapping pseudo two-phase clock which results in four clock signals (four phases) distributed in the system with no overlapping between any two pair of clock signals. NORA dynamic CMOS uses two phases of one clock signal both inverted and non-inverted phases to avoid any race conditions due to clock skews. In terms of speed, NORA dynamic CMOS technique can perform at a higher speed than C\(^2\)MOS due to the reduction of the clock skew [31].

In order to reduce the number of transistors in the CMOS circuits and avoid clock skew, the true single-phase-clocking (TSPC) register is used [31]. Fig.4.3 shows the schematic of the TSPC. The register consists of three inverter stages and operates as follows: During the low phase of the clock, the input D is sampled to node X. Since CLK is low, \(M_6\) will charge node Y to \(V_{DD}\) while \(M_8\) and \(M_9\) are off. Therefore, the register holds the previous value of Q. On the rising edge of the clock, node X transitions according to D. The dynamic inverter \(M_4-M_6\) evaluates node X and discharges node Y if node X is high or charges node Y if node X is low. The third inverter \(M_7-M_9\) passes Y to the output Q.

![Figure 4.3: Positive edge-triggered TSPC Register with reset Schematic](image)

Figure 4.3: Positive edge-triggered TSPC Register with reset Schematic
The propagation delay of this register is three inverters since it takes one inverter delay for the input to affect node X, one inverter delay to affect node Y, one inverter delay to pass to Q on the rising edge of the clock [32]. Reset is introduced to this register to force an initial value of Q. In the case of high RST, node Y is discharged and node QB is charged, thus Q becomes logic low. The layout of a TSPC register with reset is shown in Fig. 4.4 and Table 4.2 summarizes the sizing of transistors.

![Figure 4.4: TSPC Register Layout](image)

<table>
<thead>
<tr>
<th>MOS Number</th>
<th>W(µm)</th>
<th>L(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M3</td>
<td>0.22</td>
<td>0.18</td>
</tr>
<tr>
<td>M4,M5</td>
<td>0.44</td>
<td>0.18</td>
</tr>
<tr>
<td>M6-M9</td>
<td>0.22</td>
<td>0.18</td>
</tr>
<tr>
<td>M10,M11</td>
<td>0.22</td>
<td>0.18</td>
</tr>
<tr>
<td>M12,M13</td>
<td>0.22</td>
<td>0.18</td>
</tr>
</tbody>
</table>

### 4.2.3 Static Register

As shown in Fig. 3.1, static registers follow the TSPC registers. The static register is implemented using master-slave scan flip-flops, thus allowing scan chain testing where the
register accepts input from off-chip. Fig. 4.5 shows the schematic of the register where the scan enable (SE) mux allows the register to accept data from a second input. The register clock can be provided either on-chip or off-chip.

A block diagram of the static register chained in a shift register configuration is shown in Fig. 4.6. The figure illustrates the internal routing where the output of each stage is fed to SI of the next stage and the same clock is provided to all flip-flops. This allows data to be written directly from off-chip to test the encoder circuit separately from the rest of the design.
The schematic of the static register is shown in Fig. 4.7. The register uses (SE) and its invertered form (SEB) to select between D or SI input. The invertered clock (CLKB) and its invertered form (CLKBB) are used in the transmission-gate and the tri-state inverter.

![Static register schematic](image)

**Figure 4.7: Static register schematic**

The operation of the register is as follows: When SE is high, $M_7$ and $M_2$ are off while $M_4$ and $M_9$ are on, thus passing SI at the falling transition of the clock. When SE is low, $M_7$ and $M_2$ are on while $M_4$ and $M_9$ are off, thus passing D at the falling transition of the clock. When CLKB is high, the master feedback tri-state feedback inverter is off and the data on the intermediate node after the mux stage is invertered once. During this phase of the clock, the slave input transmission gate is off and the feedback inverter turns on, thus holding the previous output value. In the next phase, when CLKB is low, the slave transmission gate is on and the slave feedback tri-state inverter is turned off thus passing the value of the intermediate node to Q. At the same time, the master tri-state feedback stage inverter is on and holds its value. Fig. 4.8 shows the layout of the register.
4.2.4 Core Layout

Since the proposed design adopts a stochastic approach, which depends on the plurality of stages, layout matching is critical to reduce mismatch between stages and improve circuit performance. The design utilizes 1020 delay cells which requires the same number of each of the TSPC registers and static registers. Therefore, the delay cell, TSPC register, and the static register form one slice of the TDC, as shown in Fig. 4.9. The layout of the slice is shown in Fig. 4.10. This layout is replicated 1020 times and routed in a snake pattern to reduce the design’s total area.
4.3 Phase Detector

Fig. 4.11 illustrates the implementation of the PD. The PD is designed to detect the phase difference between the falling edges of its inputs. The operation of the PD is as follows: Initially the PD is in inactive state with both its outputs at logic low. In the case of a falling transition on input A before input B, the PD activates QA resulting in QA at logic high and QB at logic low. The circuit holds this state until a falling transition occurs.
on input B forcing QA and QB to be at logic high. Consequently, reset is activated when QA=1 and QB=1 using the NAND gate shown in Fig. 4.11, returning the PD to inactive state. The PD outputs narrow, coincident pulses to avoid dead zones [27].

![Figure 4.11: Implementation of PD](image)

Fig. 4.12 shows the implementation of the D flipflop of the PD. The flipflop consists of two cross-coupled set-reset (SR) latches each consists of two cross-coupled 2-input NAND gates. The SR latch is considered a simple one-bit memory bistable device with two inputs: Set (S) and Reset (R). In this flip-flop design, the clock is connected to the set input from the first latch and reset is connected to the reset input from the second latch. The PD layout is shown in Fig. 4.13 with the upper part showing the flip-flops layout. The layout bottom part shows the OR gate combination with two extra inverters connected to the flip-flop’s reset input.
Figure 4.12: Implementation of D flipflop

Figure 4.13: PD Layout
4.4 Charge Pump and Loop Filter

4.4.1 Charge Pump

The charge pump design translates the PD outputs to currents, which are then converted to a voltage by the LF. The schematic of the CP is shown in Fig. 4.14 where $M_1$ and $M_5$ operate as current sources conducting a current of 100 $\mu$A, and while $M_3$ and $M_4$ operate as switches. $M_7$ and $M_8$ provide a path for the current sources when $M_3$ or $M_4$ are turned off, shortening the recovering time.

Since $M_4$ is a PMOS transistor that activates on logic low, QA needs to be inverted, requiring an inverter. To compensate for the inverter delay for the QB path, a pass gate stage with the same delay is placed between QB and $M_3$. The same applies to $M_7$ and

![Figure 4.14: CP schematic](image-url)
Table 4.3 summarizes the sizing of the transistors shown in Fig. 4.14. The nominal resistance values of \( R_1 \) and \( R_2 \) are 11k\( \Omega \) and 11.6k\( \Omega \), respectively.

<table>
<thead>
<tr>
<th>MOS Number</th>
<th>W(( \mu \text{m} ))</th>
<th>L(( \mu \text{m} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,M2</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>M3,M7</td>
<td>5</td>
<td>0.18</td>
</tr>
<tr>
<td>M4,M8</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>M5,M6</td>
<td>30</td>
<td>0.5</td>
</tr>
<tr>
<td>M9,M15</td>
<td>0.83</td>
<td>0.18</td>
</tr>
<tr>
<td>M10,M16</td>
<td>1.66</td>
<td>0.18</td>
</tr>
<tr>
<td>M11,M13</td>
<td>0.42</td>
<td>0.18</td>
</tr>
<tr>
<td>M12,M14</td>
<td>0.84</td>
<td>0.18</td>
</tr>
</tbody>
</table>

According to Table 4.3, it can be noticed that the sizes of transistor \( M_5 \) and \( M_2 \) are not equal although they pass the same current. Therefore, the capacitance at their drains are not equal (node \( X \) and node \( Y \)), thus creating fluctuations on \( V_{\text{ctrl}1} \). This design nonideality can be explained as follows: When both \( M_3 \) and \( M_4 \) are off, the capacitance on \( M_2 \) drain is fully discharged and the capacitance on \( M_5 \) drain is fully charged. In the case of both \( M_3 \) and \( M_4 \) being turned on, ideally \( M_2 \) drain voltage, \( V_{D_2} \), and \( M_5 \) drain voltage, \( V_{D_5} \), are approximately equal to \( V_{\text{ctrl}1} \). However, since the capacitances on node \( X \) and node \( Y \) are not equal as mentioned earlier, \( V_{D_2} \) and \( V_{D_5} \) will not be equal, thus causing fluctuations on \( V_{\text{ctrl}1} \) [27]. In order to suppress this abnormality in operation, two extra switches \( M_7 \) and \( M_8 \) are added to the design. For example, in the case of QB at logic high and QA at logic low, \( M_3 \) is turned on and \( M_4 \) is turned off. Consequently, \( M_7 \) is turned off and \( M_8 \) is turned on, thus discharging the capacitance on node \( X \). The same applies to node \( Y \) when \( M_3 \) is off and \( M_4 \) is on. Fig. 4.15 shows the full layout of the CP with dummy gates added on both sides of each current source to minimize mismatch.
4.4.2 Loop Filter

The LF is designed to be programmable with two switches that can change the value of the resistance. Table 4.4 shows the effective resistance of the LF for different switch configuration. The programmable resistance allows debugging by changing the dynamics of the DLL where the capacitors values are $C_p = 222.2pF, C_2 = 11.11pF$. The schematic of the loop filter is shown in Fig. 4.16.

<table>
<thead>
<tr>
<th>$S_0$</th>
<th>$S_1$</th>
<th>Resistance Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>Open</td>
<td>3K $\Omega$</td>
</tr>
<tr>
<td>Open</td>
<td>Closed</td>
<td>1.5K $\Omega$</td>
</tr>
<tr>
<td>Closed</td>
<td>Open</td>
<td>0 $\Omega$</td>
</tr>
<tr>
<td>Closed</td>
<td>Closed</td>
<td>0 $\Omega$</td>
</tr>
</tbody>
</table>

The design of the switches is based on a pass gate with an inverter, as shown in Fig. 4.17. The switch can be programmed through a shift register. The switch layout is shown in Fig. 4.18 and Table 4.5 summarizes the transistor sizing. Fig. 4.19 shows the layout of the LF.
Figure 4.17: Switch Schematic

Figure 4.18: Switch Layout

Table 4.5: Switch Sizing

<table>
<thead>
<tr>
<th>MOS Number</th>
<th>W(µm)</th>
<th>L(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>3</td>
<td>0.18</td>
</tr>
<tr>
<td>M2</td>
<td>6</td>
<td>0.18</td>
</tr>
<tr>
<td>M3</td>
<td>36</td>
<td>0.18</td>
</tr>
<tr>
<td>M4</td>
<td>9</td>
<td>0.18</td>
</tr>
</tbody>
</table>
Figure 4.19: Loopfilter Layout
4.5 Wallace-Tree Encoder Circuit

The Wallace-tree encoder converts the 1020 outputs from the static registers to a 10-bit binary number by counting the number of ‘1’s’. An example 3-bit Wallace Tree encoder is shown in Fig. 4.20. The encoder uses full adders to compress all the inputs that have the same bit-weight into a binary-weighted output. Each full adder takes 3 weight-one input bits and outputs 2 binary-weighted bits.

The operation of the encoder in Fig. 4.20 is as follows: The inputs to the circuit have the same bit weight. Each set of the three inputs are summed together in a 3:2 full-adder except for the seventh input which is directly provided to the second layer. The outputs of the first layer \((sum_1, Cout_1, sum_2, Cout_2)\) are binary-weighted; each binary-weighted output is grouped together and then compressed in the second layer \((sum_1, sum_2, Cout_1, Cout_2)\). The operation continues until one bit of each bit-weight remains since all stages use a carry-save adder except the last stage that uses a carry-ripple adders. The operation can be very fast since the delay between layers is only one full-adder delay.

![Wallace-Tree Encoder Diagram](image-url)

Figure 4.20: 7x3 Wallace-Tree encoder
The Wallace tree encoder is fully synthesized using Cadence. Appendix A shows the verilog code for the encoder. The structural pipeline topology was selected in order to take advantage of the increased throughput of the pipelining and to balance the trade-off between power consumption, throughput, and latency. The latency of this design is two clock cycles. Fig. 4.20 shows a high-level block diagram of a sub-section of the encoder that takes 31 inputs and produces a 5-bit output.
Figure 4.21: 31x5 sub-section of the Wallace-tree encoder
CHAPTER 5. MEASUREMENT RESULTS

To validate the effectiveness of the proposed TDC design, a prototype chip is designed and fabricated in 0.18 μm CMOS technology. A micrograph picture of the chip is shown in Fig. 5.1. The occupies an area of 1.5366 mm$^2$. The chip operates with a 60MHz clock and draws a total current of 13.8 mA ($I_{VDDA}=10.9$ mA, $I_{VDDD}=2.6$ mA, $I_{VDDIO}=0.3$ mA) from 1.8 V supply.

![Microphotograph of the chip](image)

Figure 5.1: Microphotograph of the chip

5.1 Testbench Setup

Fig. 5.2 shows a high-level block diagram of the testbench setup for the TDC. The testbench consists of a custom designed PCB with the fabricated chip soldered on it, RF signal generators (Agilent N9310A, HP 8656B), power supplies (Keysight E3630A), logic analyzer (1692A Agilent Technologies) and an oscilloscope (Keysight DSOS204A). The testbench was automated so that the computer controls two RF signal generators that represent the circuit inputs A and B and sets the amplitude and aligns the two signals to the clock with feedback from the oscilloscope. The frequencies of A and B are slightly different to allow one signal to slide slowly over the other in time, effectively generating a time input ramp.
A custom PCB was designed to test the proposed TDC design. Fig. 5.3 shows the top layer of the PCB. The chip is placed in the middle of the board; both packaged and bare die chips were tested in an attempt to reduce noise, but no noticeable difference was observed. Three SMA connectors were soldered on the PCB for the clock and inputs A and B. The traces from these signals to the design were made smooth without any angles in the path to avoid reflection and maintain signal integrity. Two potentiometers set the CP currents. Many probing points were distributed in the PCB including probing points for the clock, A and B in order to view these signals and perform initial alignment through the testing system. All the polygon pour around the digital output traces on both layers of the PCB was removed in order to reduce coupling and parasitic capacitances. Moreover, the polygon pour around $V_{ctrl1}$ probing point was also removed and a 0Ω resistor footprint was placed between the probing point and the TDC footprint pad to reduce the effect of the oscilloscope probe capacitance on $V_{ctrl1}$. Fig. 5.4 shows the bottom layer of the custom PCB.
Figure 5.3: Custom PCB top layer

Figure 5.4: Custom PCB bottom layer
Fig. 5.5 shows the PCB with the design soldered on it. As shown in the figure, the SMA connectors serve as an interface between the function generators and the design inputs. The rest of the design ports are connected to the external hardware through headers. The surface mount decoupling capacitors minimize the noise from the power supplies. The CMOS die is placed in the middle of the bottom PCB layer and wire bonded to the traces in order to reduce noise. Fig. 5.6 shows the complete testbench setup with the test equipments connected to the PCB. Each power supply has an ammeter and voltmeter to observe the power consumption. An external precise supply voltage is used to set $V_{ctrl2}$.

Figure 5.5: PCB with external connections
Fig. 5.7 shows the schematic of the filter network used to reduce the noise from the pattern generator. The filter attenuates the noise in the clock and data lines of the pattern generator. $SDI_o$, $SE_o$ and $SCLK_o$ are the digital inputs to the TDC after filtering. The filter consists of an inductor and capacitor network with a voltage divider to level shift the pattern generator voltage to 1.8 V.
5.2 Experimental Results

The backend of the design consists of the static registers and the encoder. The backend was tested by itself by writing test vectors into the static registers and reading the outputs. The testbench consisted of a Diligent Analog Discovery pattern generator, logic analyzer, power supplies, and an oscilloscope. The pattern generator produces random input vectors while the logic analyzer reads the outputs of the design. Data is processed in Matlab to compare the acquired data versus the expected output. To test the TDC, 60-MHz, 30-MHz, and 30.000012-MHz signals are applied to the clock, A, and B inputs, respectively. The different input frequencies create an output code ramp. Fig. 5.8 and Fig. 5.9 show the testbench setup that was used to test the proposed TDC at 60°C and -10°C.

Figure 5.8: TDC in oven to test at 60°C
The TDC is designed using $2^{10}$ delay stages with 2-bit LSB truncation to get the final 8-bit output. To plot the DNL and INL, the input was swept 256 times and the outputs were averaged to remove thermal noise. Fig. 5.10 shows the TDC’s unaveraged transfer characteristic that is used to calculate its static nonlinearities.

Under all testing conditions, the TDC transfer characteristic show some nonlinearity at midscale as shown in the magnified area in Fig. 5.10. It is suspected that this nonlinearity is caused by the ripple of $V_{ctrl}$ caused by the CP. Since the VCDL is designed to delay the negative edge of the reference clock combined with jitter it can cause long reset time of the negative edge triggered PD. Therefore, wide CP enable pulses (QA and QB) are generated. These wide pulses can cause clock feedthrough even when the CP is turned off (as discussed in a following section) due to the coupling capacitance between gate-source and gate-drain for both switches $M_3$ and $M_4$ shown in Fig. 4.14. For example, when input to $M_3$ goes high, the input feeds through the gate-drain and gate-source capacitors. When the input goes low, $M_3$ is off. This creates a capacitive voltage divider between the gate-drain capacitor and the LF, which causes a static phase offset that becomes larger as the enable pulse width
increases. As phase offset accumulates, the differential nonlinearity (DNL) error increases for each code. Therefore, the DLL attempts to adjust the control voltage by decreasing it, in order to maintain locking; thus, a flat region at midscale appears as shown in the magnified area in Fig. 5.10. As shown in all the DNL figures in the next section, a drop in DNL happens directly after midscale code due to the adjustment of $V_{ctrl1}$. Consequently, since the integral nonlinearity (INL) error of each code is the summation of all previous DNL errors, an INL spike at midscale code appears. This problem can be resolved by clocking the CP in the beginning or the end of the sampling period instead of the middle, but this requires a chip re-design.

![Figure 5.10: 8-bit Stochastic TDC transfer characteristic](image)

5.2.1 Static Nonlinearities

Differential non-linearity (DNL) error is the maximum deviation from the ideal code transition of one LSB. DNL can be expressed in terms of LSB by the following equation, where $1 < n \leq 256$, $1 \text{ LSB} = \frac{16 ns}{2^m}$ and $m = 8$,

$$DNL = \frac{T_{n+1} - T_n}{T_{LSB}} - 1. \quad (5.1)$$
The relative accuracy of a TDC is the deviation of the output from a straight line drawn through zero and full scale. Such relative accuracy is sometimes referred to as integral non-linearity error (INL). INL error can be calculated either by finding the deviation from the ideal slope or by the accumulation of DNL errors to produce the total INL. The integral non-linearity can be expressed by the following equation, where $m$ represent the code value,

$$INL[m] = \sum_{i=1}^{m-1} DNL[i].$$ (5.2)

Tables 5.1 and 5.2 list the simulated and measured static nonlinearities under all testing conditions, respectively. All the measured INL results listed exclude the midscale spike. It can be noticed from the tables that the proposed TDC doesn’t miss any code while the input is swept over its range, which indicates that all the output code combinations appeared at the converter output. By comparing the INL error, it can be seen that the simulated and measured results closely agree and shows tolerance to PVT variations. The following figures shows the simulated and measured output transfer characteristic and static nonlinearities under $V_{DD} = 1.8V, T = 27^\circ C$. Please refer to appendix B for the simulated and measured TDC characteristics figures for the varying test conditions.

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C$</td>
<td>+0.997/-0.878</td>
<td>+0.925/-0.925</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C$</td>
<td>+1.109/-0.8624</td>
<td>+0.9451/-0.9451</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C$</td>
<td>+1.39/-0.9387</td>
<td>+0.9272/-0.9272</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C$</td>
<td>+1.221/-0.800</td>
<td>+0.9289/-0.9289</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C$</td>
<td>+1.281/-0.8316</td>
<td>+0.959/-0.959</td>
</tr>
</tbody>
</table>
Table 5.2: Measured static nonlinearities

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C$</td>
<td>+0.77/-0.65</td>
<td>+1.0585/-1.0585</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C$</td>
<td>+1.25/-0.5352</td>
<td>+1.0463/-1.0463</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C$</td>
<td>+1.339/-0.6912</td>
<td>+1.017/-1.017</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C$</td>
<td>+1.677/-0.6079</td>
<td>+1.013/-1.013</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C$</td>
<td>+0.9234/-0.5335</td>
<td>+1.006/-1.006</td>
</tr>
</tbody>
</table>

Figure 5.11: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C$

Figure 5.12: Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C$
Figure 5.13: Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C$

Figure 5.14: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C$

Figure 5.15: Measured DNL, $V_{DD} = 1.8V, T = 27^\circ C$
5.2.2 Power Consumption

Table 5.3 lists the power consumption under all test conditions. The power consumption was recorded when both circuit inputs are active. The table shows the pulled current from each power supply where $I_{VDDA}$, $I_{VDDD}$ and $I_{VDDIO}$ represent the current from $V_{DDA}$, $V_{DDD}$ and $V_{DDIO}$, respectively. Referring to Fig. 5.2, $V_{DDA}$, $V_{DDD}$ and $V_{DDIO}$, represent the voltage supply powering the design’s front-end, the design’s back-end and the input-output pads, respectively. Table 5.4 lists the power consumption when both circuit inputs are inactive. By comparing the current consumption in both tables, it can be noticed that current consumption from $V_{DDD}$ is higher when both circuit inputs are active due to the design’s back-end operation and high activity factor. In general the power consumption when clock is running and both inputs are active is higher than when both inputs are inactive.

Table 5.3: Power Consumption, circuit inputs active

<table>
<thead>
<tr>
<th>Test Case</th>
<th>$I_{VDDA},I_{VDDD},I_{VDDIO}$ (mA)</th>
<th>Power Consumption(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C$</td>
<td>10.9, 2.6, 0.3</td>
<td>24.84</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C$</td>
<td>9.8, 2.3, 0.3</td>
<td>20.09</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C$</td>
<td>12.2, 2.9, 0.4</td>
<td>30.69</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C$</td>
<td>10.9, 2.4, 0.7</td>
<td>25.2</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C$</td>
<td>11.7, 2.47, 1</td>
<td>27.306</td>
</tr>
</tbody>
</table>
Table 5.4: Power Consumption, circuit inputs inactive

<table>
<thead>
<tr>
<th>Test Case</th>
<th>$I_{VDDA},I_{VDDD},I_{VDDIO}$ (mA)</th>
<th>Power Consumption(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C$</td>
<td>11.8, 1.8, 0.5</td>
<td>25.38</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C$</td>
<td>9.5, 0.8, 0.4</td>
<td>17.33</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C$</td>
<td>13.5, 1.2, 0.6</td>
<td>30.29</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C$</td>
<td>11.6, 1.5, 0.7</td>
<td>24.84</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C$</td>
<td>11.8, 1.1, 1.12</td>
<td>25.236</td>
</tr>
</tbody>
</table>

5.2.3 TDC Characterization Without DLL

To demonstrate the problem of the non-integer number of wrap-around of the conventional TDC and the effectiveness of the proposed solution, the TDC is tested with the DLL turned on and off. In order to turn off the DLL, the current sources in the CP were turned off. The control voltages $V_{ctrl1}$ and $V_{ctrl2}$ were adjusted using external voltage sources.

To verify the adverse effect of non-integer number of wrap-arounds predicted from the analysis in Chapter 2, three cases of non-integer warp-around are tested under normal operating conditions. The output transfer characteristic and static nonlinearities both simulations and measurements are presented. Each of the presented cases is created by setting the appropriate $V_{ctrl1}$ value while $V_{ctrl2}$ is fixed to 900 mV. To observe the effect of the supply voltage and temperature variations on the output linearity when $N$ is non-integer, the proposed TDC was tested under different temperatures and supply voltages while maintaining the same values of $V_{ctrl1}$ and $V_{ctrl2}$. Both simulated and measured results are presented in the following figures and appendix C. The following tables summarize the simulated and measured DNL and INL errors under all testing conditions for each non-integer $N$ case. The nominal value of $N$ is denoted by $N_o$, and the actual value of $N$ is denoted by $N_{act}$ where it represents the actual value of $N$ when tested under varying testing conditions.
Table 5.5: Simulated static linearties, Fractional \( N_o=0.32 \)

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} = 1.8V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.32 )</td>
<td>+1.391/-0.8161</td>
<td>+2.177/-2.177</td>
</tr>
<tr>
<td>( V_{DD} = 1.62V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.57 )</td>
<td>+1.327/-0.8163</td>
<td>+2.682/-2.682</td>
</tr>
<tr>
<td>( V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.62 )</td>
<td>+1.288/-0.817</td>
<td>+2.421/-2.421</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = -10^\circ C, N_o = 0.32, N_{act} = 0.35 )</td>
<td>+1.65/-0.8162</td>
<td>+2.208/-2.208</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.32, N_{act} = 0.34 )</td>
<td>+1.129/-0.8621</td>
<td>+2.189/-2.189</td>
</tr>
</tbody>
</table>

Table 5.6: Measured static linearties, Fractional \( N_o=0.32 \)

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} = 1.8V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.32 )</td>
<td>+1.733/-0.5706</td>
<td>+2.3006/-2.3006</td>
</tr>
<tr>
<td>( V_{DD} = 1.62V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.57 )</td>
<td>+1.101/-0.6729</td>
<td>+2.473/-2.473</td>
</tr>
<tr>
<td>( V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.62 )</td>
<td>+1.868/-0.6486</td>
<td>+2.0645/-2.0645</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = -10^\circ C, N_o = 0.32, N_{act} = 0.35 )</td>
<td>+1.856/-0.6747</td>
<td>+2.4411/-2.4411</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.32, N_{act} = 0.34 )</td>
<td>+0.7765/-0.6014</td>
<td>+1.6533/-1.6533</td>
</tr>
</tbody>
</table>

Table 5.7: Simulated static linearties, Fractional \( N_o=0.69 \)

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} = 1.8V, T = 27^\circ C, N_o = 0.69, N_{act} = 0.69 )</td>
<td>+1.311/-0.8011</td>
<td>+2.194/-2.194</td>
</tr>
<tr>
<td>( V_{DD} = 1.62V, T = 27^\circ C, N_o = 0.69, N_{act} = 0.89 )</td>
<td>+1.203/-0.8011</td>
<td>+1.69/-1.69</td>
</tr>
<tr>
<td>( V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.69, N_{act} = \text{integer} )</td>
<td>+1.249/-0.8317</td>
<td>+0.7789/-0.7789</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = -10^\circ C, N_o = 0.69, N_{act} = 0.714 )</td>
<td>+1.315/-0.8007</td>
<td>+2.039/-2.039</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.69, N_{act} = 0.70 )</td>
<td>+1.114/-0.8928</td>
<td>+2.019/-2.019</td>
</tr>
</tbody>
</table>
Table 5.8: Measured static linearties, Fractional $N_o=0.69$

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C, N_o = 0.69, N_{act} = 0.69$</td>
<td>+1.071/-0.6766</td>
<td>+2.1039/-2.1039</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C, N_o = 0.69, N_{act} = 0.89$</td>
<td>+1.868/-0.7045</td>
<td>+2.1575/-2.1575</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.69, N_{act} = integer$</td>
<td>+0.8609/-0.5157</td>
<td>+1.388/-1.388</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C, N_o = 0.69, N_{act} = 0.714$</td>
<td>+1.646/-0.8045</td>
<td>+2.55/-2.55</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.69, N_{act} = 0.70$</td>
<td>+0.8723/-0.5714</td>
<td>+1.7471/-1.7471</td>
</tr>
</tbody>
</table>

Table 5.9: Simulated static linearties, Fractional $N_o=0.81$

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C, N_o = 0.81, N_{act} = 0.81$</td>
<td>+1.094/-0.9389</td>
<td>+2.075/-2.075</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C, N_o = 0.81, N_{act} = integer$</td>
<td>+1.383/-0.8167</td>
<td>+0.9636/-0.9636</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.81, N_{act} = 0.13$</td>
<td>+1.276/-0.7861</td>
<td>+1.695/-1.695</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C, N_o = 0.81, N_{act} = 0.84$</td>
<td>+1.31/-0.8012</td>
<td>+1.923/-1.923</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.81, N_{act} = 0.82$</td>
<td>+1.004/-0.8304</td>
<td>+1.295/-1.295</td>
</tr>
</tbody>
</table>

Table 5.10: Measured static linearties, Fractional $N_o=0.81$

<table>
<thead>
<tr>
<th>Test Case</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 1.8V, T = 27^\circ C, N_o = 0.81, N_{act} = 0.81$</td>
<td>+1.469/-0.6717</td>
<td>+2.934/-2.934</td>
</tr>
<tr>
<td>$V_{DD} = 1.62V, T = 27^\circ C, N_o = 0.81, N_{act} = integer$</td>
<td>+0.9986/-0.581</td>
<td>+1.2524/-1.2524</td>
</tr>
<tr>
<td>$V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.81, N_{act} = 0.13$</td>
<td>+1.41/-0.6276</td>
<td>+2.3189/-2.3189</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = -10^\circ C, N_o = 0.81, N_{act} = 0.84$</td>
<td>+1.581/-0.799</td>
<td>+2.1393/-2.1393</td>
</tr>
<tr>
<td>$V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.81, N_{act} = 0.82$</td>
<td>+0.8614/-5158</td>
<td>+1.3233/-1.3233</td>
</tr>
</tbody>
</table>
Figure 5.17: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$

Figure 5.18: Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$

Figure 5.19: Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$
Figure 5.20: Measured Transfer Characteristic, $V_{DD} = 1.8\,V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$

Figure 5.21: Measured DNL, $V_{DD} = 1.8\,V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$

Figure 5.22: Measured INL, $V_{DD} = 1.8\,V, T = 27^\circ C, N_o=0.32, N_{act}=0.32$
From the presented figures in this section and the figures in appendix C, it can be seen that \( N_o \) changes when the supply voltage or temperature varies from the nominal values. This shifts the location of the peak INL but not the value of it, as predicted by the analysis. This contrasts with the proposed TDC whose INL is about a factor or two lower. In addition, the proposed TDC does not have a noticeable peak (ignoring the midscale error) due to the uniform phase distribution as predicted by the analysis.

5.3 Figure of Merit and the Effective Number of Linear Bits

The effective number of linear bits \( N_{\text{linear}} \) for TDCs is a metric as a replacement for the effective number of bits (ENOB) typically used for voltage ADCs. \( N_{\text{linear}} \) is used for TDCs because it is very challenging to create a pure sinusoidal time input signal to calculate the ENOB. The equation of \( N_{\text{linear}} \) is introduced in [33] [34] as follows

\[
N_{\text{linear}} = \text{Bits} - \log_2(INL + 1),
\]

where \( \text{Bits} \) is the number of bits the TDC and INL is the peak INL. Therefore, the figure-of-Merit (FoM) of a TDC proposed in [35] can be calculated as follows

\[
\text{FoM}_{TDC} = \frac{\text{Power}}{2^{N_{\text{linear}}} \times F_s} [pJ/\text{conv.step}],
\]

where \( F_s \) represent the sampling frequency. Table 5.11 lists \( N_{\text{linear}} \) and FoM under all test conditions.

<table>
<thead>
<tr>
<th>Test Case</th>
<th>( N_{\text{linear}} )</th>
<th>FoM [pJ/conv.step]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} = 1.8V, T = 27^\circ C )</td>
<td>6.36</td>
<td>5.04</td>
</tr>
<tr>
<td>( V_{DD} = 1.62V, T = 27^\circ C )</td>
<td>6.41</td>
<td>3.98</td>
</tr>
<tr>
<td>( V_{DD} = 1.98V, T = 27^\circ C )</td>
<td>6.38</td>
<td>6.23</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = -10^\circ C )</td>
<td>6.38</td>
<td>5.04</td>
</tr>
<tr>
<td>( V_{DD} = 1.8V, T = 60^\circ C )</td>
<td>6.41</td>
<td>5.35</td>
</tr>
</tbody>
</table>
Table 5.12: Performance summary and comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>350nm CMOS</td>
<td>350nm CMOS</td>
<td>350nm CMOS</td>
<td>14nm FinFET</td>
<td>180nm CMOS</td>
</tr>
<tr>
<td>Supply(V)</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td>0.6</td>
<td>1.8</td>
</tr>
<tr>
<td>Bits</td>
<td>15</td>
<td>5</td>
<td>15</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>Resolution(ps)</td>
<td>10</td>
<td>37.5</td>
<td>12.2</td>
<td>1.17</td>
<td>62.5</td>
</tr>
<tr>
<td>PVT Tolerant</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Area(mm$^2$)</td>
<td>0.3</td>
<td>0.222</td>
<td>7.5</td>
<td>0.036</td>
<td>1.5366</td>
</tr>
<tr>
<td>Speed(MS/s)</td>
<td>100</td>
<td>56</td>
<td>5</td>
<td>850</td>
<td>60</td>
</tr>
<tr>
<td>Power(mW)</td>
<td>&lt;80</td>
<td>150</td>
<td>40</td>
<td>0.78</td>
<td>24.84</td>
</tr>
<tr>
<td>DNL(LSB)</td>
<td>0.08</td>
<td>0.4</td>
<td>N/A</td>
<td>0.8</td>
<td>0.77</td>
</tr>
<tr>
<td>INL(LSB)*</td>
<td>3</td>
<td>0.7</td>
<td>2.45</td>
<td>2.3</td>
<td>2.1</td>
</tr>
<tr>
<td>Range</td>
<td>160 ns</td>
<td>1.4 ns</td>
<td>3 - 12 ns</td>
<td>1.2 ns</td>
<td>16 ns</td>
</tr>
<tr>
<td>$N_{linear}$**</td>
<td>13</td>
<td>4.23</td>
<td>13.21</td>
<td>8.28</td>
<td>6.36</td>
</tr>
<tr>
<td>Type</td>
<td>Vernier Interp.</td>
<td>Vernier</td>
<td>Interp.</td>
<td>Stochastic</td>
<td>Stochastic</td>
</tr>
<tr>
<td>FoM***</td>
<td>3.255</td>
<td>0.499</td>
<td>8.442</td>
<td>0.025</td>
<td>5.04</td>
</tr>
</tbody>
</table>

* Maximum INL of entire measurement range

** $N_{linear} = \text{Bits} - \log_2(\text{INL} + 1)$

*** FoM = Power/(2$^{N_{linear}} \times F_s$) [pJ/conv.step]
CHAPTER 6. CONCLUSION

6.1 Thesis Contributions

The contributions of this thesis are:

• Designed and fabricated a DLL-based stochastic pulsed TDC using Cadence tools in 0.18 \( \mu m \) technology.

• Analyzed the linearity of stochastic delay-line TDCs and explained the problem of non-integer warp-arounds and its effect on the INL; verified the analytical model in simulations and measurement.

• Created a polar visualization of the phase distribution for the linearity analysis.

• Developed behavioral models in Matlab to simulate stochastic delay-line TDCs; verified the behavioral models with measurement results.

• Designed and fabricated PCBs for chip testing; created scripts for chip control and data acquisition.

• Measured the proposed TDC and validated the linearity theory of the stochastic delay-line TDC; measured the linearity of the TDC with and without the proposed DLL activated for different supply voltages and temperatures.

6.2 Summary

This work presented the complete design of a PVT-tolerant DLL-based stochastic pulsed TDC. Many PVT-tolerant TDC architectures and other stochastic TDC architectures were researched before but PVT-tolerant stochastic TDCs was only investigated once. The novelty in this design lies in introducing a DLL to the stochastic delay-line TDC design
proposed in [20] and due to the concept of digitizing a time pulse instead of digitizing the
time difference between the rising edges of start and stop signals. The design consists of
a DLL, a TSPC register stage, a static register stage and a Wallace Tree encoder circuit.
Extensive testing demonstrates correct functionality of all design blocks and improvements
in key metrics over prior work. The proposed design can be scaled to achieve more output
bits by extending the delay-line.

Chapter 1 discussed prior TDC topologies, stochastic TDCs and their design con-
cepts and implementation. A delay-line TDC is an excellent choice since it doesn’t require
post-calibration to improve the output code linearity as the other discussed stochastic TDC
designs.

Chapter 2 presented the linearity analysis of the TDC and the problem of non-integer
number wrap-arounds and its effect on the output code linearity. Graphical models are devel-
oped to explain the concept clearly showing the effect of non-integer number wrap-arounds
on output code linearity. The effect of nonidealities is also shown on both integer and non-
integer number of wrap-arounds.

Chapter 3 described the operation and timing of the proposed TDC design. A system
level overview of each block in the DLL, analysis of the DLL behavior and justification of
the design decisions in the loop filter and their affect on the system’s stability and transfer
characteristics. The issue of false-locking is discussed and its effect on the end-application
of the DLL.

Chapter 4 described the design of each block of the proposed TDC. This chapter
shows the schematics and layout of each block. The selection of circuit architectures is jus-
tified with explanation of design non-idealities.

Chapter 5 provides measurement results of the proposed TDC. The static nonlin-
earities behavior and power consumption under varying test conditions are listed in this
chapter. The effect of non-integer number of wrap-arounds is shown in measurement results and compared against simulated results. The performance metrics of the proposed TDC are compared against other PVT-tolerant TDC prior work.

6.3 Future Work

Listed are just a few ideas for further research on the TDC:

1. To overcome the spike in INL due to static phase offset, a positive-edge triggered PD or a double-edge triggered PD can be utilized. Since the design of the VCDL delays the negative edge, a PD that compares the positive edges of its inputs can reduce noise on $V_{ctrl1}$ due to clock feedthrough. A double-edge triggered PD can further more improve the performance of the TDC since it compares both the positive and negative edges allowing reduction in DLL locking speed.

2. In order to reduce power consumption and improve the LSB resolution, the design can be implemented in smaller CMOS technology since the resolution of a delay-line TDC depends on the propagation delay of delay stages. Therefore, improving FoM.
REFERENCES


[34] S. Kim, T. Kim, and H. Park, “A 0.63ps, 12b, synchronous cyclic TDC using a time adder for on-chip jitter measurement of a SoC in 28nm CMOS technology,” IEEE Int. Symp. VLSI Circuits Dig., Jul. 2014. 76


83
'timescale 1ns/1ns
module fadd(input A, input B, input CI, output S, output CO);
    adder_1 add(.A(A), .B(B), .CI(CI), .S(S), .CO(CO));
endmodule // fadd

module wallace ( 
    input clk,
    input clken,
    input [1019:0] Dstoch,
    output reg [9:0] D
);

reg [9:0] Dres1;
wire [9:0] Dres;

include "wallace_tree_gen.vi"
always @(posedge clk)
    if (clken) begin
        Dres1 <= Dres;
        D <= Dres1;
    end
endmodule // wallace_beh
APPENDIX B. TDC NONLINEARITIES CHARACTERIZATION

Figure B.1: Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$

Figure B.2: Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C$
Figure B.3: Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C$

Figure B.4: Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$

Figure B.5: Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C$
Figure B.6: Measured INL, $V_{DD} = 1.62\, V$, $T = 27^\circ\, C$

Figure B.7: Simulated Transfer Characteristic, $V_{DD} = 1.98\, V$, $T = 27^\circ\, C$

Figure B.8: Simulated DNL, $V_{DD} = 1.98\, V$, $T = 27^\circ\, C$
Figure B.9: Simulated INL, $V_{DD} = 1.98V, T = 27^\circ C$

Figure B.10: Measured Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C$

Figure B.11: Measured DNL, $V_{DD} = 1.98V, T = 27^\circ C$
Figure B.12: Measured INL, $V_{DD} = 1.98V, T = 27^\circ C$

Figure B.13: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C$

Figure B.14: Simulated DNL, $V_{DD} = 1.8V, T = -10^\circ C$
Figure B.15: Simulated INL, $V_{DD} = 1.8V, T = -10^\circ C$

Figure B.16: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C$

Figure B.17: Measured DNL, $V_{DD} = 1.8V, T = -10^\circ C$
Figure B.18: Measured INL, $V_{DD} = 1.8V, T = -10^\circ C$

Figure B.19: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C$

Figure B.20: Simulated DNL, $V_{DD} = 1.8V, T = 60^\circ C$
Figure B.21: Simulated INL, $V_{DD} = 1.8V, T = 60^\circ C$

Figure B.22: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C$

Figure B.23: Measured DNL, $V_{DD} = 1.8V, T = 60^\circ C$
Figure B.24: Measured INL, $V_{DD} = 1.8\, V, T = 60^\circ C$
APPENDIX C. NON-INTEGER N EFFECT ON TDC NONLINEARITIES CHARACTERIZATION

Figure C.1: Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.57$

Figure C.2: Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.57$
Figure C.3: Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.57$

Figure C.4: Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.57$

Figure C.5: Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.57$
Figure C.6: Measured INL, $V_{DD} = 1.62\, V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.57$

Figure C.7: Simulated Transfer Characteristic, $V_{DD} = 1.98\, V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.62$

Figure C.8: Simulated DNL, $V_{DD} = 1.98\, V, T = 27^\circ C$, $N_o=0.32$, $N_{act}=0.62$
Figure C.9: Simulated INL, $V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.62$

Figure C.10: Measured Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.62$

Figure C.11: Measured DNL, $V_{DD} = 1.98V, T = 27^\circ C, N_o = 0.32, N_{act} = 0.62$
Figure C.12: Measured INL, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.32, N_{act}=0.62$

Figure C.13: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35$

Figure C.14: Simulated DNL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35$
Figure C.15: Simulated INL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35$

Figure C.16: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35$

Figure C.17: Measured DNL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.32, N_{act}=0.35$
Figure C.18: Measured INL, $V_{DD} = 1.8\, V$, $T = -10^\circ C$, $N_0=0.32$, $N_{act}=0.35$

Figure C.19: Simulated Transfer Characteristic, $V_{DD} = 1.8\, V$, $T = 60^\circ C$, $N_0=0.32$, $N_{act}=0.34$

Figure C.20: Simulated DNL, $V_{DD} = 1.8\, V$, $T = 60^\circ C$, $N_0=0.32$, $N_{act}=0.34$
Figure C.21: Simulated INL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34$

Figure C.22: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34$

Figure C.23: Measured DNL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32, N_{act}=0.34$
Figure C.24: Measured INL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.32$, $N_{act}=0.34$

Figure C.25: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69$, $N_{act}=0.69$

Figure C.26: Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.69$, $N_{act}=0.69$
Figure C.27: Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.69$

Figure C.28: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.69$

Figure C.29: Measured DNL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.69$
Figure C.30: Measured INL, $V_{DD} = 1.8V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.69$

Figure C.31: Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.89$

Figure C.32: Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.89$
Figure C.33: Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89$

Figure C.34: Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89$

Figure C.35: Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.69, N_{act}=0.89$
Figure C.36: Measured INL, $V_{DD} = 1.62\, V$, $T = 27^\circ C$, $N_o=0.69$, $N_{act}=0.89$

Figure C.37: Simulated Transfer Characteristic, $V_{DD} = 1.98\, V$, $T = 27^\circ C$, $N_o=0.69$, $N_{act}=\text{integer}$

Figure C.38: Simulated DNL, $V_{DD} = 1.98\, V$, $T = 27^\circ C$, $N_o=0.69$, $N_{act}=\text{integer}$
Figure C.39: Simulated INL, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=\text{integer}$

Figure C.40: Measured Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=\text{integer}$

Figure C.41: Measured DNL, $V_{DD} = 1.98V, T = 27^\circ C$, $N_o=0.69$, $N_{act}=\text{integer}$
Figure C.42: Measured INL, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.69, N_{act}=\text{integer}$

Figure C.43: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714$

Figure C.44: Simulated DNL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714$
Figure C.45: Simulated INL, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.69$, $N_{act}=0.714$

Figure C.46: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.69$, $N_{act}=0.714$

Figure C.47: Measured DNL, $V_{DD} = 1.8V, T = -10^\circ C$, $N_o=0.69$, $N_{act}=0.714$
Figure C.48: Measured INL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.69, N_{act}=0.714$

Figure C.49: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70$

Figure C.50: Simulated DNL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70$
Figure C.51: Simulated INL, $V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.69, N_{act} = 0.70$

Figure C.52: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.69, N_{act} = 0.70$

Figure C.53: Measured DNL, $V_{DD} = 1.8V, T = 60^\circ C, N_o = 0.69, N_{act} = 0.70$
Figure C.54: Measured INL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.69, N_{act}=0.70$

Figure C.55: Simulated Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.81, N_{act}=0.81$

Figure C.56: Simulated DNL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.81, N_{act}=0.81$
Figure C.57: Simulated INL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.81, N_{act}=0.81$

Figure C.58: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.81, N_{act}=0.81$

Figure C.59: Measured DNL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.81, N_{act}=0.81$
Figure C.60: Measured INL, $V_{DD} = 1.8V, T = 27^\circ C, N_o=0.81, N_{act}=0.81$

Figure C.61: Simulated Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.81, N_{act} = \text{integer}$

Figure C.62: Simulated DNL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.81, N_{act} = \text{integer}$
Figure C.63: Simulated INL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.81, N_{act} = \text{integer}$

Figure C.64: Measured Transfer Characteristic, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.81, N_{act} = \text{integer}$

Figure C.65: Measured DNL, $V_{DD} = 1.62V, T = 27^\circ C, N_o=0.81, N_{act} = \text{integer}$
Figure C.66: Measured INL, $V_{DD} = 1.62\,V, T = 27^\circ C$, $N_o=0.81$, $N_{act} = integer$

Figure C.67: Simulated Transfer Characteristic, $V_{DD} = 1.98\,V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$

Figure C.68: Simulated DNL, $V_{DD} = 1.98\,V, T = 27^\circ C$, $N_o=0.81$, $N_{act}=0.13$
Figure C.69: Simulated INL, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.81, N_{act}=0.13$

Figure C.70: Measured Transfer Characteristic, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.81, N_{act}=0.13$

Figure C.71: Measured DNL, $V_{DD} = 1.98V, T = 27^\circ C, N_o=0.81, N_{act}=0.13$
Figure C.72: Measured INL, $V_{DD} = 1.98\,\text{V}, T = 27^\circ\text{C}$, $N_o=0.81$, $N_{act}=0.13$

Figure C.73: Simulated Transfer Characteristic, $V_{DD} = 1.8\,\text{V}, T = -10^\circ\text{C}$, $N_o=0.81$, $N_{act}=0.84$

Figure C.74: Simulated DNL, $V_{DD} = 1.8\,\text{V}, T = -10^\circ\text{C}$, $N_o=0.81$, $N_{act}=0.84$
Figure C.75: Simulated INL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.81, N_{act}=0.84$

Figure C.76: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.81, N_{act}=0.84$

Figure C.77: Measured DNL, $V_{DD} = 1.8V, T = -10^\circ C, N_o=0.81, N_{act}=0.84$
Figure C.78: Measured INL, $V_{DD} = 1.8 V, T = -10^\circ C, N_o=0.81, N_{act}=0.84$

Figure C.79: Simulated Transfer Characteristic, $V_{DD} = 1.8 V, T = 60^\circ C, N_o=0.81, N_{act}=0.82$

Figure C.80: Simulated DNL, $V_{DD} = 1.8 V, T = 60^\circ C, N_o=0.81, N_{act}=0.82$
Figure C.81: Simulated INL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.81, N_{act}=0.82$

Figure C.82: Measured Transfer Characteristic, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.81, N_{act}=0.82$

Figure C.83: Measured DNL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.81, N_{act}=0.82$
Figure C.84: Measured INL, $V_{DD} = 1.8V, T = 60^\circ C, N_o=0.81, N_{act}=0.82$