Brigham Young University
BYU ScholarsArchive

All Theses and Dissertations

2013-06-13

Subthreshold Op Amp Design Based on the Conventional Cascode Stage

Kurtis Daniel Cahill
Brigham Young University - Provo

Follow this and additional works at: https://scholarsarchive.byu.edu/etd

 Part of the Electrical and Computer Engineering Commons

BYU ScholarsArchive Citation

Cahill, Kurtis Daniel, "Subthreshold Op Amp Design Based on the Conventional Cascode Stage" (2013). *All Theses and Dissertations*. 3611.
https://scholarsarchive.byu.edu/etd/3611

This Thesis is brought to you for free and open access by BYU ScholarsArchive. It has been accepted for inclusion in All Theses and Dissertations by an authorized administrator of BYU ScholarsArchive. For more information, please contact scholarsarchive@byu.edu, ellen_amatangelo@byu.edu.

Subthreshold Op Amp Design Based on the Conventional Cascode Stage

Kurtis Cahill

A thesis submitted to the faculty of
Brigham Young University
in partial fulfillment of the requirements for the degree of

Master of Science

David J. Comer, Chair
Doran K. Wilde
Richard H. Selfridge

Department of Electrical and Computer Engineering

Brigham Young University

June 2013

Copyright © 2013 Kurtis Cahill

All Rights Reserved

ABSTRACT

Subthreshold Op Amp Design Based on the Conventional Cascode Stage

Kurtis Cahill
Department of Electrical and Computer Engineering
Master of Science

Op amps are among the most-used components in electronic design. Their performance is important and is often measured in terms of gain, bandwidth, power consumption, and chip area. Although BJT amplifiers can achieve high gains and bandwidths, they tend to consume a lot of power. CMOS amplifiers utilizing the strong inversion region alone use less power than BJT amplifiers, but generally have lower gains and bandwidths. When CMOS SPICE models were improved to accurately simulate all regions of inversion, researchers began to test the performance of amplifiers operating in the weak and moderate inversion regions.

Previous work had dealt with exploring the parameters of composite cascode stages, including inversion coefficients. This thesis extends the work to include conventional cascode stages and presents an efficient method for exploring design parameters. A high-gain (137.7 dB), low power (4.347 μW) operational amplifier based on the conventional cascode stage is presented.

Keywords: subthreshold, CMOS, circuit, low-power, high-gain, inversion coefficient

ACKNOWLEDGMENTS

I thank my advisor Dr. David Comer for his guidance in the whole research process. I also thank committee members Dr. Doran Wilde and Dr. Richard Selfridge for reviewing this thesis and providing valuable feedback. I also thank my family and friends for the support that they have provided.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

Op amps are among the most-used components in electronics design. This thesis describes an approach that can be used to design op amps while improving performance in categories such as gain, bandwidth and power consumption. Subthreshold operation has proven to be effective at allowing CMOS (complementary metal-oxide-semiconductor) amplifiers to achieve high performance while consuming little power.

Early integrated amplifiers used BJTs (bipolar junction transistors) and could achieve high gains with only a few stages. BJTs also allow for high frequency operation. However, they also consume a lot of power.

Modern integrated circuits favor the use of MOSFETs (metal-oxide-semiconductor field-effect transistors) over BJTs. This is due to reduced power consumption. Up until the late 1990s, however, SPICE (Simulation Program with Integrated Circuit Emphasis) models did not accurately represent MOSFET devices in all inversion regions [1]. Thus most MOSFET amplifiers were designed to operate the devices in the strong inversion region. MOSFETs operating only in this region could not achieve the high gains of BJTs.

Enz et al. came up with a transistor model (known as the EKV model) that is valid in all regions of operation [2]. Vittoz demonstrated that operating MOSFETs in weak inversion can have performance characteristics similar to BJTs, but with the added benefit of reduced power consumption [3]. When the BSIM3v3 SPICE models became available, researchers began to look at the weak and moderate inversion regions in designing CMOS amplifier stages.

The main purpose of this research is to improve the performance of ultra-low power op amps, with emphasis on reduced power consumption. Earlier research done by the BYU circuits group focused on the use of the composite cascode stage [4, 5] in building high gain,

low power op amps while the research of this thesis extends the work to the conventional cascode configuration. A secondary purpose of this research is the development of efficient simulation methods over a wide range of parameter variations to determine near-optimal performance with respect to those parameters.

1.1 Contributions

In order to improve circuit performance, the designer must explore a great deal of design space by testing the effects of various circuit parameters (such as bias current, transistor dimensions etc.) and running the required simulations. Changing such parameters, however, requires the DC bias to be recalculated if an AC simulation is to be performed. This is traditionally done manually in SPICE. The problem with this is that each additional circuit parameter to be tested increases the design space exponentially – rendering manual simulation intractable. Although automated simulation is signficantly faster than manual simulation, it doesn't reduce the complexity of this problem. Thus a systematic (and automated) method must be used in order to cover a signficant portion of the design space. Varying appropriate parameters exponentially allows for greater testing coverage. To this end, a computer program that explores some parameters of a conventional cascode stage was written. The contributions of this thesis include:

1. the development of source code demonstrating an efficient method of running SPICE simulations for the purpose of improving circuit performance;

2. the design of a high-gain, low power operational amplifier based on the conventional cascode differential stage demonstrating principles found from the SPICE simulations.

Chapter 2

Background

In order to understand the content of this thesis, the reader must have a basic understanding of CMOS transistors, inversion coefficients and cascode configurations. The sections that follow provide some background information on these, and may be skipped if the reader wishes.

2.1 Inversion Coefficient

CMOS amplifiers can be improved by making use of inversion coefficients. Although inversion coefficients can be defined in many ways, we use the definitions given by Binkley [6]. The inversion coefficient for a CMOS device is a dimensionless quantity and is defined as

$$i_f = \frac{I_D L}{I_0 W} \tag{2.1}$$

where I_D is the drain current of the device, L and W are the length and width of the device, respectively, and I_0 is the technology current for the device. The technology current may be found by

$$I_0 = 2n\mu C_{ox}\phi_t^2 \tag{2.2}$$

where n is a substrate factor ranging from 1.3 to 1.6 (from strong inversion to weak inversion), μ is the carrier mobility, C_{ox} is the capacitance of the device's oxide per unit area, and ϕ_t is the thermal voltage of the device.

There are three levels of inversion: strong inversion, moderate inversion and weak inversion. These are defined by the relations found in Table 2.1. Within the weak inversion

Table 2.1: Inversion level definition

Region	i_f
Strong Inversion	> 10
Moderate Inversion	$0.1 - 10$
Weak Inversion	< 0.1

region, subthreshold operation takes place whenever the gate-to-source voltage of an NMOS transistor is less than its threshold voltage [7].

The gain of a single common-source transistor with an ideal load is well-known to be [8]

$$A = -g_m r_{ds} \tag{2.3}$$

where g_m is the small-signal transconductance from the gate voltage to the drain current of the transistor and r_{ds} is the small-signal drain-to-source resistance. In strong inversion, the transconductance is found to be

$$g_m = \sqrt{2\mu C_{ox} \kappa_S I_D W/L}. \tag{2.4}$$

κ_S accounts for the body effect and is given by

$$\kappa_S = \left(1 + \frac{\gamma}{2\sqrt{\phi_0 + V_{SB}}}\right)^{-1} \tag{2.5}$$

where γ is the body-effect coefficient, ϕ_0 depends on the doping and inversion levels of the transistor and V_{SB} is the source-to-bulk voltage. In weak inversion, the transconductance is

$$g_m = \frac{\kappa_S I_D}{\phi_t}. \tag{2.6}$$

In both weak and strong inversion, the small-signal drain-to-source resistance is

$$r_{ds} = \frac{V_A}{I_D} \tag{2.7}$$

where V_A represents the Early voltage of the transistor. It should be noted that this Early voltage is higher in strong inversion than it is in weak inversion, so we will refer to it as V_{AS} for strong inversion and V_{AW} for weak inversion. Equations (2.4) - (2.7) assume that the transistor is in saturation. If we substitute (2.4) and (2.7) into (2.3) for strong inversion, we obtain

$$A_{strong} = -\frac{V_{AS}\sqrt{2\mu C_{ox}\kappa_S W/L}}{\sqrt{I_D}}. \tag{2.8}$$

Substituting (2.6) and (2.7) into (2.3) for weak inversion yields

$$A_{weak} = -\frac{\kappa_S V_{AW}}{\phi_t}. \tag{2.9}$$

Comer et al. [9] have worked on finding transistor gains with respect to inversion level. In both the strong and weak inversion regions, r_{ds} is inversely proportional to the transistor's drain current. In weak inversion, g_m is proportional to the drain current, which means that the product $g_m r_{ds}$ is constant as shown in (2.9). This gain may increase slightly as the transistor gets near the moderate inversion region. In moderate inversion, this gain continues to increase as drain current increases and peaks at the upper edge of the moderate inversion region. When the transistor is in strong inversion, however, g_m is proportional to the square root of the drain current. Thus $g_m r_{ds}$ is inversely proportional to the square root of the drain current as shown in (2.8). The gain thus decreases as current increases further. Figure 2.1 shows an example of this gain for a single transistor ($W/L = 4\,\mu\text{m}/2\,\mu\text{m}$) [9].

2.2 Cascode Configurations

Figure 2.2 shows two types of cascode stages: composite and conventional. In the composite cascode configuration (shown in Figure 2.2(a)), M_1 and M_2 share the same DC gate voltage and AC input source. In the conventional cascode configuration (shown in Figure 2.2(b)), M_1 and M_2 may have different DC gate voltages and the AC input is only attached to the gate of M_1. The interested reader may consult [10, 11] for more information on cascode stages.

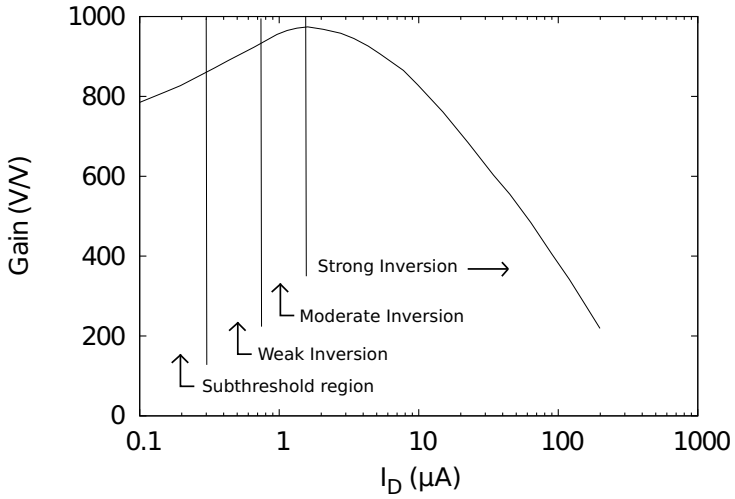
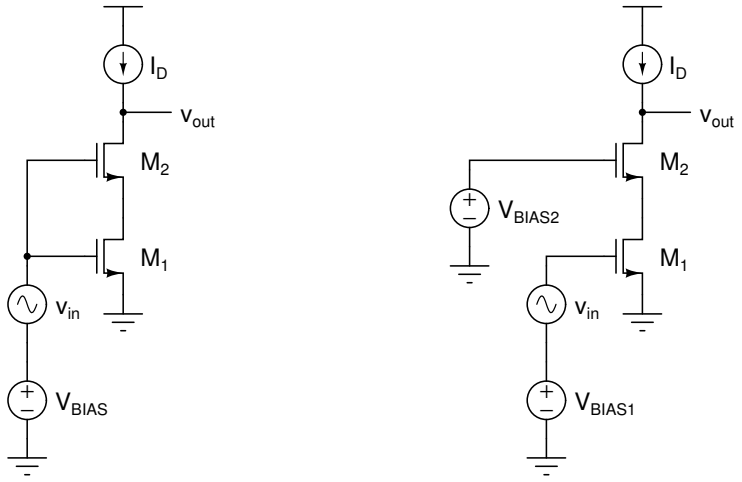


Figure 2.1: Gain of a transistor ($W/L = 4\,\mu\text{m}/2\,\mu\text{m}$) with respect to drain current



(a) Composite (b) Conventional

Figure 2.2: Types of cascode stages

Previous work increased the gains of composite cascode stages [4, 5]. This thesis extends the work to conventional cascodes and takes a step further by improving not only gains, but also gain-bandwidth products and gain-bandwidth/current figures.

The small-signal gain of the composite cascode circuit is found to be

$$A_{comp} = -\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2}) + g_{m2}g_{ds1}}{g_{ds1}g_{ds2} + G_L(g_{ds1} + g_{m2} + g_{s2} + g_{ds2})} \tag{2.10}$$

where g_m is the device transconductance from source-to-gate voltage to drain current, g_s is the transconductance from source-to-bulk voltage to drain current, g_{ds} is the admittance between the source and drain terminals, and G_L is the load admittance. The small-signal gain of the conventional cascode stage is found to be

$$A_{conv} = -\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2})}{g_{ds1}g_{ds2} + G_L(g_{ds1} + g_{m2} + g_{s2} + g_{ds2})}. \tag{2.11}$$

These equations are derived in Appendix A. Now if we assume that each of these stages has infinite load resistance ($G_L = 0$), then we can simplify (2.10) and (2.11) to be

$$A_{comp} = -\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2}) + g_{m2}g_{ds1}}{g_{ds1}g_{ds2}} \tag{2.12}$$

and

$$A_{conv} = -\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2})}{g_{ds1}g_{ds2}}, \tag{2.13}$$

respectively.

It would appear at first glance that composite cascode stages should have higher gain magnitude than conventional cascode circuits. This, however, is generally not the case because the composite cascode stage has less freedom in DC biasing. For example, in Figure 2.2(a), M_1 is often biased near the triode region to accommodate M_2 having the same gate voltage. As a result, the impedance level at the output and the transconductance of M_1 are lower than they otherwise would be – leading to reduced gain. The conventional cascode stage allows more freedom in DC biasing at the cost of an extra voltage source.

Chapter 3

Cascode Experiment

The Analog/Mixed Signal Research Group at Brigham Young University had previously done work on high gain composite cascode amplifiers [4, 5]. Li designed a high-gain (117 dB), moderate power (110 μW) op amp using the composite cascode stage. Singh et al. sought to reduce power consumption and designed a high-gain (113 dB), low power (21.3 μW) amplifier based on the composite cascode stage.

As noted in section 2.2, however, a conventional cascode stage has advantages over a composite cascode stage. This suggests that an operational amplifier with better performance could be designed if a conventional cascode stage is used instead. In order to find a good starting point for designing an amplifier based on a conventional cascode stage, we performed an experiment using AMI's 0.5 μm technology SPICE models.

Figure 3.1 shows a simple cascode stage that was used for SPICE simulations. In order to find gain and bandwidth trends for the cascode op amps, automated simulations that were performed iterated over the inversion coefficients for each device, V_{BDIFF}, and I_D. A 5 V power supply was used and V_{BIAS} was adjusted so that V_{OUT} was biased at 2.5 V for each simulation. V_{BDIFF} ranged from 0 V to 3 V in 0.1 V increments. I_D ranged exponentially from 0.1 μA to 10 μA with 2 samples per decade. The inversion coefficients (represented by i_f) varied exponentially from 0.003 to 300 with 2 samples per decade. A script written in the C programming language was used to call LTspiceIV and perform these simulations. The source code may be found in Appendix B.

The results of the simulations were stored into a text file that can be imported into a spreadsheet program. In all the tables that follow, I_D is in μA, V_{BDIFF} is in volts, GBW and BW are in Hz, and GBW/I_D is in Hz/μA. The transistor dimensions shown are in μm,

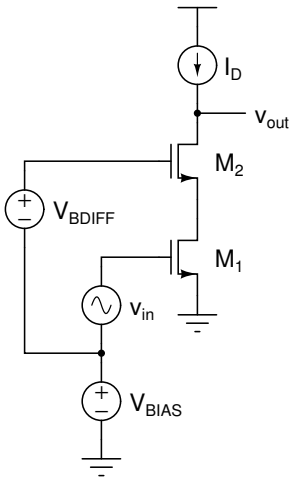


Figure 3.1: Cascode stage used for experiment

and are rounded to the nearest $0.1\,\mu$m. In the case where the dimensions exceed $1000\,\mu$m, only 4 significant figures are shown.

Table 3.1 shows the top 20 highest gain setups (in descending order) for the cascode stage. From these simulations, we have found that the highest gains are obtained by placing M_1 in the moderate inversion region and M_2 in the strong inversion region. Specifically, $i_{f1} = 3$ and i_{f2} ranging from 100–300 produced the highest gains. This is quite different from the results previously found [4, 5] for the composite cascode stage which suggested that M_1 would be in strong inversion and M_2 would be in weak inversion. Since the gain of a cascode configuration can be approximated by the product of individual common-source transistor gains, it makes sense that the highest gains would occur when both transistors are near the upper edge of moderate inversion. M_2 is further into the strong inversion region than initially expected, but this is due to the biasing differences found between the two transistors (including the body-effect of M_2). The median value for V_{BDIFF} was 2.1 V and I_D was $0.3\,\mu$A in all the cases. The bandwidth ranged from 58 Hz to 105 Hz.

Table 3.2 shows the top 20 highest gain results found with $V_{BDIFF} = 0\,\text{V}$. Here, low currents are represented. M_1 is in moderate/strong inversion, but M_2 is far in the weak inversion. These results are consistent with those found with the composite cascode configuration. The reason M_2 must be in weak inversion here is because both devices have their gates tied to the same voltage. If we place M_2 in the strong inversion region, M_1 is

Table 3.1: High gain results

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	Gain	BW	GBW	GBW/I_D
2.4	0.3	3	300	3.0/7.7	3.0/687.5	1.95E+006	6.37E+001	1.24E+008	4.14E+008
2.4	0.3	3	100	3.0/7.7	3.0/229.2	1.78E+006	7.63E+001	1.36E+008	4.53E+008
2.1	0.3	3	100	3.0/7.7	3.0/229.2	1.76E+006	7.98E+001	1.41E+008	4.68E+008
1.9	0.3	3	100	3.0/7.7	3.0/229.2	1.76E+006	7.98E+001	1.40E+008	4.68E+008
1.8	0.3	3	100	3.0/7.7	3.0/229.2	1.71E+006	7.98E+001	1.36E+008	4.54E+008
1.7	0.3	3	100	3.0/7.7	3.0/229.2	1.66E+006	8.35E+001	1.38E+008	4.61E+008
1.6	0.3	3	100	3.0/7.7	3.0/229.2	1.63E+006	8.35E+001	1.36E+008	4.55E+008
2.4	0.3	10	300	3.0/22.9	3.0/687.5	1.62E+006	4.86E+001	7.84E+007	2.61E+008
2.0	0.3	3	100	3.0/7.7	3.0/229.2	1.60E+006	8.35E+001	1.34E+008	4.46E+008
2.2	0.3	3	300	3.0/7.7	3.0/687.5	1.56E+006	6.97E+001	1.09E+008	3.62E+008
2.2	0.3	10	100	3.0/22.9	3.0/229.2	1.55E+006	5.82E+001	9.00E+007	3.00E+008
2.4	0.3	10	100	3.0/22.9	3.0/229.2	1.53E+006	5.82E+001	8.89E+007	2.96E+008
2.0	0.3	3	30	3.0/7.7	3.0/68.8	1.52E+006	9.56E+001	1.45E+008	4.85E+008
2.2	0.3	1	300	3.0/2.6	3.0/687.5	1.51E+006	1.05E+002	1.58E+008	5.28E+008
2.6	0.3	3	30	3.0/7.7	3.0/68.8	1.50E+006	1.00E+002	1.50E+008	5.00E+008
2.1	0.3	10	100	3.0/22.9	3.0/229.2	1.50E+006	5.82E+001	8.73E+007	2.91E+008
1.8	0.3	3	30	3.0/7.7	3.0/68.8	1.50E+006	1.00E+002	1.50E+008	4.99E+008
2.2	0.3	3	100	3.0/7.7	3.0/229.2	1.50E+006	8.73E+001	1.31E+008	4.35E+008
1.9	0.3	10	100	3.0/22.9	3.0/229.2	1.49E+006	5.82E+001	8.67E+007	2.89E+008
2.3	0.3	10	100	3.0/22.9	3.0/229.2	1.49E+006	5.82E+001	8.64E+007	2.88E+008

forced into the triode region of operation. This prevents the gains from being as high as they could be if we did not restrict V_{BDIFF}.

We can gain more insight in how increasing i_{f2} reduces the gain of the stage if we observe how the drain-to-source voltage of M_1 (v_{ds1}) is affected. Table 3.3 illustrates what happens when i_{f2} increases while leaving other variables constant. It is seen that v_{ds1} decreases until it is below v_{dsat1}, the saturation voltage of M_1. Thus M_1 enters the triode operating region – leading to an overall gain decrease. This happens because with reduced v_{ds1}, M_1 must have a higher gate voltage in order to maintain the same current. However, if V_{BDIFF} is at a higher value (say 1.8 V), then M_1 has more voltage headroom. This is illustrated by Table 3.4, where increasing i_{f2} still reduces v_{ds1}, but never below v_{dsat1}. Thus M_1 is still in the active operating region. In fact, overall gain of the cascode stage increases significantly since M_2 moves toward a more favorable operating point. Figure 3.2 graphically

Table 3.2: High gain results with $V_{BDIFF} = 0\,\mathrm{V}$

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	Gain	BW	GBW	GBW/I_D
0.0	0.1	10	0.003	3.0/68.8	106.4/0.9	1.29E+005	9.14E+000	1.18E+006	1.18E+007
0.0	0.1	3	0.003	3.0/23.0	106.4/0.9	1.26E+005	1.44E+001	1.80E+006	1.80E+007
0.0	0.1	30	0.003	3.0/206.3	106.4/0.9	1.08E+005	6.37E+000	6.85E+005	6.85E+006
0.0	0.3	10	0.003	3.0/22.9	319.1/0.9	1.04E+005	1.15E+001	1.19E+006	3.98E+006
0.0	0.1	3	0.01	3.0/23.0	31.9/0.9	1.04E+005	5.56E+001	5.75E+006	5.75E+007
0.0	0.1	10	0.01	3.0/68.8	31.9/0.9	1.03E+005	3.70E+001	3.80E+006	3.80E+007
0.0	0.3	30	0.003	3.0/68.8	319.1/0.9	1.02E+005	6.66E+000	6.82E+005	2.27E+006
0.0	0.3	100	0.003	3.0/229.2	319.1/0.9	9.19E+004	4.24E+000	3.90E+005	1.30E+006
0.0	0.1	1	0.003	3.0/7.7	106.4/0.9	9.10E+004	2.58E+001	2.35E+006	2.35E+007
0.0	0.3	10	0.01	3.0/22.9	95.7/0.9	8.86E+004	4.44E+001	3.93E+006	1.31E+007
0.0	0.3	30	0.01	3.0/68.8	95.7/0.9	8.54E+004	2.70E+001	2.31E+006	7.69E+006
0.0	0.3	3	0.003	3.0/7.7	319.1/0.9	8.41E+004	2.15E+001	1.81E+006	6.04E+006
0.0	0.1	30	0.01	3.0/206.3	31.9/0.9	8.40E+004	2.70E+001	2.27E+006	2.27E+007
0.0	0.1	100	0.003	3.0/687.5	106.4/0.9	8.19E+004	4.64E+000	3.80E+005	3.80E+006
0.0	0.3	300	0.003	3.0/687.5	319.1/0.9	8.02E+004	2.70E+000	2.17E+005	7.22E+005
0.0	0.1	1	0.01	3.0/7.7	31.9/0.9	7.65E+004	1.00E+002	7.65E+006	7.65E+007
0.0	0.3	100	0.01	3.0/229.2	95.7/0.9	7.62E+004	1.64E+001	1.25E+006	4.17E+006
0.0	1	100	0.003	3.0/68.8	1064/0.9	7.56E+004	5.08E+000	3.84E+005	3.84E+005
0.0	1	300	0.003	3.0/206.3	1064/0.9	7.44E+004	2.96E+000	2.20E+005	2.20E+005
0.0	0.3	3	0.01	3.0/7.7	95.7/0.9	7.33E+004	8.35E+001	6.12E+006	2.04E+007

shows how v_{ds1} and v_{dsat1} change with an increase in i_{f2}. Figure 3.2(a) shows the case where $V_{BDIFF} = 0\,\mathrm{V}$ and Figure 3.2(b) shows the case where $V_{BDIFF} = 1.8\,\mathrm{V}$.

One concern engineers may have in these results is that some of the shown transistor dimensions may not be available under certain technologies. If such is the case for the technology being used, then the designer may filter the results to obtain the relevant values. For example, Table 3.5 shows the top 20 high gain results obtained when the $W < 300\,\mu\mathrm{m}$ and $L < 90\,\mu\mathrm{m}$ for each transistor.

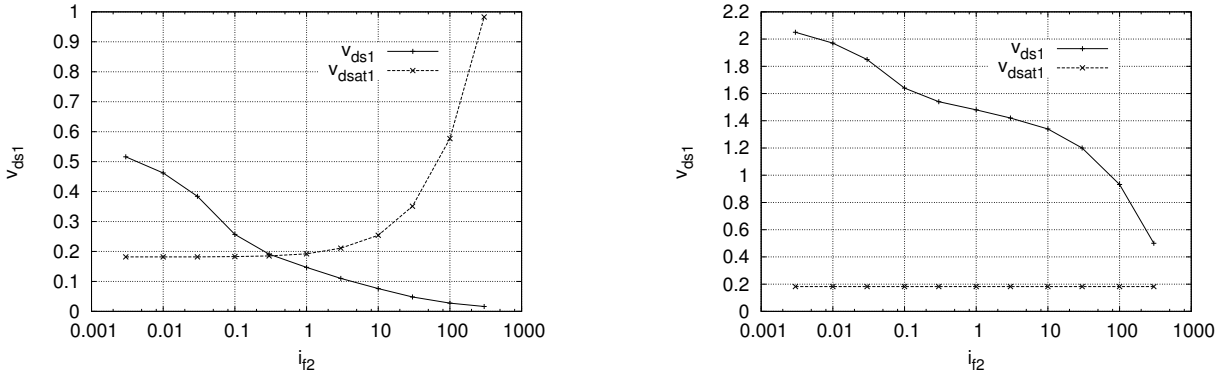
Table 3.6 shows the top 20 highest gain-bandwidth products found. In all cases, $I_D = 10\,\mu\mathrm{A}$. The median value for V_{BDIFF} was $1.5\,\mathrm{V}$. Here, i_{f1} ranged from 0.1 to 0.3 and i_{f2} ranged from 30 to 100. Thus, placing M_1 in moderate inversion and M_2 in strong inversion while using more power leads to high gain-bandwidth products.

Table 3.3: Increasing i_{f2} while holding other variables constant with $V_{BDIFF} = 0\,\mathrm{V}$

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	v_{ds1}	v_{dsat1}	Gain	BW
0.0	0.1	10	0.003	3.0/68.8	106.4/0.9	0.5160	0.1820	1.29E+005	9.14E+000
0.0	0.1	10	0.01	3.0/68.8	31.9/0.9	0.4620	0.1820	1.03E+005	3.70E+001
0.0	0.1	10	0.03	3.0/68.8	10.6/0.9	0.3840	0.1820	6.09E+004	1.80E+002
0.0	0.1	10	0.1	3.0/68.8	3.5/0.9	0.2570	0.1830	1.14E+004	2.47E+003
0.0	0.1	10	0.3	3.0/68.8	3.0/2.3	0.1910	0.1850	8.89E+003	3.23E+003
0.0	0.1	10	1	3.0/68.8	3.0/7.7	0.1470	0.1920	3.81E+003	6.09E+003
0.0	0.1	10	3	3.0/68.8	3.0/23.0	0.1100	0.2110	2.11E+003	6.97E+003
0.0	0.1	10	10	3.0/68.8	3.0/68.8	0.0762	0.2540	1.18E+003	6.37E+003
0.0	0.1	10	30	3.0/68.8	3.0/206.3	0.0482	0.3510	6.05E+002	3.88E+003
0.0	0.1	10	100	3.0/68.8	3.0/687.5	0.0274	0.5770	2.76E+002	1.72E+003
0.0	0.1	10	300	3.0/68.8	3.0/2063	0.0162	0.9830	1.11E+002	8.35E+002

Table 3.4: Increasing i_{f2} while holding other variables constant with a higher value of V_{BDIFF}

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	v_{ds1}	v_{dsat1}	Gain	BW
1.8	0.1	10	0.003	3.0/68.8	106.4/0.9	2.0500	0.1820	1.81E+005	6.37E+000
1.8	0.1	10	0.01	3.0/68.8	31.9/0.9	1.9700	0.1820	1.79E+005	2.15E+001
1.8	0.1	10	0.03	3.0/68.8	10.6/0.9	1.8500	0.1820	2.11E+005	5.08E+001
1.8	0.1	10	0.1	3.0/68.8	3.5/0.9	1.6400	0.1820	2.64E+005	1.05E+002
1.8	0.1	10	0.3	3.0/68.8	3.0/2.3	1.5400	0.1820	5.57E+005	5.82E+001
1.8	0.1	10	1	3.0/68.8	3.0/7.7	1.4800	0.1820	6.16E+005	5.08E+001
1.8	0.1	10	3	3.0/68.8	3.0/23.0	1.4200	0.1820	6.68E+005	4.64E+001
1.8	0.1	10	10	3.0/68.8	3.0/68.8	1.3400	0.1820	7.02E+005	4.44E+001
1.8	0.1	10	30	3.0/68.8	3.0/206.3	1.2000	0.1820	6.99E+005	4.05E+001
1.8	0.1	10	100	3.0/68.8	3.0/687.5	0.9320	0.1820	7.30E+005	3.70E+001
1.8	0.1	10	300	3.0/68.8	3.0/2063	0.5000	0.1820	6.60E+005	2.96E+001



(a) $V_{BDIFF} = 0\,\mathrm{V}$ (b) $V_{BDIFF} = 1.8\,\mathrm{V}$

Figure 3.2: Impact that increasing i_{f2} has on v_{ds1} and v_{dsat1}

Table 3.5: High gain results with $W < 300\,\mu$m and $L < 90\,\mu$m for the transistors

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	Gain	BW	GBW	GBW/I_D
2.0	0.3	3	30	3.0/7.7	3.0/68.8	1.52E+006	9.56E+001	1.45E+008	4.85E+008
2.6	0.3	3	30	3.0/7.7	3.0/68.8	1.50E+006	1.00E+002	1.50E+008	5.00E+008
1.8	0.3	3	30	3.0/7.7	3.0/68.8	1.50E+006	1.00E+002	1.50E+008	4.99E+008
1.6	0.3	3	30	3.0/7.7	3.0/68.8	1.45E+006	1.00E+002	1.45E+008	4.84E+008
1.7	0.3	3	30	3.0/7.7	3.0/68.8	1.44E+006	1.00E+002	1.44E+008	4.81E+008
1.5	0.3	3	30	3.0/7.7	3.0/68.8	1.44E+006	1.00E+002	1.44E+008	4.80E+008
2.3	0.3	3	30	3.0/7.7	3.0/68.8	1.44E+006	1.00E+002	1.44E+008	4.78E+008
1.9	0.3	3	30	3.0/7.7	3.0/68.8	1.43E+006	1.00E+002	1.43E+008	4.77E+008
1.4	0.3	3	30	3.0/7.7	3.0/68.8	1.40E+006	1.00E+002	1.40E+008	4.66E+008
1.3	0.3	3	30	3.0/7.7	3.0/68.8	1.38E+006	1.09E+002	1.51E+008	5.02E+008
2.2	0.3	10	30	3.0/22.9	3.0/68.8	1.37E+006	6.97E+001	9.54E+007	3.18E+008
2.3	0.3	10	30	3.0/22.9	3.0/68.8	1.36E+006	6.97E+001	9.50E+007	3.17E+008
1.6	0.3	10	30	3.0/22.9	3.0/68.8	1.36E+006	6.97E+001	9.48E+007	3.16E+008
2.4	0.3	1	30	3.0/2.6	3.0/68.8	1.35E+006	1.44E+002	1.94E+008	6.46E+008
1.5	0.3	10	30	3.0/22.9	3.0/68.8	1.34E+006	6.97E+001	9.36E+007	3.12E+008
2.1	0.3	1	30	3.0/2.6	3.0/68.8	1.33E+006	1.44E+002	1.91E+008	6.38E+008
1.8	0.3	10	30	3.0/22.9	3.0/68.8	1.33E+006	6.97E+001	9.28E+007	3.09E+008
2.0	0.3	10	30	3.0/22.9	3.0/68.8	1.32E+006	6.97E+001	9.21E+007	3.07E+008
2.3	0.3	1	30	3.0/2.6	3.0/68.8	1.32E+006	1.44E+002	1.90E+008	6.32E+008
2.7	0.3	1	30	3.0/2.6	3.0/68.8	1.32E+006	1.44E+002	1.90E+008	6.32E+008

Table 3.7 shows the top 20 highest gain-bandwidth/current results. In these results, $I_D = 0.1\mu$A. This suggests that increasing power for the purpose of increasing the gain-bandwidth product has diminishing returns. V_{BDIFF} had a range of values slightly higher than those found in the highest gain-bandwidth results, with a median value of 2.1 V. Also, $i_{f1} = 0.003$ for all of these particular results while i_{f2} ranges from 0.3 to 3. Here, placing M_1 in the weak inversion region and M_2 in moderate inversion led to the highest gain-bandwidth/current results over the simulated parameter ranges. The highest gain-bandwidth results at each value of I_D show that i_{f1} tends to increase linearly with I_D. This suggests that for ultra low-power circuits, the highest gain-bandwidth results occur with M_1 in weak inversion.

Figure 3.3 summarizes the experimental results. In the next chapter, the design of an ultra low power amplifier that emphasizes gain is detailed. Though some of the settings are

Table 3.6: High gain-bandwidth results

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	Gain	BW	GBW	GBW/I_D
1.5	10	0.3	30	117.4/0.9	3.0/2.1	7.41E+004	1.00E+005	7.41E+009	7.41E+008
1.3	10	0.1	30	352.1/0.9	3.0/2.1	7.08E+004	1.05E+005	7.41E+009	7.41E+008
1.6	10	0.1	30	352.1/0.9	3.0/2.1	7.39E+004	1.00E+005	7.39E+009	7.39E+008
1.0	10	0.1	30	352.1/0.9	3.0/2.1	5.36E+004	1.37E+005	7.35E+009	7.35E+008
1.4	10	0.3	30	117.4/0.9	3.0/2.1	7.35E+004	1.00E+005	7.35E+009	7.35E+008
1.0	10	0.3	30	117.4/0.9	3.0/2.1	5.56E+004	1.31E+005	7.29E+009	7.29E+008
1.8	10	0.3	30	117.4/0.9	3.0/2.1	6.66E+004	1.09E+005	7.29E+009	7.29E+008
1.5	10	0.1	30	352.1/0.9	3.0/2.1	7.28E+004	1.00E+005	7.28E+009	7.28E+008
1.6	10	0.1	100	352.1/0.9	3.0/6.9	7.61E+004	9.56E+004	7.27E+009	7.27E+008
1.9	10	0.3	30	117.4/0.9	3.0/2.1	6.65E+004	1.09E+005	7.27E+009	7.27E+008
1.6	10	0.3	30	117.4/0.9	3.0/2.1	7.26E+004	1.00E+005	7.26E+009	7.26E+008
1.4	10	0.1	30	352.1/0.9	3.0/2.1	7.26E+004	1.00E+005	7.26E+009	7.26E+008
2.0	10	0.3	30	117.4/0.9	3.0/2.1	6.32E+004	1.15E+005	7.23E+009	7.23E+008
1.7	10	0.3	30	117.4/0.9	3.0/2.1	6.91E+004	1.05E+005	7.23E+009	7.23E+008
1.9	10	0.1	100	352.1/0.9	3.0/6.9	7.90E+004	9.14E+004	7.22E+009	7.22E+008
1.1	10	0.1	30	352.1/0.9	3.0/2.1	6.30E+004	1.15E+005	7.21E+009	7.21E+008
1.4	10	0.1	100	352.1/0.9	3.0/6.9	6.29E+004	1.15E+005	7.20E+009	7.20E+008
1.6	10	0.3	100	117.4/0.9	3.0/6.9	7.52E+004	9.56E+004	7.19E+009	7.19E+008
1.1	10	0.3	30	117.4/0.9	3.0/2.1	6.28E+004	1.15E+005	7.19E+009	7.19E+008
0.9	10	0.1	30	352.1/0.9	3.0/2.1	3.81E+004	1.88E+005	7.17E+009	7.17E+008

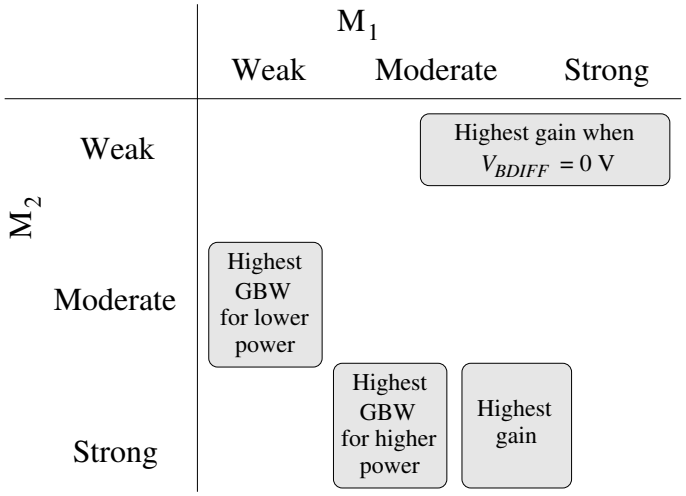


Figure 3.3: Experimental results summary

Table 3.7: High gain-bandwidth/current results

V_{BDIFF}	I_D	i_{f1}	i_{f2}	W_1/L_1	W_2/L_2	Gain	BW	GBW	GBW/I_D
2.5	0.1	0.003	1	106.4/0.9	3.0/7.7	1.62E+005	6.66E+002	1.08E+008	1.08E+009
1.9	0.1	0.003	1	106.4/0.9	3.0/7.7	1.69E+005	6.37E+002	1.08E+008	1.08E+009
2.9	0.1	0.003	3	106.4/0.9	3.0/23.0	2.32E+005	4.64E+002	1.08E+008	1.08E+009
1.7	0.1	0.003	1	106.4/0.9	3.0/7.7	1.69E+005	6.37E+002	1.07E+008	1.07E+009
2.0	0.1	0.003	1	106.4/0.9	3.0/7.7	1.69E+005	6.37E+002	1.07E+008	1.07E+009
1.3	0.1	0.003	1	106.4/0.9	3.0/7.7	1.61E+005	6.66E+002	1.07E+008	1.07E+009
1.8	0.1	0.003	1	106.4/0.9	3.0/7.7	1.68E+005	6.37E+002	1.07E+008	1.07E+009
2.6	0.1	0.003	3	106.4/0.9	3.0/23.0	2.41E+005	4.44E+002	1.07E+008	1.07E+009
1.6	0.1	0.003	1	106.4/0.9	3.0/7.7	1.68E+005	6.37E+002	1.07E+008	1.07E+009
2.1	0.1	0.003	1	106.4/0.9	3.0/7.7	1.68E+005	6.37E+002	1.07E+008	1.07E+009
2.7	0.1	0.003	1	106.4/0.9	3.0/7.7	1.53E+005	6.97E+002	1.07E+008	1.07E+009
1.5	0.1	0.003	3	106.4/0.9	3.0/23.0	2.40E+005	4.44E+002	1.07E+008	1.07E+009
2.6	0.1	0.003	1	106.4/0.9	3.0/7.7	1.60E+005	6.66E+002	1.07E+008	1.07E+009
2.7	0.1	0.003	3	106.4/0.9	3.0/23.0	2.40E+005	4.44E+002	1.06E+008	1.06E+009
2.2	0.1	0.003	1	106.4/0.9	3.0/7.7	1.67E+005	6.37E+002	1.06E+008	1.06E+009
2.8	0.1	0.003	1	106.4/0.9	3.0/7.7	1.52E+005	6.97E+002	1.06E+008	1.06E+009
1.1	0.1	0.003	3	106.4/0.9	3.0/23.0	2.09E+005	5.08E+002	1.06E+008	1.06E+009
2.1	0.1	0.003	3	106.4/0.9	3.0/23.0	2.50E+005	4.24E+002	1.06E+008	1.06E+009
1.5	0.1	0.003	1	106.4/0.9	3.0/7.7	1.67E+005	6.37E+002	1.06E+008	1.06E+009
2.4	0.1	0.003	0.3	106.4/0.9	3.0/2.3	9.69E+004	1.09E+003	1.06E+008	1.06E+009

different (such as power source being $\pm 1.5\,\mathrm{V}$ rather than ranging from $0\,\mathrm{V}$ to $5\,\mathrm{V}$), many of the principles remain the same.

Chapter 4

Amplifier Design

After completing the experiment, we designed a 2-stage op amp that maximizes gain while consuming little power. The final design of the op amp is shown in Figure 4.1. The power supply was chosen to be 1.5 V in both directions. This is a common supply voltage for low power circuits. For this amplifier, we restricted the dimensions of the transistors so that the minimum width is 6 μm and the maximum length is 20 μm in order to make this amplifier more flexible to different technologies.

The first stage uses a differential, conventional cascode configuration with a wide-swing, high-impedance current mirror. A current of 100 nA was chosen for each branch in this stage. This is a reasonable choice of current for low power circuits, and is near the minimum allowed for IC technologies. M_1 and M_2 are in the moderate inversion region while M_3 and M_4 are near the upper edge of moderate inversion. V_{BDIFF} for this stage is 0.8 V, and is provided by M_{15} and M_{16}. This value for V_{BDIFF} was selected because we only have 3 V between the supplies. $M_5 - M_8$ form the current mirror load for this stage and are built for high-impedance. The capacitors C_1 and C_2, as explained later, provide extra compensation for the op amp. A cascode current mirror ($M_{11} - M_{14}$) provides the impedance necessary for the gain of this stage. M_{17} provides a steady gate voltage for M_7 and M_8.

The second stage is a common-source gain stage consisting of M_9 and M_{10}. In order to allow for greater bandwidth, we designed this stage to have 400 nA of current. This stage was designed to have lower output impedance than the first and to have a low DC output offset voltage. Additionally, this stage has a fairly wide swing since it doesn't have cascoded transistors.

The capacitors $C_1 - C_3$ and the resistor R_1 are used to compensate the op amp. C_3 and R_1 give the familiar lead compensation that is common in op amp design. Lead compensation

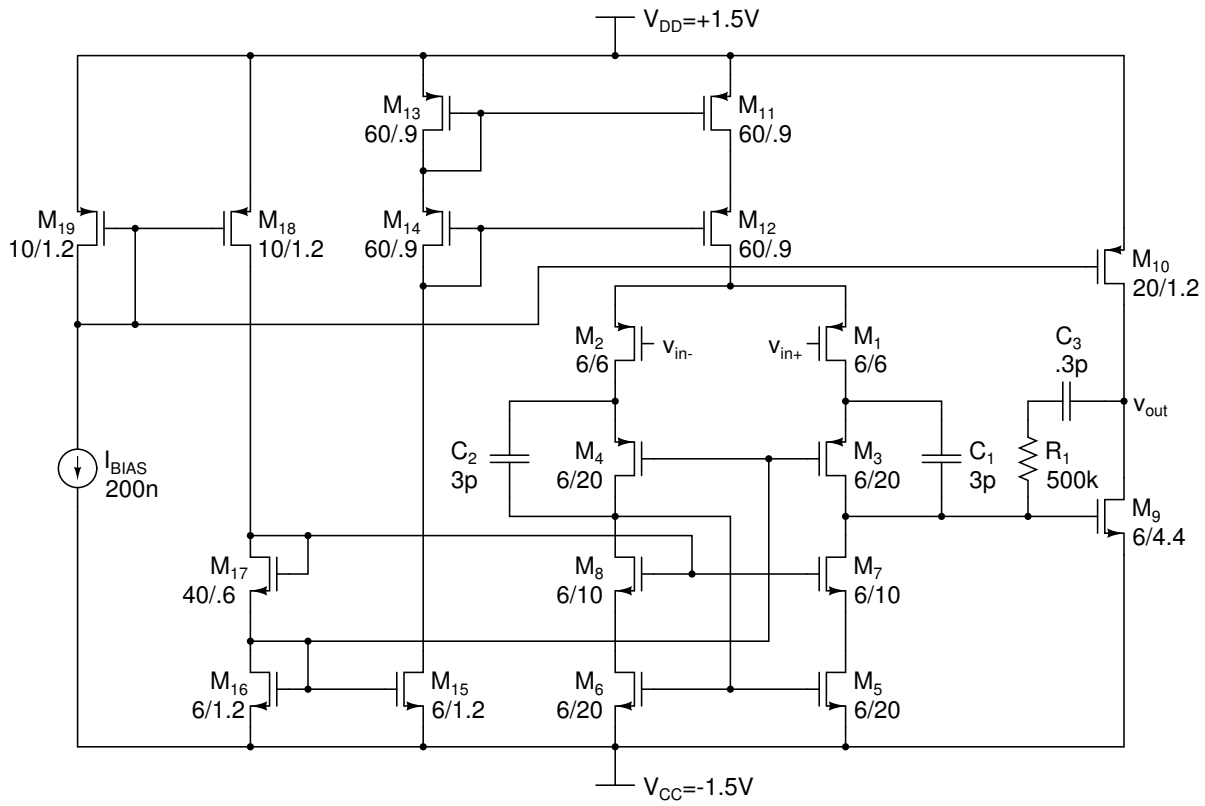


Figure 4.1: Final op amp schematic

is used because it provides more phase margin than dominant pole compensation, thus allowing for less bandwidth degradation. In this case, an actual resistor is used for R_1 instead of a transistor because a transistor in the triode region wouldn't provide enough small-signal resistance. C_3 has a rather small value and would thus requires a rather large series resistance in order to shift a pole and provide a zero at the proper frequencies. Capacitors C_1 and C_2 provide extra phase margin by reducing the impedance (and thus the gain) of the first stage near the unity-gain frequency of the op amp.

The biggest drawback to including capacitors and a resistor in the design is chip area. Figure 4.2 shows a possible layout for the op amp. We can see the relative sizes of the capacitors and the resistor. From this layout, it is clear that the capacitors (totaling 6.3 pF) occupy the most chip area. The resistor (500 kΩ) also occupies a significant portion of the chip area. It may be possible to shave off some capacitance and resistance from the design, but this will lead to reduced phase margin.

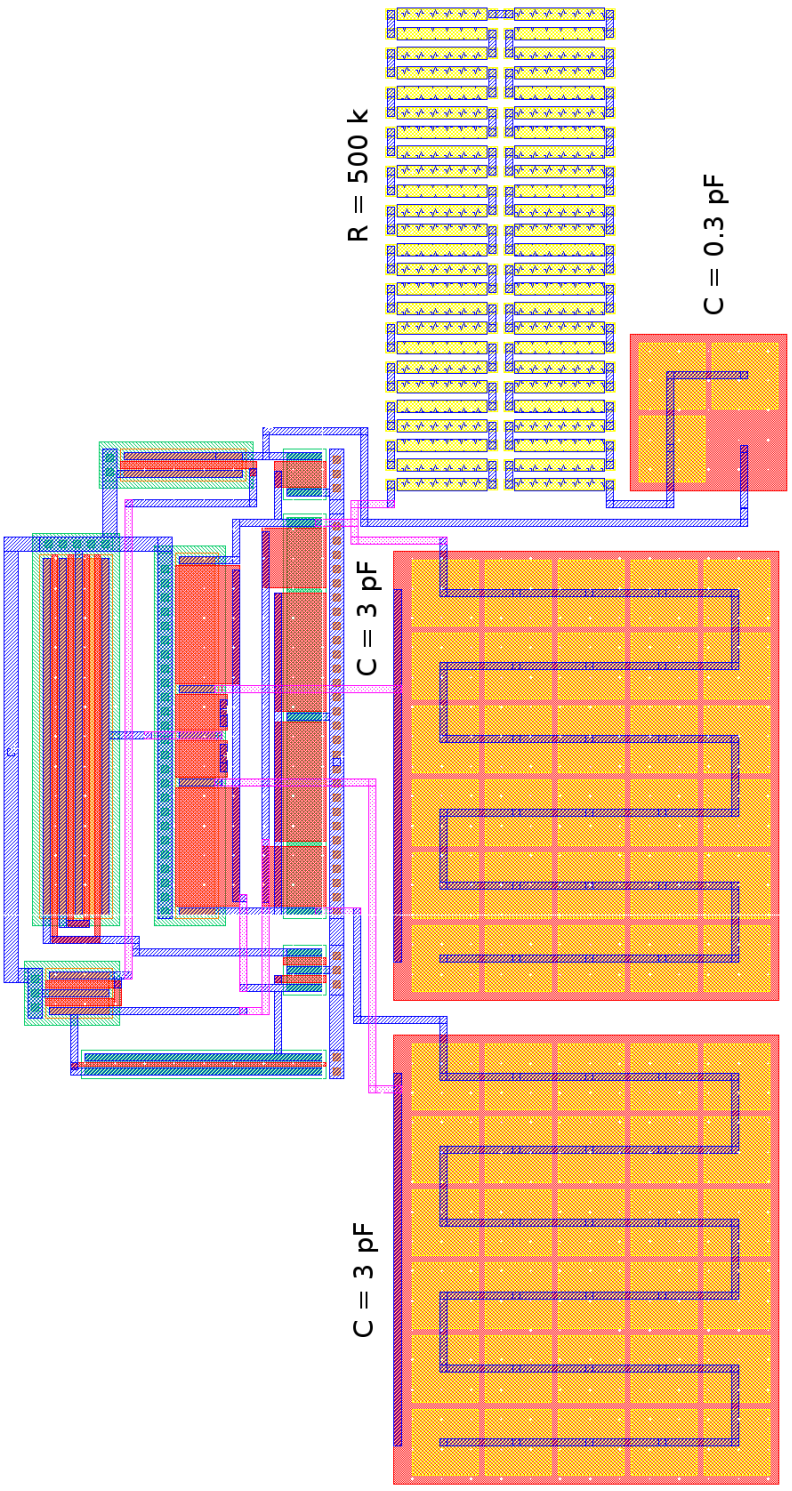


Figure 4.2: Op amp layout demonstrating relative component sizes

Chapter 5

Simulation Results

The amplifier of Figure 4.1 was simulated with a 0.5 pF load capacitor in Cadence. This was done using AMI 0.5 μm technology.

5.1 DC Offset and Output Range

The DC offset of an op amp is usually defined in one of two ways:

1. DC offset taken at the input is defined as the voltage V_{IOS} that must be applied between the op amp's inputs in order to produce an output voltage of 0 V;

2. DC offset taken at the output is defined as the voltage V_{OS} that occurs at the output when the inputs of the op amp are both at 0 V.

In this work, we use the output offset V_{OS} of the op amp.

Figure 5.1 shows the simulation setup used for measuring the DC offset and output range of the amplifier. Figure 5.2 shows the DC simulation output. The DC offset at the output is found to be 8.7 mV and the output range is nearly rail-to-rail.

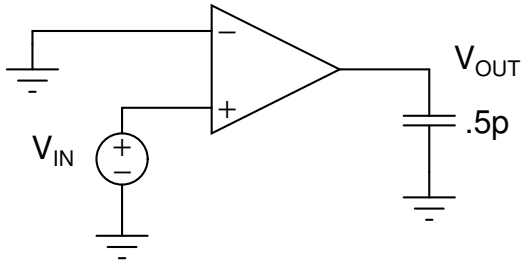


Figure 5.1: DC simulation setup

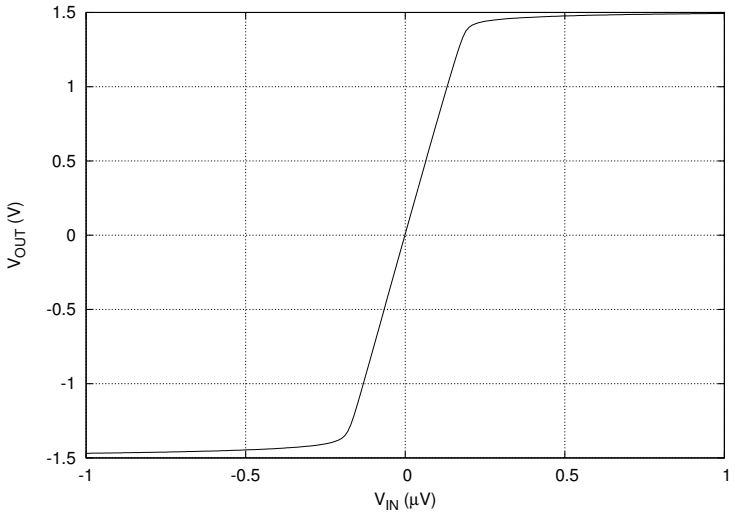


Figure 5.2: DC simulation results of op amp in Figure 4.1

5.2 Gain, Bandwidth and Phase Margin

The differential gain of an amplifier is defined as the magnitude ratio of its output voltage over the difference between the input voltage sources. In other words, the differential gain A_d is defined as

$$A_d = \frac{V_o}{(V_+ - V_-)} \tag{5.1}$$

where V_o is the output voltage and V_+ and V_- are the voltages at the positive and negative inputs of the op amp.

The bandwidth of a low-pass amplifier is defined as the frequency in which the output AC power is half of its maximum. In other words, the bandwidth of an amplifier is described by the frequency f_2 such that

$$|A_d(f_2)| = \frac{|A_{d-max}|}{\sqrt{2}}. \tag{5.2}$$

The phase margin (PM) of a low-pass amplifier is defined as

$$\text{PM} = \angle A_d(f_0) + 180^\circ \tag{5.3}$$

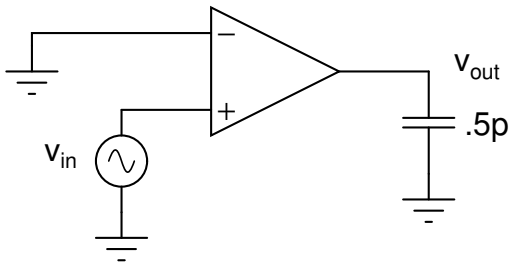


Figure 5.3: Simulation setup for measuring gain and bandwidth of op amp in Figure 4.1

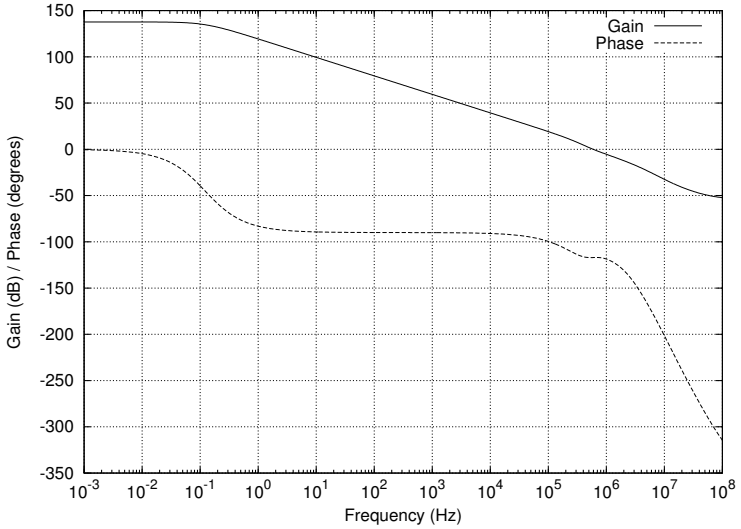


Figure 5.4: AC simulation results of op amp in Figure 4.1

where $\angle A_d$ is the phase of the amplifier's gain in degrees and f_0 is the frequency at which $|A_d| = 1$.

Figure 5.4 displays the AC simulation results. The differential gain of the amplifier at low frequencies is 137.7 dB. The gain of the first stage alone is 101.8 dB (123 kV/V). The bandwidth is found to be 0.118 Hz. The unity-gain frequency is about 600 kHz. The phase margin is 65°.

5.3 Input-referred Noise

Noise is typically measured in terms of a spectral density as a function of frequency such that noise power over a band of frequencies is calculated

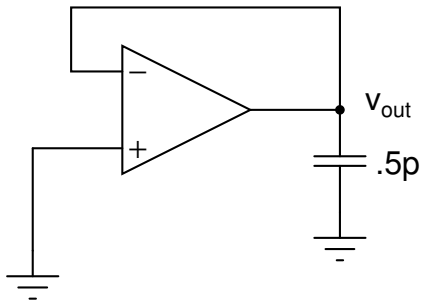


Figure 5.5: Simulation setup for measuring input-referred noise

$$v_{n(rms)}^2 = \int_{f_1}^{f_2} v_n^2(f) df \tag{5.4}$$

where f_1 and f_2 denote the band of frequencies of interest and $v_n^2(f)$ is the noise power density at frequency f. In order to find the total noise power over all frequencies, simply let $f_1 = 0$ and $f_2 \to +\infty$.

The simulation program reports the root spectral density of the noise at the output, which is simply $v_{no}(f)$. Input-referred noise is found by dividing the root spectral density taken at the output by the gain of the amplifier at each frequency so that

$$v_{ni}(f) = \frac{v_{no}(f)}{|A(f)|}. \tag{5.5}$$

Figure 5.5 shows the simulation setup for measuring input-referred noise. Since this op amp is in unity-gain configuration, input-referred noise can be measured by looking at the output. Figure 5.6 shows the resulting root spectral density of noise as a function of frequency. At lower frequencies, this noise density is measured to be $175.3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The noise density peaks at 800 kHz with a value of $869.3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This frequency is close to the unity-gain frequency of the amplifier.

5.4 Power Dissipation

Instantaneous power in electronic circuits is defined as

$$P = VI \tag{5.6}$$

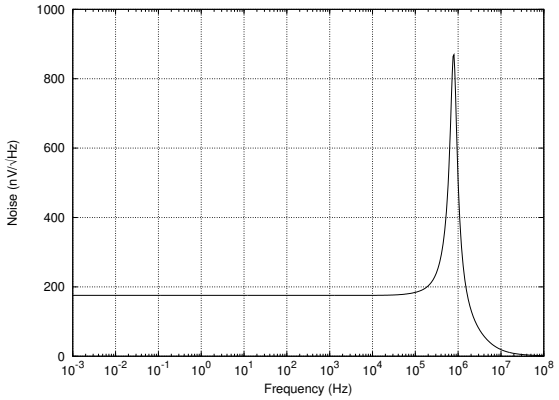


Figure 5.6: Noise root spectral density of op amp in Figure 4.1

where V is voltage drop in the current's direction and I is magnitude of that current. Engineers are typically more interested in average power. In the case of DC power, the magnitude of average power is the same as instantaneous power.

In the op amp of Figure 4.1, the current drawn from the power supplies is $1.449\,\mu$A. Since the total voltage drop of the supplies is $3\,$V, the power dissipation is $4.347\,\mu$W.

5.5 Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) of an op amp is defined as the ratio of change in the supply voltage to the change in input voltage required to offset that change. In other words,

$$\text{PSRR} = \frac{\Delta V_{supply}}{\Delta V_{IOS}}. \tag{5.7}$$

Figure 5.7 shows how to measure the PSRR of an op amp. Since the op amp is in unity-gain configuration, the output voltage is equivalent to the input voltage. Thus the resulting input voltage can be measured directly by inspecting the output. Figure 5.8 shows the results found from simulation. The PSRR is found to be $132.1\,$dB at low frequencies.

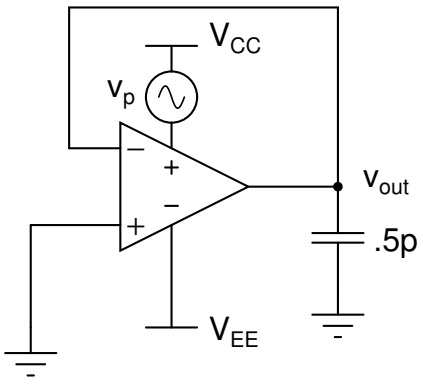


Figure 5.7: Simulation setup for measuring PSRR

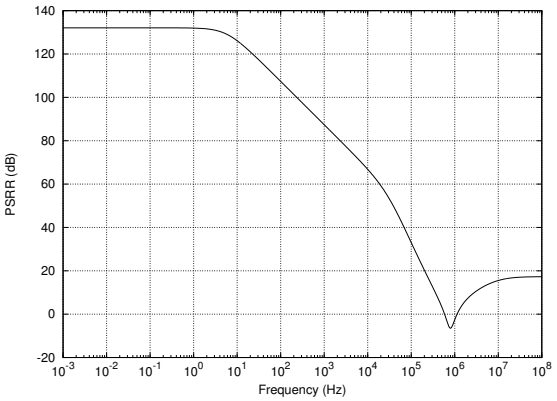


Figure 5.8: PSRR simulation results of the op amp in Figure 4.1

5.6 Common-mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an op amp is defined as the ratio of powers of the differential gain over the common-mode gain. The common-mode gain A_{cm} is defined as

$$A_{cm} = \frac{V_o}{\frac{1}{2}(V_+ + V_-)} \tag{5.8}$$

with the same variable definitions as described in defining A_d, the differential voltage of the amplifier. The CMRR of the op amp is computed

$$\text{CMRR} = 10 \log_{10} \left(\frac{A_d}{A_{cm}} \right)^2 . \tag{5.9}$$

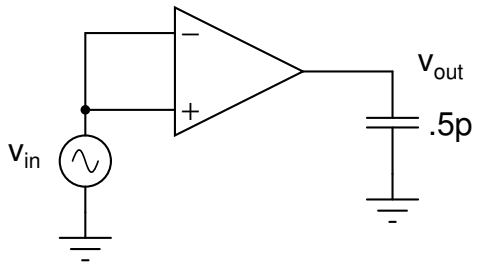


Figure 5.9: Simulation setup for measuring common-mode gain

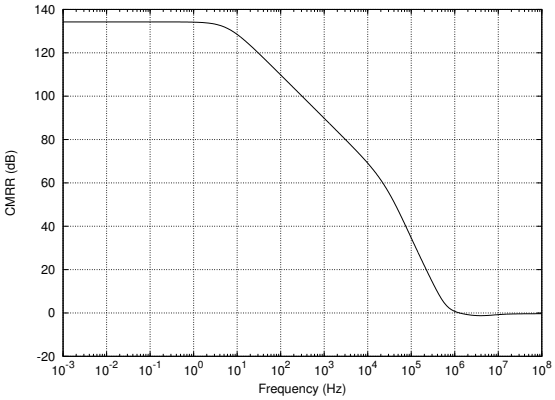


Figure 5.10: CMRR simulation results for op amp in Figure 4.1

Figure 5.9 shows the configuration used for measuring the common-mode gain of the op amp. The AC source is tied to both inputs of the op amp and the gain is found at v_{out}. The AC differential gain of the op amp is then divided by this gain at each frequency (both simulations ran over the same frequencies with 51 points per decade). Figure 5.10 shows the resulting CMRR of the amplifier. The CMRR is found to be 134.3 dB at low frequencies.

5.7 Slew Rate

The slew rate of an op amp is defined as the maximum rate of change in the output voltage. Thus the slew rate (SR) is computed as

$$\mathrm{SR} = \max \left| \frac{dv_{out}(t)}{dt} \right|. \tag{5.10}$$

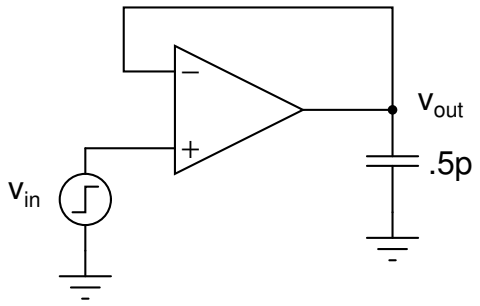


Figure 5.11: Simulation setup for finding slew rate

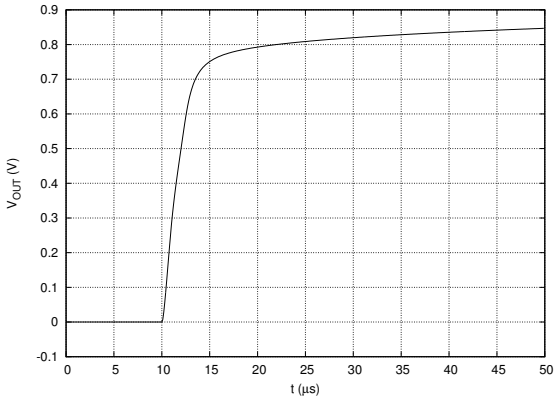


Figure 5.12: Step response of the op amp in Figure 4.1

One way to measure the slew rate of an op amp is to take its unity-gain step response and find where the greatest slope of the output voltage occurs. Figure 5.11 shows the simulation setup for finding the slew rate. Figure 5.12 shows the step response of the op amp in unity gain configuration when a 1 V square pulse is applied to its input. The slope is highest near the beginning of this step response, and was thus measured in the first 1 μs interval after the pulse was applied. The slew rate found in this interval is 278.5 kV/s.

5.8 Total Harmonic Distortion

The total harmonic distortion (THD) of a signal is defined as the ratio of the combined amplitudes of its harmonic frequencies over that of the fundamental frequency. The amplitudes of the harmonics are combined as root-mean-square (RMS) values. In other words, the THD of a signal is computed

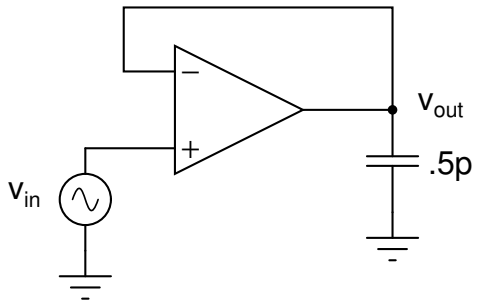


Figure 5.13: Simulation setup for measuring THD

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + \ldots + V_\infty^2}}{V_1} \tag{5.11}$$

where V_1 to V_∞ are amplitudes of the signal at the fundamental frequency and its harmonics.

Figure 5.13 shows the simulation setup for measuring the THD of an op amp. To measure the THD, a 0.5 V peak sinusoid input voltage operating at 4 kHz was applied to the input of a unity-gain configuration. The THD was found to be 0.111%. The simulation results are summarized in Table 5.1.

5.9 Comparison to Other Amps

The amplifier of Figure 4.1 is compared to other low power op amps in Table 5.2. This amplifier has the highest gain and lowest power dissipation of the amplifiers presented here. However, this amplifier requires more compensation capacitance than the other amplifiers and also uses a resistor. These components require the most chip area, making this amplifier costly in that category. This amplifier also has difficulty in driving loads with capacitance greater than 0.5 pF. This can be alleviated by adding a unity-gain buffer stage at the output (a CMOS source-follower stage will do).

This op amp performs better than the one proposed by Singh [5] in almost every category except phase margin, input-referred noise and required compensation capacitance and resistance. This demonstrates the benefit of having an extra degree of freedom in the conventional cascode configuration over the composite cascode. The phase margin is lower,

Table 5.1: Op amp simulation summary

Parameter	Performance
Voltage Supply (V)	±1.5
Power (μW)	4.347
Gain (dB)	137.7
Bandwidth (Hz)	0.118
GBW (MHz)	0.9
Phase Margin (degrees)	65
Output DC Offset (mV)	8.7
CMRR (dB)	134.3
PSRR (dB)	132.1
Input-referred Noise (nV/$\sqrt{\text{Hz}}$)	175.3
Slew Rate (V/μs)	0.279
THD (%)	0.111

Table 5.2: Op amp simulation comparison

Results Comparison	This work	[5]	[4]	[13]	[12]
Voltage Supply (V)	±1.5	±1.5	±1	-	1.8
Power (μW)	4.347	28.11	110	280	450
Gain (dB)	137.7	113.4	120	45	83.7
GBW (MHz)	0.9	0.31	1.42	1.1	69
Phase Margin (degrees)	65	75	43	-	87
CMRR (dB)	134.3	132	-	75	-
PSRR (dB)	132.1	131	-	-	-
Input-referred Noise (nV/$\sqrt{\text{Hz}}$)	175.3	134.5	49	22	-
Slew Rate (V/μs)	0.279	0.170	0.26	-	226
Comp. Capacitance (pF)	6.3	0	3.5	-	0

which means more compensation would be required to make these equal. This in turn would lead to reduced gain-bandwidth.

It is interesting to note that the op amp proposed by Sarbishaei [12] has a much better slew rate/power efficiency than the op amp proposed here. A class AB output stage could be used to improve the slew rate efficiency of the op amp of Figure 4.1.

Chapter 6

Conclusion and Future Work

This work demonstrates how circuit designers may increase gains and gain-bandwidth products for the CMOS cascode stage by using different inversion regions. For a chosen power level, the user may now find a near-optimal gain-bandwidth product for such a stage. Conversely, if a certain gain-bandwidth product is to be attained, the user can find the near-lowest power dissipation required. This allows for more efficient amplifiers to be designed.

This work also demonstrates how automation may be used to quickly explore circuit design space, especially in the case where changing parameters would require a new DC operating point to be found. A computer script was written to iterate over DC current, voltage bias difference, and the inversion coefficients for each transistor in the cascode configuration. The source code for this script is included, and may be extended by using threads that allow the simulation to time out if convergence doesn't occur.

The op amp of Figure 4.1 demonstrates that a conventional cascode stage has many benefits over a composite cascode stage such as higher gain, bandwidth, reduced power consumption and higher slew rates. Some drawbacks include increased compensation requirements (and thus more chip area) and increased input-referred noise. Though the op amp has been laid out, it was never fabricated. Thus a natural extension to this work is to fabricate this circuit (or perhaps an ultra low power amplifier tailored for gain-bandwidth product instead). Another possible extension to this work is to improve amplifier performance for chip area in addition to power.

Bibliography

[1] D. Foty and D. Foty, *MOSFET modeling with SPICE: principles and practice*, ser. Prentice Hall series in innovative technology. Prentice Hall PTR, 1997. [Online]. Available: http://books.google.com/books?id=tSVTAAAAMAAJ 1

[2] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical mos transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, July 1995. [Online]. Available: http://dx.doi.org/10.1007/BF01239381 1

[3] E. Vittoz and J. Fellrath, "Cmos analog integrated circuits based on weak inversion operations," *Solid-State Circuits, IEEE Journal of*, vol. 12, no. 3, pp. 224 – 231, jun 1977. 1

[4] D. T. Comer, D. J. Comer, and L. Li, "A high-gain complementary metal-oxide semiconductor op amp using composite cascode stages," *International Journal of Electronics*, vol. 97, no. 6, pp. 637–646, 2010. [Online]. Available: http://www.tandfonline.com/doi/abs/10.1080/00207211003646928 1, 6, 9, 10, 30

[5] R. P. Singh, D. J. Comer, T. Waddel, D. T. Comer, and K. Layton, "High-gain microwatt composite cascode op amps," *International Journal of Electronics*, vol. 99, no. 9, pp. 1179–1190, 2012. [Online]. Available: http://www.tandfonline.com/doi/abs/10.1080/00207217.2011.653952 1, 6, 9, 10, 29, 30

[6] D. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*. John Wiley & Sons, 2008. [Online]. Available: http://books.google.com/books?id=uGJIfTz-Z40C 3

[7] R. Sarpeshkar, *Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems*. 4

[8] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed. John Wiley & Sons, 2012. 4

[9] D. Comer and D. Comer, "Using the weak inversion region to optimize input stage design of cmos op amps," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 51, no. 1, pp. 8 – 14, jan 2004. 5

[10] D. J. Comer and D. T. Comer, *Fundamentals of Electronic Circuit Design*. John Wiley & Sons, 2003. [Online]. Available: http://books.google.com/books?id=A4UeAQAAIAAJ 5

[11] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, 2001. [Online]. Available: http://books.google.com/books?id=-VmVQgAACAAJ 5

[12] H. Sarbishaei, T. Kahookar Toosi, E. Zhian Tabasy, and R. Lotfi, "A high-gain high-speed low-power class ab operational amplifier," in *Circuits and Systems, 2005. 48th Midwest Symposium on*, aug. 2005, pp. 271 –274 Vol. 1. 30

[13] M. Goswami and S. Khanna, "Dc suppressed high gain active cmos instrumentation amplifier for biomedical application," in *Emerging Trends in Electrical and Computer Technology (ICETECT), 2011 International Conference on*, march 2011, pp. 747 –751. 30

Appendix A

Derivation of Cascode Gain Equations

A.1 Conventional Cascode

In order to derive the gain equation for a cascode stage with a resistive load, we must use a small-signal model. Figure A.1 shows such a model for a conventional cascode stage. Performing node-voltage analysis, we find that

$$g_{m1}v_{gs1} + g_{ds1}v_{s2} - g_{m2}v_{gs2} - g_{s2}v_{bs2} + g_{ds2}(v_{s2} - v_{out}) = 0 \tag{A.1}$$

and

$$g_{m2}v_{gs2} + g_{s2}v_{bs2} + g_{ds2}(v_{out} - v_{s2}) + G_L v_{out} = 0 \tag{A.2}$$

where $g_{ds} = 1/r_{ds}$ and $G_L = 1/R_L$. Now realizing that $v_{gs2} = v_{bs2} = -v_{s2}$ and $v_{gs1} = v_{in}$, we can simplify and rearrange (A.1) and (A.2) to obtain

$$g_{m1}v_{in} + (g_{ds1} + g_{m2} + g_{s2} + g_{ds2})v_{s2} - g_{ds2}v_{out} = 0 \tag{A.3}$$

and

$$-(g_{m2} + g_{s2} + g_{ds2})v_{s2} + (g_{ds2} + G_L)v_{out} = 0, \tag{A.4}$$

respectively. Further arrangement of (A.4) yields

$$v_{s2} = \frac{g_{ds2} + G_L}{g_{m2} + g_{s2} + g_{ds2}} v_{out}. \tag{A.5}$$

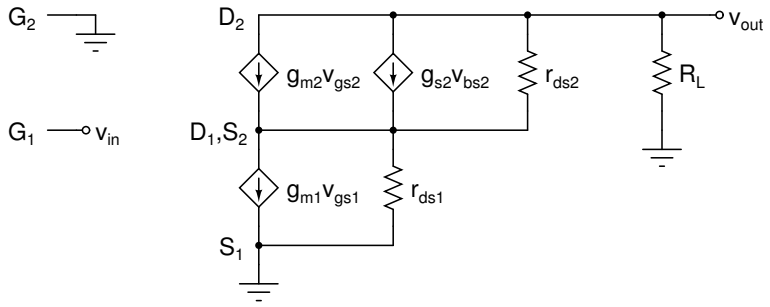


Figure A.1: Small-signal model for conventional cascode stage

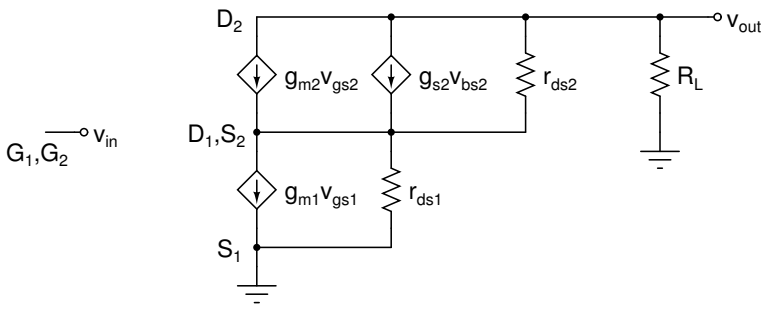


Figure A.2: Small-signal model for composite cascode stage

Substituting (A.5) into (A.3) yields

$$g_{m1}v_{in} + \frac{g_{ds1}g_{ds2} + G_L(g_{ds1} + g_{m2} + g_{s2} + g_{ds2})}{g_{m2} + g_{s2} + g_{ds2}}v_{out} = 0. \tag{A.6}$$

Rearranging (A.6) gives us the final result

$$A_{conv} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2})}{g_{ds1}g_{ds2} + G_L(g_{ds1} + g_{m2} + g_{s2} + g_{ds2})}. \tag{A.7}$$

A.2 Composite Cascode

Figure A.2 shows the small-signal model for the composite cascode stage. The only difference between this model and that for the conventional cascode stage is that both gates are tied to v_{in} rather than just that of M_1. Performing node-voltage analysis yields (A.1) and (A.2) as shown above. Once again, $v_{bs2} = -v_{s2}$ and $v_{gs1} = v_{in}$. However, $v_{gs2} = v_{in} - v_{s2}$, which will yield different equations

$$(g_{m1} - g_{m2})v_{in} + (g_{ds1} + g_{m2} + g_{s2} + g_{ds2})v_{s2} - g_{ds2}v_{out} = 0 \tag{A.8}$$

and

$$g_{m2}v_{in} - (g_{m2} + g_{s2} + g_{ds2})v_{s2} + (g_{ds2} + G_L)v_{out} = 0. \tag{A.9}$$

Rearranging (A.9) gives us

$$v_{s2} = \frac{g_{m2}}{g_{m2} + g_{s2} + g_{ds2}}v_{in} + \frac{g_{ds2} + G_L}{g_{m2} + g_{s2} + g_{ds2}}v_{out}. \tag{A.10}$$

Substituting (A.10) into (A.8) gives

$$\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2}) + g_{m2}g_{ds1}}{g_{m2} + g_{s2} + g_{ds2}}v_{in} + \frac{g_{ds1}g_{ds2} + G_L(g_{ds1} + g_{m2} + g_{s2} + g_{ds2})}{g_{m2} + g_{s2} + g_{ds2}}v_{out} = 0. \tag{A.11}$$

Rearranging (A.11) yields the final result

$$A_{comp} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}(g_{m2} + g_{s2} + g_{ds2}) + g_{m2}g_{ds1}}{g_{ds1}g_{ds2} + G_L(g_{ds1} + g_{m2} + g_{s2} + g_{ds2})}. \tag{A.12}$$

Appendix B

Source Code for Experiment

```
/* Include the headers necessary for the functions that we use. */
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <math.h>

/* These are transistor constants */
static double h = 1.5; /* The drain/source tap length (in micrometers) */
static double mu = 513.5602; /* cm^2 / Volt-sec */
static double eps0 = 8.884E-14; /* Permittivity of free space: F/cm */
static double epsr_sio2 = 3.9; /* Relative permittivity of SiO2: No units */
static double tox = 13.5E-7; /* oxide thickness: in cm */
static double cox; /* oxide capacitance: F/cm^2 */
static double Ut = 25.86E-3; /* In volts */
static double i0; /* Technology current in amps *without* substrate factor */

/* This function must be called before the simulations are performed to obtain
   correct results. */
static void initConstants() {
  cox = eps0*epsr_sio2/tox;
  i0 = 2.0*mu*cox*Ut*Ut; /* Substrate factor is not included here */
}

/* Inversion coefficients */
static double ics[] = {
  .003,
  .01,
  .03,
  .1,
  .3,
  1.,
  3.,
  10.,
  30.,
  100.,
  300.
};
static int icCount = sizeof(ics)/sizeof(double);

/* Drain currents in uA */
static double currents[] = {
  .1,
  .3,
  1.,
  3.,
  10.
};
static int currentCount = sizeof(currents)/sizeof(double);

/* Differences between bias voltages of M1 and M2 */
static double vbdiffs[] = {
  0.,
  .1,
```

```
  .2,
  .3,
  .4,
  .5,
  .6,
  .7,
  .8,
  .9,
  1.,
  1.1,
  1.2,
  1.3,
  1.4,
  1.5,
  1.6,
  1.7,
  1.8,
  1.9,
  2.,
  2.1,
  2.2,
  2.3,
  2.4,
  2.5,
  2.6,
  2.7,
  2.8,
  2.9,
  3.
};
static int vbdiffCount = sizeof(vbdiffs)/sizeof(double);

/* Used for file-reading operations */
static char buf[256];

/* This function calculates the width and length of a transistor based on the
   drain current and the inversion coefficient. */
static void calc_wl(double *w, double *l, double id, double ic) {
  double n,x,y;

  /* Calculate the substrate factor */
  if (ic < .1)
    n = 1.6;
  else if (ic < 10.)
    n = 1.45;
  else
    n = 1.3;

  /* Compute the dimensions. The minimum dimensions used are W=3u and L=.9u */
  x = .9;
  y = 1.0E-6*id*x/(n*i0*ic); /* Include substrate factor here */

  if (y < 3.) {
    x *= 3./y;
    y = 3.;
  }
  *w = y;
  *l = x;
}

/* This function prints the SPICE circuit file for DC simulation. */
static void print_dc(double vbdiff, double curr, double w1, double l1,
    double w2, double l2, double start, double stop, double inc) {
  FILE *file;

  file = fopen("test.cir","w");
  fprintf(file,
    "* C:\\ktech\\spice\\test.asc\n"
```

```
    "M1 N004 N005 0 0 nami l=%lfu w=%lfu pd=%lfu ps=%lfu ad=%lfp as=%lfp\n"
    "M2 N002 N003 N004 0 nami l=%lfu w=%lfu pd=%lfu ps=%lfu ad=%lfp as=%lfp\n"
    "V1 N005 N006 0 ac 1\n"
    "V2 N001 0 5\n"
    "V3 N006 0 1\n"
    "V4 N003 N006 %lf\n"
    "I1 N001 N002 %lfu\n"
    ".include mosmodels.txt\n"
    ".dc V3 %.9lf %.9lf %.9lf\n"
    ".print dc V(N002)\n"
    ".end",
    l1,w1,w1+2.*h,w1+2.*h,w1*h,w1*h,
    l2,w2,w2+2.*h,w2+2.*h,w2*h,w2*h,
    vbdiff,curr,start,stop,inc);
  fclose(file);
}

/* This function parses the simulation results from the last DC simulation. */
static int parse_dc(double *vinc, double *voutc, double start, double incr) {
  FILE *file;
  double point,vin,vout,trueVin;
  int parsedHead,parsedTail;

  /* Since the gains of some of these circuits are high, a small increment in
     bias voltage can cause the output voltage to skip. This allows us to find
     the closest voltage to 2.5V that we find. */
  *voutc = -100000.;
  *vinc = 0.;
  trueVin = start;

  file = fopen("test.raw","r");
  if (!file)
    return 0;
  parsedHead = 0;
  while (!parsedHead) {
    if (!fgets(buf,256,file))
      return 0;
    if (strstr(buf,"Values"))
      parsedHead = 1;
  }
  parsedTail = 0;
  while (fscanf(file, "%lf %lf %lf", &point, &vin, &vout) == 3) {
    if (fabs(2.5-vout) < fabs(2.5-*voutc)) {
      *voutc = vout;
      *vinc = trueVin;
      parsedTail = 1;
    }
    trueVin += incr;
  }
  fclose(file);
  return parsedTail;
}

/* This prints the circuit file for finding the transistor operating points. */
static void print_op(double vbdiff, double curr, double w1, double l1,
    double w2, double l2, double vbias) {
  FILE *file;

  file = fopen("test.cir","w");
  fprintf(file,
    "* C:\\ktech\\spice\\test.asc\n"
    "M1 N004 N005 0 0 nami l=%lfu w=%lfu pd=%lfu ps=%lfu ad=%lfp as=%lfp\n"
    "M2 N002 N003 N004 0 nami l=%lfu w=%lfu pd=%lfu ps=%lfu ad=%lfp as=%lfp\n"
    "V1 N005 N006 0 ac 1\n"
    "V2 N001 0 5\n"
    "V3 N006 0 %lf\n"
    "V4 N003 N006 %lf\n"
    "I1 N001 N002 %lfu\n"
```

```
    ".include mosmodels.txt\n"
    ".op\n"
    ".print op V(N004)\n"
    ".end",
    l1,w1,w1+2.*h,w1+2.*h,w1*h,w1*h,
    l2,w2,w2+2.*h,w2+2.*h,w2*h,w2*h,
    vbias,vbdiff,curr);
  fclose(file);
}

/* This structure is used for parsing the operating points of each
   transistor. */
typedef struct MosOp MosOp;
struct MosOp {
  double id,vgs,vds,vbs,vth,vdsat,gm,gds,gmb,cbd,cbs,cgsov,cgdov,cgbov;
};

/* This function parses the operating points of each transistor. */
static int parse_op(MosOp *m1, MosOp *m2) {
  FILE *file;
  int parsedHead,i;

  /* The operating point is stored in a separate log file. This file is not to
     be confused with test_log.txt, which is used to store the success/failure
     of each overall result. */
  file = fopen("test.log","r");
  if (!file)
    return 0;
  parsedHead = 0;
  while (!parsedHead) {
    if (!fgets(buf,256,file))
      return 0;
    if (strstr(buf,"BSIM3 MOSFETS"))
      parsedHead = 1;
  }
  for (i = 0; i < 3; ++i) {
    if (!fgets(buf,256,file))
      return 0;
  }
  if (sscanf(buf+8, " %lf %lf", &m2->id, &m1->id) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->vgs, &m1->vgs) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->vds, &m1->vds) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->vbs, &m1->vbs) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->vth, &m1->vth) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->vdsat, &m1->vdsat) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->gm, &m1->gm) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->gds, &m1->gds) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->gmb, &m1->gmb) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->cbd, &m1->cbd) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->cbs, &m1->cbs) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->cgsov, &m1->cgsov) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->cgdov, &m1->cgdov) != 2) return 0;
  if (!fgets(buf,256,file)) return 0;
  if (sscanf(buf+8, " %lf %lf", &m2->cgbov, &m1->cgbov) != 2) return 0;
  fclose(file);
  return 1;
```

```
}

/* This function prints the AC simulation circuit file. */
static void print_ac(double vbdiff, double curr, double w1, double l1,
    double w2, double l2, double vbias) {
  FILE *file;

  file = fopen("test.cir","w");
  fprintf(file,
    "* C:\\ktech\\spice\\test.asc\n"
    "M1 N004 N005 0 0 nami l=%lfu w=%lfu pd=%lfu ps=%lfu ad=%lfp as=%lfp\n"
    "M2 N002 N003 N004 0 nami l=%lfu w=%lfu pd=%lfu ps=%lfu ad=%lfp as=%lfp\n"
    "V1 N005 N006 0 ac 1\n"
    "V2 N001 0 5\n"
    "V3 N006 0 %lf\n"
    "V4 N003 N006 %lf\n"
    "I1 N001 N002 %lfu\n"
    ".include mosmodels.txt\n"
    ".ac dec 51 1m 100G\n"
    ".print ac V(N002)\n"
    ".end",
    l1,w1,w1+2.*h,w1+2.*h,w1*h,w1*h,
    l2,w2,w2+2.*h,w2+2.*h,w2*h,w2*h,
    vbias,vbdiff,curr);
  fclose(file);
}

/* This structure represents a 2D vector, and is used when parsing AC simulation
   results. */
typedef struct Vect2d Vect2d;
struct Vect2d {
  double x,y;
};

/* This is the only vector function used, so it is included here for brevity. */
double vect2d_len(Vect2d *vect) {
  return sqrt(vect->x*vect->x+vect->y*vect->y);
}

/* This function parses the AC simulation to find gain and bandwidth. */
static int parse_ac(double *gain, double *bw) {
  Vect2d v;
  FILE *file;
  double point,freq,dummy;
  int parsedHead,parsedGain,parsedBw;

  parsedGain = 0;
  parsedBw = 0;
  *gain = 0.;
  *bw = 0.;

  file = fopen("test.raw","r");
  if (!file)
    return 0;
  parsedHead = 0;
  while (!parsedHead) {
    if (!fgets(buf,256,file))
      return 0;
    if (strstr(buf,"Values"))
      parsedHead = 1;
  }
  while (fscanf(file, "%lf %lf,%lf %lf,%lf", &point, &freq, &dummy, &v.x, &v.y) == 5) {
    if (parsedGain == 0) {
      *gain = vect2d_len(&v);
      parsedGain = 1;
    }
    if (parsedBw == 0) {
      if (vect2d_len(&v) <= 0.70710678118*(*gain)) {
```

```
        *bw = freq;
         parsedBw = 1;
      }
    }
  }
  fclose(file);
  return (parsedGain && parsedBw);
}

int main() {
  MosOp m1,m2;
  FILE *file,*logfile;
  double vout,vin,gain,bw,start,stop,incr,w1,l1,w2,l2;
  int i,j,k,l,is,js,ks,ls;

  /* Must be called before the simulations to ensure that NMOS parameters have
     their proper values */
  initConstants();

  /* This file is used for storing the results in the simulation. This file can
     be imported into any spreadsheet program since it is stored in text
     format. */
  file = fopen("test_results.txt","w");
  fprintf(file, "#Vbdiff    Id          IC1         IC2         Vin                 "
    "Vout                Gain          BW          Vgs1          Vds1          Vbs1"
    "          Vth1          Vdsat1        Gm1           Gds1          Gmb1          Cbd1"
    "          Cbs1          Cgsov1        Cgdov1        Cgbov1        W1            L1"
    "            Vgs2          Vds2"
    "          Vbs2          Vth2          Vdsat2        Gm2           Gds2          Gmb2"
    "          Cbd2          Cbs2          Cgsov2        Cgdov2        Cgbov2"
    "       W2            L2\n");

  /* The log file keeps track of which simulations went well and which ones had
     problems (and if possible, where the problems occurred). */
  logfile = fopen("test_log.txt","w");

  /* These allow us to select where in the simulation to resume if something
     (such as SPICE not converging) goes wrong. */
  is = 0;
  js = 0;
  ks = 0;
  ls = 0;

  /* Iterate over the voltage bias difference, drain current and the inversion
     coefficients of the cascoded transistors. */
  for (i = is; i < vbdiffCount; ++i) { /* vbdiff */
    for (j = js; j < currentCount; ++j) { /* curr */
      for (k = ks; k < icCount; ++k) { /* ic1 */
        /* Obtain M1 dimensions */
        calc_wl(&w1, &l1, currents[j], ics[k]);

        for (l = ls; l < icCount; ++l) { /* ic2 */
          /* Obtain M2 dimensions */
          calc_wl(&w2, &l2, currents[j], ics[l]);

          /* Print out which iteration we're in just in case we need to stop
             program */
          fprintf(stderr, "Process %d %d %d %d: ", i, j, k, l);
          fprintf(logfile, "Process %d %d %d %d: ", i, j, k, l);

          /* Perform 3 DC simulations in order to find the bias voltage (to the
             nearest nV) that gets the output voltage closest to 2.5V. */
          print_dc(vbdiffs[i],currents[j],w1,l1,w2,l2,0.,5.,.001);

          /* Each system command runs LTspice in batch mode and prints out the
             results in text form that can be parsed. */
          system("scad3.exe -b -ascii test.cir");
          if (!parse_dc(&vin,&vout,0.,.001)) {
```

```
  fprintf(stderr, "failed DC1\n");
  fprintf(logfile, "failed DC1\n");
  continue;
}

/* Run 2nd DC simulation, stepping bias voltage by 1uV */
if (vout < 2.5)
  start=vin-.001;
else
  start=vin;
stop=start+.001;
incr=.000001;
print_dc(vbdiffs[i],currents[j],w1,l1,w2,l2,start,stop,incr);
system("scad3.exe -b -ascii test.cir");
if (!parse_dc(&vin,&vout,start,incr)) {
  fprintf(stderr, "failed DC2\n");
  fprintf(logfile, "failed DC2\n");
  continue;
}

/* Run 3rd DC simulation, stepping bias voltage by 1nV */
if (vout < 2.5)
  start=vin-.000001;
else
  start=vin;
stop=start+.000001;
incr=.000000001;
print_dc(vbdiffs[i],currents[j],w1,l1,w2,l2,start,stop,incr);
system("scad3.exe -b -ascii test.cir");
if (!parse_dc(&vin,&vout,start,incr)) {
  fprintf(stderr, "failed DC3\n");
  fprintf(logfile, "failed DC3\n");
  continue;
}

/* If we are more than .1V away from 2.5V at the output, then we
   reject this result and move on. */
if (fabs(2.5-vout) > .1) {
  fprintf(stderr, "failed vout\n");
  fprintf(logfile, "failed vout\n");
  continue;
}

/* This parses the operating point of the transistors so that we can
   print various transistor parameters. */
print_op(vbdiffs[i],currents[j],w1,l1,w2,l2,vin);
system("scad3.exe -b -ascii test.cir");
if (!parse_op(&m1,&m2)) {
  fprintf(stderr, "failed OP\n");
  fprintf(logfile, "failed OP\n");
  continue;
}

/* Here we parse the AC simulation result. */
print_ac(vbdiffs[i],currents[j],w1,l1,w2,l2,vin);
system("scad3.exe -b -ascii test.cir");
if (!parse_ac(&gain,&bw)) {
  fprintf(stderr, "failed AC\n");
  fprintf(logfile, "failed AC\n");
  continue;
}

/* We were successful in parsing all the intermediate results, so
   print out what we have found. */
fprintf(file, "%.11E  %.11E  %.11E  %.11E  %.91E  %.91E  %.31E  %.31E"
  "  %.31E  %.31E  %+.31E  %.31E  %.31E  %.31E  %.31E  %.31E  %.31E"
  "  %.31E  %.31E  %.31E  %.31E  %.31E  %.31E"
  "  %.31E  %.31E  %+.31E  %.31E  %.31E  %.31E  %.31E  %.31E  %.31E"
```

```
            "  %.3lE  %.3lE  %.3lE  %.3lE  %.3lE  %.3lE\n",
             vbdiffs[i], currents[j], ics[k], ics[l], vin, vout, gain, bw,
             m1.vgs, m1.vds, m1.vbs, m1.vth, m1.vdsat, m1.gm, m1.gds, m1.gmb, m1.cbd,
             m1.cbs, m1.cgsov, m1.cgdov, m1.cgbov, w1, l1,
             m2.vgs, m2.vds, m2.vbs, m2.vth, m2.vdsat, m2.gm, m2.gds, m2.gmb, m2.cbd,
             m2.cbs, m2.cgsov, m2.cgdov, m2.cgbov, w2, l2);
           fflush(file);

           /* Update the log file and echo the result in the command line. */
           fprintf(stderr, "OK\n");
           fprintf(logfile, "OK\n");
         }
         ls = 0;
       }
       ks = 0;
     }
     js = 0;
   }

   fclose(file);
   fprintf(stderr, "Done.\n");
   return 0;
}
```

Listing B.1: Source Code for Cascode Experiment