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A High-Gain, Low-Power CMOS Operational Amplifier Using Composite Cascode Stage in the Subthreshold Region

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A HIGH GAIN, LOW POWER CMOS OPERATIONAL AMPLIFIER 
USING COMPOSITE CASCODE STAGE IN 
THE SUBTHRESHOLD REGION 

Rishi Pratap Singh 

A thesis submitted to the faculty of 
Brigham Young University 
in partial fulfillment of the requirements for the degree of 

Master of Science 

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ABSTRACT

A HIGH GAIN, LOW POWER CMOS OPERATIONAL AMPLIFIER
USING COMPOSITE CASCODE STAGE IN
THE SUBTHRESHOLD REGION

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Master of Science

This thesis demonstrates that the composite cascode differential stage, operating in the subthreshold region, can form the basis of a high gain (113 dB) and low-power op amp (28.1 $\mu$W). The circuit can be fabricated without adding a compensation capacitance. The advantages of this architecture include high voltage gain, low bandwidth, low harmonic distortion, low quiescent current and power, and small chip area. These advantages suggest that this design might be well-suited for biomedical applications where low power, low noise bio-signal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range is required.

Keywords: high gain, low power, low noise, low distortion, composite cascode stage, subthreshold operation, strong inversion, moderate inversion, weak inversion operation, amplifier
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Chapter 1

Introduction

The operational amplifier or op amp is the most popular integrated circuit chip in the electronics world and plays an important role in integrated circuit simulations, control systems and low-to-moderate frequency amplifier applications. Since new technology demands efficient circuits with high accuracy and low power consumption, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) offers flexibility to both analog and digital designers for the design of such circuits. One of these circuits is discussed in this thesis - a high-gain, low-power Complementary Metal Oxide Semiconductor (CMOS) op amp using a composite cascode stage in the subthreshold region. This work also considers existing compensation methods of op amps relative to chip area and compares the chip area to that of a previously published composite cascode op amp [1].

In the classical operational amplifier (discussed in chapter 2), a large compensation capacitor is used to stabilize the amplifier requiring a large amount of area on the integrated circuit chip. Additionally, this capacitor limits the bandwidth of the op amp and also affects the slew rate. Slew rate is the maximum rate at which the output voltage of an op amp can change and in general, designers always look for a higher slew rate. Moreover the supply voltage used for the classical designs is quite high (> 5V) and that limits its application in low power circuits.

The proposed design (discussed in detail in later chapters) offers an op amp with high gain, low power operation without using a compensation capacitor. For low power operation, MOSFETs are used as a building block for the op amp to improve its efficiency. The characteristics of these op amps will be appreciated in any chip designs where minimizing the chip area and power is essential. This type of design can be used in applications such as in the biomedical field where the need to miniaturize battery operated devices is in high
demand [2]. There is a need among medical scientists and clinicians for low-noise, low-
power, bio-signal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range
while rejecting large DC offsets generated at the electrode/tissue interface. The advent of
fully implantable multi-electrode arrays has created a need for fully integrated micro power
amplifiers [3]. Low current amplifiers are the basic building blocks of the pulse oximeter
($SpO_2$), a wireless sensor network system that has the capability to monitor physiological
signs and heart beat rate in real-time from the human body [4] [5].

1.1 Theme of the thesis

This thesis discusses the design of a high-gain, low power, low harmonic distortion
op amp. The basis of the work is a differential composite cascode stage operating in the
subthreshold region as an input stage followed by a class AB output stage. This design
allows the elimination of the bridging capacitor between the input and output of the second
stage for compensation while reducing the chip area required by the amplifier. Operation in
the subthreshold operation leads to a low bias current, resulting in low power consumption,
and low harmonic distortion [6], [7].

1.2 Outline of the thesis

This thesis is divided into eight chapters including the introduction. It starts with a
brief introduction of the op amp transitioning into an explanation of the classical amplifier
and its merits and disadvantages. Chapter 3 proposes a new design of the op amp followed
by a detailed explanation of the circuit design and the layout of the corresponding amplifier.
The section on circuit design and the layout covers a wide range of theoretical as well as
practical approaches in determining the efficiency of the integrated circuit. Later chapters
emphasize optimization of the load seen by the circuit for testing purposes, other simulation
methods, test results and related topics of interest for future research.

1.3 Contributions

The contributions of this thesis include:
• the design of a two stage op amp with high gain (113 dB), low power (21.3 µW), and low distortion (0.22% THD);

• the layout and fabrication of the op amp with performance that agrees closely with the simulation.
Chapter 2

Classical operational amplifier

The term classical op amp refers to the op amp designed in the early phase of integrated circuits. Since then the op amp has evolved in terms of speed, design complexity, linearity, lower power consumption and accuracy.

The first generation, bipolar junction transistor (BJT), integrated circuit op amp of 1964 was designed to have a high voltage gain differential input stage, a moderately high voltage gain second stage, and a low voltage gain/high current gain third stage that acts as a buffer [8]. The second stage has a modest voltage gain compared to the first stage and is often used to compensate the op amp. The usual practice is to place the compensating capacitor between the input and output of the second stage utilizing the Miller effect to multiply the capacitor value. Bridging the input and output nodes of the second stage results in a phenomenon known as pole splitting. This phenomenon lowers the pole or 3-dB frequency of the first stage and moves the pole of the second stage to a higher frequency which helps the op amp to achieve required stability in the presence of feedback. Pole splitting is advantageous in achieving a higher frequency design, but requires a capacitance and a resistance for proper compensation of MOSFET op amps and, thus, adds complexity to the design [9].

The size of the compensating capacitor as well as the resistance needed for stability can also require a large chip area. The first method of compensation included use of an external off-chip capacitor but limited the bandwidth of the amplifier. The National LM101 (designed by Widlar) and the Fairchild Semiconductor Corporation 741 were introduced in 1967 and used similar circuit architecture [10]. Both of these amplifiers used BJTs and eliminated the use of external capacitors for the compensation.
BJTs burn more power than MOSFETs, raising red flags for its implementation in low power design. The data-sheet of the LM741 [11] showed the voltage noise and the supply current to be 30 nV/(square root Hz) and 1.7 mA respectively during normal operation which is considered high for many modern application specific integrated circuits (ASIC) such as low-power instrumentation applications in biomedical fields. Classical op amp designs with a compensation capacitor also impact the speed of the operational amplifier and other applications where the rise times of digital signals are quite small. At times, when the rise time of the digital signal is small, feed-through takes place in the second stage due to the bridging capacitor. The signal at the input of this stage now has two paths, one through the amplifier and another through the compensation capacitor. This signal that feeds through the compensation capacitor introduces a right hand plane zero that can affect the stability of the op amp as it boosts the magnitude response and lags the phase response of the op amp. As a usual practice, a nulling resistance is added in series with the compensation capacitor to gain control over this right hand plane zero introduced by the bridging capacitor.

Today, the MOSFET is gaining popularity in op amp design because of its potential low power operation, but it has been difficult to design a MOSFET op amp that follows a Widlar architecture and achieves a high voltage gain. A new design [1], offers a high gain CMOS op amp that uses a Widlar architecture. The measured gain of 117 dB is comparable to that achieved in bipolar designs in this architecture. Another new design [7] proposed in this thesis does not follow the Widlar architecture, but offers a low power CMOS op amp with a high voltage gain (113 dB) and eliminates the use of a bridging (Miller) capacitor for compensation and is discussed in detail in later chapters.
Chapter 3

Proposed design of operational amplifier

In recent years, an area of increasing interest is that of biomedical instrumentation amplifiers [2], [12]. These applications typically require high gain, low power, and low frequency amplifiers that occupy minimal chip real estate. The proposed design discusses the subthreshold operation of composite cascode stages to achieve advantages such as high voltage gain [1], low distortion [2], [6], low noise [2], low power, low chip area, and low bandwidth. Although low bandwidth is often considered a shortcoming, in this case, it is used to eliminate the need for a compensation capacitor to achieve stable operation in the presence of feedback.

An earlier work [6] demonstrated that high voltage gain could be obtained by operation of MOS (Metal Oxide Semiconductor) devices in the weak or moderate inversion regions and mentions the advantages of designing the input differential stage of CMOS op amps to operate in the moderate and weak inversion regions. Furthermore, it also offers guidelines to optimize an op amp performance by obtaining higher gain, less power dissipation, less distortion, and a smaller value of compensation capacitor. In another work [13], it was suggested that a voltage gain exceeding 60 dB per stage could be achieved by combining operation in the weak or moderate inversion region with the composite cascode configuration of Fig. 3.1. A circuit configuration similar to this configuration but with the p-MOS composite cascode as a driver and the n-MOS composite cascode as a load is covered in detail in Chapter 4. Chapter 4 also mentions the conditions required to attain the subthreshold or weak or strong inversion MOS operations exploited in these circuit configurations for higher voltage gain. The point to be noted in Fig. 3.1 is that the device M2 operates in the subthreshold region while M1 operates in the weak, moderate, or strong inversion region for higher voltage gain. The subthreshold drain current of device M2 leads to a large output resistance looking into
the drain of device M2 (explained in Chapter 4). These devices combine with the composite cascode load (devices M3 and M4) which provide a large output resistance and results in a very high voltage gain. This concept was implemented for the first time [1] in a high gain (\( \sim 120 \) dB) CMOS op amp that used the Widlar architecture. In that work, both the first and second stages have high gain (\( \sim 60 \) dB) and moderate bandwidth. The circuit for this op amp is shown in Fig. 3.2. It also demonstrated that the compensation capacitor can be minimized with this approach, requiring a 3.5 pF value for the op amp which is quite low compared to the classical op amp compensation capacitor.

The proposed design in this thesis takes the earlier mentioned work in [1] to the next level by emphasizing the use of the composite cascode differential stage, operating in

Figure 3.1: Single ended composite cascode gain stage
subthreshold region that can form the basis of a high gain ($\sim 113$ dB), and low-power op amp ($\sim 28.11 \mu$W) without adding an intentional compensation capacitor. The proposed design can drive a capacitive load of 0.5 pF and resistor of 100 k$\Omega$. The immediate advantage of this design over the earlier work [1], classical amplifiers, and other op amp designs requiring compensation capacitors can be realized not only in the reduction of the effects of feed through but also the chip area. The parasitic capacitance at the output of the first stage is used to compensate the op amp. Because of the low DC current required by the differential input stage, DC power consumption is also minimized. In addition, operation in the weak
inversion region can also lead to lower harmonic distortion than normally achieved in strong inversion operation [6] of devices. Such performance by the proposed op amp is well-suited for low-power instrumentation applications requiring multiple amplifiers as often found in biomedical applications [2], [12].

The circuit for the proposed design is shown in Fig. 5.2. The next chapter covers the details behind the circuit design of the proposed operational amplifier.
Figure 3.3: Proposed design of amplifier
Chapter 4

Circuit design of proposed operational amplifier

The circuit for the proposed design of an op amp can be divided into four parts: a Constant-$g_m$ biasing circuit, an input differential stage, a class AB output stage, and a control circuit. The Constant-$g_m$ biasing circuit and the control circuit assure stability and low power operation of the op amp whereas the class AB output stage allows a smaller quiescent bias current, saving power while still being able to source large currents for dynamic transitions. The first section below explains in detail the theory behind the operation of the MOS devices in a state that is exploited in the input differential stage for higher voltage gain. The other sections not only explain the circuit in detail but also mention the specific applications of the involved circuitry in the proposed op amp design. Simulation results related to proposed design are discussed in following chapter.

4.1 Subthreshold/weak inversion region

MOS devices in amplifiers are generally biased to operate in the strong inversion region where the variation in $I_D$ with gate-to-source ($V_{GS}$) voltage almost follows the square-law variation as given by [14]

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda (V_{DS} - V_{DSP})),$$

$$= \frac{2\eta\mu C_{ox} W V_T^2}{L} \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) [15]. \quad (4.1)$$
The transconductance \( (g_m) \) of a device in strong inversion region is proportional to the square root of the drain current \( (I_D) \) and is given by [14]

\[
g_m = \sqrt{2\mu_n C_{ox} \left( \frac{W}{L} \right) I_D} \tag{4.2}
\]

where the value of \( \eta \), a nonideality factor, ranges from 1.6 in weak inversion region to 1.3 in the strong inversion region [16], [17]. The parameters \( g_m \) and the incremental resistance \( (r_{ds}) \) from the drain to source of a MOS device are responsible for the voltage gain from the gate to drain of a device. The expression for the \( r_{ds} \) is given by

\[
r_{ds} = \frac{1}{\lambda I_D}. \tag{4.3}
\]

For devices biased to operate in the weak or subthreshold region, the expression for the \( r_{ds} \) and the relationship between current \( I_D \) and voltage \( V_{GS} \) is given by [18]

\[
r_{ds} = \frac{V_A}{I_D}, \tag{4.4}
\]

\[
I_D = I_{D0} \exp \left( \frac{V_{GS}}{\eta V_T} \right) \tag{4.5}
\]

where the specific current \( (I_{D0}) \) [16] and the thermal voltage \( (V_T) \) is given by

\[
I_{D0} = 2\eta \mu C_{ox} V_T^2 \frac{W}{L}, \tag{4.6}
\]

\[
V_T = \frac{KT}{q}. \tag{4.7}
\]
where $V_A$ is an Early voltage which is approximately constant for a given channel length. Also from the definition of $g_m$ keeping $V_{DS}$ constant, we have

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{\eta V_T}. \quad (4.8)$$

From Fig. 4.1, it can be seen that devices operating in subthreshold region have lower $V_{GS}$ than the one operating in the strong inversion region. The V-I curve in the Fig. 4.1 also shows that $r_{ds}$ is larger for the device biased in the subthreshold region than the one biased in the strong inversion region.

An earlier work [6] mentions the conditions for the operation of a MOS device in strong, weak or moderate inversion regions. Fig. 4.1 shows that the control of the voltage $V_{GS}$ over the threshold voltage ($V_{TH}$) affects the operation of the n-MOS device. Generally circuits are designed keeping bias currents in mind. As a guideline [15], the operating regions can also be estimated in terms of the inversion coefficient (IC), $IC = I_D/I_{D0}$. Weak inversion corresponds to $IC < 0.1$, moderate inversion corresponds to $0.1 < IC < 10$ and strong inversion corresponds to $IC > 10$. Since $I_{D0}$ is proportional to the width of the device, a larger width decreases IC enabling the weak or moderate inversion operation of the device. Larger devices exhibit larger parasitic capacitances resulting in lower bandwidth of the stage. This can be advantageous if used in the input differential stage of the op amp that requires a small compensating capacitor to stabilize the op amp.

This work [6] also suggests that MOS devices operating in subthreshold region when used in amplifier stages lead to various advantages such as higher voltage gain, lower power dissipation due to decreased $I_D$, and reduced total harmonic distortion. Higher voltage gain is related to the transconductance efficiency ($g_m/I_D$) of the devices operating in weak or moderate inversion. In these inversion regions, $g_m/I_D$ approaches a constant and reaches maximum values in the weak/subthreshold region and decreases as the inverse square-root of $IC$ in the strong inversion region [6],[15]. The expression for $g_m/I_D$ is given by $g_m/I_D = 1/(\eta V_T)$ and $g_m/I_D = 1/(\eta V_T \sqrt{IC})$ for the device biased in the weak or subthreshold region and the strong inversion region respectively. Subthreshold or weak inversion operation of MOS devices results in higher voltage gain at the cost of lower bandwidth. Since subthreshold
inversion requires larger devices for lower IC, the intrinsic gate capacitance and the gate-to-
bulk capacitance increase lowering the intrinsic bandwidth. But lower IC also decreases the
thermal-noise voltage density as $g_m/I_D$ and $g_m$ increases. The flicker noise voltage density
also increases with IC, because the gate area decreases with IC in the transition from weak
to strong inversion region and vice versa [15]. Lower noise is an important aspect of any low
power circuit design.

4.2 Composite cascode stage

An earlier work [13] demonstrated several advantages of the composite cascode stage
over the conventional cascode stage. The architecture requires one less bias voltage reference
to bias the composite cascode stage. Other advantages of the composite cascode stage
pertinent to the proposed design include the realization of the input differential stage with
higher voltage gain, low drain current, and low bandwidth. The low bandwidth is better
as it helps in dominant pole compensation of the op amp. Fig. 4.2 shows the composite
cascode stage with an ideal current source as a load. It can be shown (see appendix) that
the voltage gain of the stage is given by

$$A_{MB} = \frac{V_{OUT}}{V_{IN}} = \frac{-g_m r_{ds1} (g_{m2} + g_{mb2}) r_{ds2} + g_m r_{ds1} + g_m r_{ds2}}{1 + \frac{1}{R} [(g_{m2} + g_{mb2}) r_{ds1} r_{ds2} + r_{ds1} + r_{ds2}]^2}$$

(4.9)
where $r_{ds1}$ and $r_{ds2}$ are the incremental resistances between drain and source of device M1 and M2 respectively and $g_{mb2}$ represents the body effect of device M2. Both devices M1 and M2 are biased to operate in the active region with M2 biased to operate in the subthreshold region and M1 in the weak, moderate, or strong inversion region.

The more practical composite cascode stage with a composite cascode current mirror as a load is shown in Fig. 4.3. The voltage gain of such a stage can be approximated by

$$A_{MB} = \frac{-[g_m r_{ds1}(g_m + g_{mb2})r_{ds2} + g_m r_{ds1}^2 + g_{mb2} r_{ds2}^2]}{1 + \frac{(g_m + g_{mb2})r_{ds1}r_{ds2} + r_{ds1} + r_{ds2}}{(g_m + g_{mb4})r_{ds1}r_{ds2} + r_{ds1} + r_{ds2}}}.$$  \hspace{1cm} (4.10)

In Fig. 4.3, all the devices are biased to operate in the active region with M2 and M4 biased to operate in the subthreshold region and M1 and M3 in either the subthreshold or moderate or strongly inverted region. M3 and M4 form a composite cascode current mirror load for the stage. The aspect ratio (W/L) of devices M1(M3) is chosen much smaller
than that of M2(M4) such that the IC of device M1(M3) is about 100 times larger than the IC of device M2(M4) for a selected bias current. As discussed in an earlier section, $g_m/I_D$ remains constant in the weak or subthreshold region [15], resulting in the overall product of $(g_{m2} + g_{mb2})$ and $r_{ds2}$ being approximately constant with $I_D$. This work [15] also demonstrates that Early voltage ($V_A$) increases rapidly as channel length increases from the process minimum. Using this technique $r_{ds1}$ can also be maximized, since $r_{ds} = V_A/I_D$ and higher $V_A$ results in larger $r_{ds}$ for a selected $I_D$. Lower bias current for the stage will also insure the maximization of the product of $g_{m1}$ and $r_{ds1}$ as the falloff of $g_{m1}$ is less significant than the increase in $r_{ds1}$ resulting in higher overall voltage gain approximated by Eq. 4.10.
Also, the effective resistance, \( R_{\text{effective1}} \), looking into the drain of M2 can be approximated by

\[
R_{\text{effective1}} = (g_{m2} + g_{mb2})r_{ds2}r_{ds1} + r_{ds2} + r_{ds1}. \tag{4.11}
\]

It can be seen from Eq. 4.11 that the \( R_{\text{effective1}} \) increases with \( r_{ds1} \) which can be maximized by selecting a certain aspect ratio of the device M1. Similarly, \( R_{\text{effective2}} \) looking into the drain of device M4, \( R_{\text{effective2}} = (g_{m4} + g_{mb4})r_{ds4}r_{ds3} + r_{ds4} + r_{ds3} \), can be maximized following the same approach. Comparing Fig. 4.3 with the common source gain stage, the mid-band voltage gain can be approximated by the product \( g_m R_{OUT} \) of the stage. Since the \( R_{OUT} \) looking from \( V_{OUT} \) into the drain of M2 and M4 is given by parallel combination of \( R_{\text{effective1}} \) and \( R_s \), increasing \( r_{ds3} \) increases the \( R_{\text{effective1}} \) which increases the \( R_{OUT} \) and the voltage gain. \( r_{ds3} \) can be increased by choosing the longer channel length of the device.

The derivation of the small signal voltage gain of Fig. 4.3 is provided in the appendix.

### 4.3 Input differential stage

The input differential stage shown in Fig. 4.4, forms the first stage of the proposed design. The approach covered in an earlier section of this chapter is utilized to design this stage. A Constant-\( g_m \) biasing circuit, explained in the next section, biases this stage and provides a constant \( g_m \) for the devices M9 - M12 over change in any process and temperature. Devices M11 - M14 are biased to operate in the subthreshold region whereas M9, M10, M15 and M16 are biased to operate in the weak or moderate inversion region. This setup along with low bias current (\(< 200 \) nA) for the stage insures higher voltage gain (\( \sim 98 \) dB) and low bandwidth. Since the bandwidth and the gain are related (the higher the gain the lower is the bandwidth), a change in \( V_{bias} \) affects the total bias current in the stage which in turn affects the gain and bandwidth. The higher total bias current decreases the gain and vice versa. The gain of this stage is approximated by

\[
A_{MB} = \frac{-[g_{m10}r_{ds10}(g_{m12} + g_{mb12})r_{ds12} + g_{m10}r_{ds10} + g_{m12}r_{ds12}]}{1 + \frac{(g_{m12} + g_{mb12})r_{ds12} + g_{m10}r_{ds10} + r_{ds12}}{(g_{m14} + g_{mb14})r_{ds14} + r_{ds14} + r_{ds12}}}. \tag{4.12}
\]
Figure 4.4: Input differential stage

Again the effective resistance, $R_s$, looking into the drain of M14 is approximately given by

$$R_s = (g_{m14} + g_{mb14})r_{ds16} + r_{ds16} + r_{ds14}.$$  \hspace{1cm} (4.13)

The bandwidth of the stage depends upon the effective resistance and capacitance looking from the node $V_{OUT}$ as

$$\omega_{3dB} \approx \frac{1}{R_{effective}C_{effective}}.$$  \hspace{1cm} (4.14)
The effective resistance and capacitance can be approximated by

\[ R_{\text{effective}} = R_s||R_D, \]  

(4.15)

\[ C_{\text{effective}} = C_{gd14} + C_{db14} + C_{gd12} + C_{db12} + C_2 \]  

(4.16)

where \( R_D \) and \( R_s \) are the effective resistance looking into the drain of M12 and drain of M14 respectively and can be approximated using the Eq. 4.9. \( C_2 \) is the effective capacitance looking into the input of the next stage (Fig. 4.6) which can be approximated for the proposed design by

\[ C_2 = C_{gs20} + C_{gd20}(1 + A_{20}) + C_{gd22}(1 + A_{22}) + C_{gs22} \]  

(4.17)

where \( A_{20} \) and \( A_{22} \) are the gain from gate to source of device M20 and gate to drain of device M22 respectively.

The composite cascode current mirror load in Fig. 4.4 produces a mirror pole which can affect the stability of the op amp. Careful analysis is required to compensate this pole for better phase margin, explained in detail in a later section. The effective resistance and capacitance looking into the junction of the drain of device M11 and drain and gate of M13 affects the placement of the mirror pole in the frequency domain. Looking into the drain of the diode connected device M13, the reciprocal of transconductance \( g_{m13} \) dominates the effective resistance (\( R_M \)) whereas the effective capacitance can be approximated by

\[ C_m = C_{db11} + C_{gs13} + C_{db13} + C_{gs15} + C_{gd15}(1 + A_{15}) + C_{gs14} + C_{gd14}(1 + A_{14}) + C_{gs16} + C_{gd16}(1 + A_{16}) \]  

(4.18)

where \( A_{ij} \) is the gain from gate to drain of the respective devices.

The other consideration taken for minimizing flicker noise (\( \frac{1}{f} \) noise) and maximizing the slew rate and unity-gain frequency of the op amp, p-channel input devices are used in this stage. The flicker noise is lower in p-channel devices than the n-channel devices since
their majority carriers (holes) have less potential to be trapped in surface states [9]. The slew rate of the two stage op amp as discussed in [9], [15] is approximated by

\[ SR = V_{eff1} \frac{g_{m1}}{C_C}, \]  

(4.19)

\[ V_{eff1} = V_{GS} - V_{TH1} = \sqrt{\frac{2I_D}{\mu p C_{ox} W_1 L_1}}, \]  

(4.20)

\[ = 2\eta V_T \ln (\exp(\sqrt{IC}) - 1). \]  

(4.21)

From Eq. 4.17, it is clear that with the increase in \( V_{eff} \) slew rate increases. p-channel input transistors for the first stage have a larger \( V_{eff} \) than would be the case for n-channel transistors (assuming similar maximum widths are chosen to maximize the gain) [9]. The nonlinearity factor (substrate factor) \( \eta \) of p-channel transistors is also slightly higher than the n-channel transistors [15].

### 4.4 Constant-\( g_m \) biasing circuit

Since the \( g_m \) of the input driver of the differential stage has a significant effect on the overall gain of the stage, it is very critical that the \( g_m \) of these devices do not change much over the process and temperature corners.

The circuit shown in Fig. 4.5 provides a constant \( g_m \) for the device M6 and other devices biased by current \( I_{out1} \) over any variations in MOS device parameters. Devices M1 - M4 are matched with targeted devices M9 - M12 for which the constant \( g_m \) over the corners is deemed. It can be shown that [19]

\[ I_{OUT1} = \frac{2}{\mu n C_{ox}(\frac{W}{L})R_2^2} \left(1 - \frac{1}{\sqrt{2}}\right)^2, \]  

(4.22)
Figure 4.5: Constant-$g_m$ biasing circuit

\[ g_{m6} = \sqrt{2\mu_n C_{ox} \left( \frac{W}{L} \right)} I_{D6} \]

\[ = \frac{2}{R_2} \left( 1 - \frac{1}{\sqrt{2}} \right). \quad (4.23) \]

The above equation for $g_{m6}$ is free of any device parameters. MOS device M7 acts as a capacitor and resolves the start-up issue if present in constant-$g_m$ biasing circuit. The circuit can settle into one of two different operating conditions: zero current condition and $I_{OUT1} \neq 0$. 
The start-up problem arises whenever all the MOS devices carry zero current when the power supply is turned on, that is, the loop carries a zero current and the circuit can be stable but with device M7 acting as a capacitor it injects enough current in the loop to rejuvenate the circuit out of the zero current state.

The other such constant-$g_m$ biasing circuit shown in Fig. 5.2 that uses the same approach as mentioned earlier is used to bias the control circuit (explained in a later section) of the amplifier.

4.5 Class AB output stage

The Class AB circuit shown in Fig. 4.6 forms the output stage of the proposed design. Since the higher portion of the overall voltage gain came from the input differential stage ($> 95$ dB), low voltage gain ($10$ dB $\sim 15$ dB) is needed from this stage. The class AB stage is used as opposed to class A or class B stage as the efficiency of this stage is near that of a class B stage, and gets rid of any dead zones when transitioning between the pull up and pull down operation. All the devices are biased to operate in their active regions. Devices M20 and M19 comprise a circuit for a level shifter that controls the quiescent current in device M21 for low power dissipation when the circuit is not amplifying. Since the gain of the level shifter is not exactly unity, the half wave symmetry of the output signal during the pull up and the pull down operation might differ slightly introducing low distortion in the output signal which is negligible. The voltage gain for the pull up and pull down operation of this stage can be approximated by

Pull up:

\[ A_{MB} = - \left[ g_{m21}(r_{ds21}|r_{ds22}) \left( \frac{r_{ds19}}{r_{ds19} + \frac{1}{g_{m20}}} \right) \right], \quad \text{(4.24)} \]

and Pull down:

\[ A_{MB} = - \left[ g_{m22}(r_{ds22}|r_{ds21}) \right]. \quad \text{(4.25)} \]
Lower gain is sought for this stage as it maximizes the bandwidth. Higher bandwidth places the pole from this stage at a much higher frequency compared to the pole of the input differential stage that improves the phase margin of the op amp.

### 4.6 Compensation procedure for op amp stabilization

Op amps are used in negative feedback for amplification and are generally internally compensated to overcome unstable behavior. In Fig. 4.7, the two conditions that may cause oscillations are as follow [20]:

![Figure 4.6: Class AB output stage](image-url)
• The angle of $AF$ is $0^\circ$ or some multiple of $360^\circ$.

where the Feedback factor ($F$) is,

$$F = \frac{R_2}{R_2 + R_F} \quad (4.26)$$

and the Gain of the op amp is $A$.

• $|AF| \geq 1$.

In words, the loop gain $AF$ can cause oscillations only if it has a $0^\circ$ (or $360^\circ$) phase shift and the magnitude of $AF$ is unity or greater. The stability of the op amp is tested with the unity feedback condition (worst case scenario) and a phase margin of at least $45^\circ$ insures the stability of the op amp. Phase margin (measured in degrees) is the difference between the phase of an amplifier’s output signal and $180^\circ$ at the frequency where the loop gain of the op amp is unity. A negative phase margin at a frequency where the loop gain exceeds unity guarantees instability and hence positive phase margin is desired. A phase margin of $60^\circ$ is better as it provides a faster settling time for a step response.

Since no compensation capacitor along with the resistors are used to compensate the proposed op amp, the sizes of the devices in the input differential stage and Class AB output stage are optimized for better phase margin and gain margin to insure the stability of the op amp in unity feedback. In Fig. 4.4, devices M13 and M14 in the input differential stage are chosen to be quite wide to increase the transconductance of these devices. Since the effective
resistance \( R_m \), looking into the junction of the drains of M11 and M13 is dominated by the reciprocal of \( g_{m13} \) (impedance of diode-connected device M13), an increase in \( g_{m13} \) decreases the \( R_m \) but wider devices (M13 and M14) also increase the effective capacitance \( C_m \). The increase in transconductance of M13 dominates the increase in \( C_m \). Since the placement of the mirror pole in the frequency domain depends upon these parameters, \( R_m \) and \( C_m \), a decrease in the time-constant places the mirror pole at higher frequencies away from the pole of the input differential stage. Wider M14 also increases the parasitic capacitance of M14 that helps in narrow-banding the dominant pole of the this stage. The sizes of devices M15 and M16 in the composite cascode load are chosen to be longer as this increases the effective resistance looking into the drain of M13 and M14 which increases the voltage gain of the stage.

As mentioned earlier the size of the devices in the output stage are optimized to give a low voltage gain of about (10 dB ~ 15 dB) resulting in higher bandwidth of the stage. The higher bandwidth in this stage diminishes the effect of the pole from this stage and the input differential stage which results in better phase margin \( 75^\circ \) required for the stability of the op amp.

### 4.7 Control circuit

The control circuit shown in Fig. 4.8 diminishes the change in gate to source voltage \( V_{GS} \) of device M20 in the quiescent state over the process and temperature corners. Simulation results show that in the absence of this circuit the maximum quiescent power dissipation of the op amp over the corners is about 84 \( \mu W \) as opposed to 35 \( \mu W \) when this circuit is included. Over corners, the threshold voltage of device M20 varies which varies the bias voltage of device M21 driving more current into the load. In the circuit shown, devices M20 and M26, M22 and M28, M19 and M23, and M21 and M25 are matched and the circuit is biased in such a manner that the node \( V_X = V_Y \) and \( V_Q = V_R \).

In order to understand the circuit in detail, suppose the voltages at node \( V_X \) and \( V_Y \) increase over the corner in a quiescent state. As \( V_Y \) increases, the gate to source voltage of device M26 drops and drives the source voltage of M26 (M37) higher as more current flows through the device M37. With the increase in the drain current through the device M37 the
drain and gate voltages of devices M32 and M24 increases. The high gate voltage of device M24 also drives the device’s respective source voltage high. The increase in gate voltage of device M19 and source voltage of device M24 decrease the drain current in M19, thereby decreasing the $V_{GS}$ of device M20 by the same amount as the voltages at node $V_X$ and $V_Y$ increase over the corner keeping the voltages at nodes $V_Q$ and $V_R$ equal.
Chapter 5

Layout of proposed operational amplifier

Layout of any circuit plays an important role in the behavior of a final integrated circuit. It is the representation of the integrated circuit at the transistor level in terms of planar geometrical shapes; these shapes are composed of different combinations of layers of silicon, silicon oxide, diffusion, metal and polysilicon. The layout of an integrated circuit is broken down into certain blocks of components that comprise the integrated circuit and the connections and positions of these blocks significantly affect the behavior of the integrated circuit in the physical world. Certain guidelines are followed while designing the layout of these blocks such as matching of transistors, use of dummy devices, shielding and guard rings.

The layout of the proposed op amp follows some of the above mentioned key guidelines as required to ensure acceptable performance. Fig. 5.1 shows the layout of the op amp. The highlighted areas in the layout; A, B, C and D represent the first stage, constant-$g_m$ biasing circuit of the first stage, second stage along with the control circuit and constant-$g_m$ biasing circuit for the control circuit of the proposed op amp respectively. All of the respective transistors with equal width and length are matched to minimize the effects of the process variation. Certain common techniques are used to match such devices to compensate for boundary conditions such as representation of larger devices using unit fingers, use of dummy devices, device orientation, interleaving, cross quadding, and locality of the devices. Extra care was taken to make sure the current flow is identical throughout the current mirror devices and any other devices that required matching, this technique is also called photolithographic invariance. The total area of the layout is 0.129 mm$^2$, but with some optimizations the layout could be more compact. Figure. 5.2 shows the schematic of the overall op amp consisting of the stages discussed in Chapter 4.
Figure 5.1: Layout of proposed operational amplifier
Figure 5.2: Proposed design of amplifier
Chapter 6

Simulation setup and results of proposed operational amplifier

This chapter includes the simulations of the proposed op amp to characterize and optimize its operation. These simulations are divided into three sections; small signal AC, large signal transient and DC responses. All of the op amp simulations were performed with a resistive load of 100 kΩ in parallel with a capacitive load of 0.5 pF. AVDD is the positive power supply and AVSS is the negative power supply.

6.1 DC response

DC analysis ensures the correct biasing of the op amp in a quiescent state. It also characterizes the total power dissipation of the op amp in a quiescent state and the output offset that the op amp incurs due to mismatch of the involved transistors and other parasitics. Fig. 6.1 shows the setup circuit to measure the offset voltage and the total quiescent current consumption by the op amp. The DC response showed the total current consumption in the quiescent state to be 9.376 µA and the offset voltage to be 3.223 µV.

6.2 Small signal AC response

The small signal AC response examines the response of the op amp to a small sinusoidal voltage imposed upon a generally much larger DC bias voltage. This response can be characterized by the voltage gain, bandwidth, phase margin, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) and noise analysis of the op amp.

6.2.1 Open-loop gain, bandwidth and phase margin

Figure. 6.2 shows the setup for characterization of the open-loop voltage gain and bandwidth of the op amp shown earlier in Fig. 5.2. The open-loop gain of the op amp in
dB is given by \[20 \log \left(\frac{V_{OUT}}{V_{in+} - V_{OUT}}\right)\]. Figure 6.3 shows the frequency response of the first and second stage of the op amp and Fig. 6.4 shows the frequency response of the op amp along with the phase plot. The simulation results show that the gain of the first stage is
approximately about 98 dB with a bandwidth \((f_{21})\) of about 1.07 Hz and the second stage has a gain of about 13 dB with a bandwidth \((f_{22})\) of about 4.9 MHz. The simulated results clearly show the pole from the first stage being much lower than the other pole which insures the stability of the op amp. The phase and gain margin of the op amp are about 75\(^0\) and 17.65 dB respectively. The gain margin is the factor by which the op amp gain can be increased before the op amp becomes unstable. The simulated overall voltage gain of the op amp is about 113.4 dB with a crossover frequency at 311 kHz.

![Figure 6.3: Frequency response for the open-loop gain and bandwidth of the output loaded first and second stages respectively. Red color denotes the first stage gain and the blue denotes the second stage gain. Scaling in Y-axis is in dB and X-axis is in Hz.](image)

**Figure 6.3:** Frequency response for the open-loop gain and bandwidth of the output loaded first and second stages respectively. Red color denotes the first stage gain and the blue denotes the second stage gain. Scaling in Y-axis is in dB and X-axis is in Hz.
Figure 6.3 shows that the first stage frequency response has a zero at about 10 MHz which explains the small bump in the overall frequency response of the op amp shown in Fig. 6.4. This zero is coming from the feedback capacitance $C_{gd}$ of device M14 in Fig. 4.4. Since this bump is farther away from the cross over frequency and does not hurt the phase and gain margin much, it can be ignored.

Figure 6.4: Frequency response for the open-loop gain, bandwidth, phase margin and gain margin of the loaded op amp. Scaling in Y-axis is in dB and X-axis is in Hz for the Amplitude (Gain) response and is in deg (degrees) and Hz for the Phase response.
6.2.2 Noise analysis

Figure 6.5 shows the output voltage noise spectral density of the op amp. It is a measurement of root-mean-square noise voltage per square root Hertz. The simulated results shows two types of noise, $\frac{1}{f}$ noise and white noise, a flat spectral noise density above 1 Hz is a white noise. The plot below 1 Hz which is inversely proportional to frequency is referred to as $\frac{1}{f}$ noise. The intersection of the $\frac{1}{f}$ noise and the white noise is often referred to as $\frac{1}{f}$ noise corner and it occurs at about 4 mHz. The spectral noise density at 1 KHz is about 134.5 nV/$\sqrt{\text{Hz}}$.

**Figure 6.5:** Noise analysis at the output of the op amp
6.2.3 Common mode rejection ratio (CMRR)

CMRR is a measure in dB of the mismatch of incremental gain from each of the two inputs to output of the op amp. If the incremental gain from each input to output were equal, the CMRR would be infinite [14]. CMRR can also be defined as the measure of the tendency of the op amp to reject the input signals common to both inputs. Fig. 6.6 shows the setup for the characterization of CMRR of the op amp. The CMRR of the op amp is given by

\[
CMRR = 20 \log \left( \frac{|A_D|}{|A_{CM}|} \right) \quad (6.1)
\]

\[
= 20 \log \left( \frac{V_{CM}}{V_p - V_n} \right). \quad (6.2)
\]

\(A_D\) and \(A_{CM}\) are the differential gain and the common mode gain of the op amp respectively. It can be seen from Eq. 6.1 that the higher the CMRR is, the smaller is the effect of \(A_{CM}\) on the output voltage compared to \(A_D\).

Figure 6.6: Setup for Common-mode gain measurement
Figure 6.7 shows the frequency response for the CMRR of the op amp. The simulated results show that at lower frequencies the CMRR is quite high, about 132 dB, and starts to fall off above 1 Hz as the differential gain falls. The CMRR of the op amp at 1 KHz is about 92.49 dB.

![Figure 6.7: Frequency response for the measurement of the CMRR of the op amp. Y-axis is in dB whereas X-axis is in Hz.](image-url)
6.2.4 Power supply rejection ratio (PSRR)

PSRR (measured in dB) is the ratio of change in the input offset voltage to a unit change in the power supply voltage [14]. PSRR can also be defined as the measure by which the ripple in the power supply is rejected by the op amp at its output. Figure 6.8 shows the setup for the characterization of PSRR of the op amp.

![Figure 6.8: Set up for PSRR response of the op amp.](image)

Figure 6.9 shows the frequency response for the PSRR of the op amp. The simulated results shows that at lower frequencies the PSRR is about 131 dB and at 1 KHz, it is about 73.6 dB.
**Figure 6.9:** Frequency response for the measurement of the PSRR of the op amp. Y-axis is in dB whereas X-axis is in Hz.
6.3 Large signal transient response

Large signal transient response examines the response of the op amp to a change from a quiescent state. This response characterizes the slew rate and total harmonic distortion of the op amp.

6.3.1 Slew rate

Slew rate is the maximum rate at which the output changes when input signals are large. Figure 6.10 shows the setup for the characterization of the slew rate of the op amp.

![Figure 6.10: Setup for slew rate response of op amp](image)

Figure 6.10: Setup for slew rate response of op amp

Figure 6.11 shows the response of the op amp to an input ramp signal. The rate at which the output signal changes with respect to the input signal is measured to be about 170 KV/s.
6.3.2 Total harmonic distortion (THD)

THD is a major specification used to characterize the op amp performance. Ideally the output signal of an op amp should contain only the frequency components present in the input signal. But the nonlinear nature of the amplifying devices introduces extraneous frequencies in the output signal that are not contained in the input signal, also referred to as harmonics [20]. Nonlinearity is introduced in the MOSFET between the gate voltage and the drain current. THD can be defined as a percentage by [20]

\[
THD = \sqrt{\frac{v_2^2 + v_3^2 + v_4^2 + \cdots + v_n^2}{v_f}}. \tag{6.3}
\]
In Eq. 6.3, $v_f$ is the fundamental frequency and $v_2$, $v_3$ and $v_n$ are the amplitudes of the respective harmonics. Fig. 6.12 shows the setup for the characterization of the THD. Using a calculator tool in Cadence with Spectre, the THD was calculated for 10 periods of fundamental frequency (4 KHz) and found to be 0.38% in unity gain feedback.

![Figure 6.12: Setup for Total harmonic distortion measurement](image-url)

Figure 6.12: Setup for Total harmonic distortion measurement
Chapter 7

Test results of operational amplifier

The proposed op amp was fabricated in an ON Semiconductor 0.5-\(\mu\)m CMOS process. Since the proposed op amp can drive a maximum capacitive load of about 0.5 pF without affecting its stability and performance and the testing probes introduce a capacitance of about 20 pF which can significantly affect the performance of the op amp, a new approach was taken to test the op amp. The proposed op amp was cascaded with the buffer amplifier that can drive a capacitive load of more than 20 pF. The buffer amplifier needs to be significantly faster than the proposed op amp such that in a unity feedback (worst case scenario) this buffer does not affect the stability, accuracy, and speed of the op amp.

Figure. 7.1 shows the setup for the testing of the proposed op amp for most of the responses mentioned in Chapter 6. Due to the constraint in resolution of the measuring equipment and inability to produce a noise free small input signal, the open loop voltage gain was hard to measure. Figure. 7.2 shows the setup for testing the open loop voltage gain of the proposed op amp. From Fig. 7.2, applying Kirchhoff node voltage analysis at \(V_1\) gives

\[
V_1 = \left( \frac{R_2}{R_1 + R_2} \right) V_x, \quad (7.1)
\]

\[
A = - \frac{V_{OUT}}{V_1} = - \left( \frac{R_1 + R_2}{R_2} \right) \frac{V_{OUT}}{V_x}. \quad (7.2)
\]

Resistor values of 100 K\(\Omega\), 500K \(\Omega\), and 100 \(\Omega\) were chosen for \(R\), \(R_1\) and \(R_2\) respectively for the measurement of the gain. From Eq. 7.2 the first term, \((R_1 + R_2)/R_2\), of the gain \(A\) can be considered as a constant and the \(V_{OUT}\) and \(V_x\) signal are large enough to be accurately measured by the measuring equipment.

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The accuracy of the other measurements, CMRR and PSRR, of the op amp also depended on resistor matching and the accuracy of the measuring equipment. An earlier work [21], shows that the highest achievable CMRR of op amp with the resistors mis-match within 0.001% is 86 dB. With better precision resistors, the reported CMRR of the op amp in this thesis could be much higher. Similarly for the measurement of PSRR, the accuracy of the measuring equipment is critical in evaluating the voltage changes in the output with respect to the changes in power supply. Again with better accuracy equipment, the reported PSRR could be higher.

The test results agree with the simulation results of the op amp. The measured open loop gain, gain bandwidth product, power dissipation, and total harmonic distortion is about 110 dB, 420 KHz, 21.3 $\mu$W and 0.215 % respectively. The lower power dissipation is due to the lower quiescent current required to bias the first stage of the op amp ($< 200$ nA). Table 7.1 shows the comparison between the simulation and test results. The results were also compared with the op amp mentioned in [1] which formed a basis of this thesis. The key topic of interest were low power design, elimination of the compensation capacitor and reduction in chip area. The test results show that the power dissipation is much lower at about 21.3 $\mu$W compared to the op amp mentioned in an earlier work [1] which was about 110 $\mu$W. The other improvement was seen in the slew rate measurement, the measured slew rate is about 280 KV/s as compared to 260 KV/s mentioned in [1]. This improvement in slew rate can be explained due to the elimination of the compensation capacitor as mentioned in Chapter 3. In contrast, the layout area ($\sim 0.12 \text{ mm}^2$) turned out to be higher as compared to the op amp mentioned in [1] ($\sim 0.05 \text{ mm}^2$) which is due to the introduction of Constant-$g_m$ biasing circuit for the first stage and the large sizes of the devices in the first stage of the op amp operating in the subthreshold region. The monte-carlo simulation results showed variation in voltage gain of the first stage over the mismatch of these devices which were unjustified. Further investigation showed no variation in the $g_m$ and $g_{ds}$s of the devices in the first stage, yet the gain varied so the BSIM3 modeling of the subthreshold devices is suspected for such results. The variation in gain severely affected the stability of the op amp, and to minimize the effect large device sizes were chosen which also introduced larger parasitic capacitance that helped in narrow banding the first stage increasing the stability.
of the op amp. The constant-g\textsubscript{m} biasing circuit was also used to keep the g\textsubscript{m} of these devices fairly constant over mismatch and process corners. With better understanding of the models of the device in subthreshold region, the device sizes can be reduced and could be a topic for future research.

Table 7.2 compares and shows that the proposed op amp in this thesis has achieved appreciable performance when compared to the previously published op amps for the application in biomedical fields. The gain is comparatively high and the low power dissipation of the op amp makes it an ideal candidate for use in neurophysiology laboratories, biomedical sensors such as heart rate sensors, ECG sensors, and EEG sensors.

7.1 Comparison tables

The comparison between the simulated and the test results of the proposed op amp is summarized in Table 7.1. Table 7.2 compares the key parameters related to the performance of the proposed op amp with the previously published op amp for the application in biomedical fields.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation Results</th>
<th>Test Results</th>
<th>Units</th>
</tr>
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<tr>
<td>Power Supply</td>
<td>± 1.5</td>
<td>± 1.5</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent DC current</td>
<td>9.37</td>
<td>7.1</td>
<td>µA</td>
</tr>
<tr>
<td>No signal Power dissipation</td>
<td>28.11</td>
<td>21.3</td>
<td>µW</td>
</tr>
<tr>
<td>Input voltage offset</td>
<td>3.223</td>
<td>119</td>
<td>µV</td>
</tr>
<tr>
<td>Open loop Gain</td>
<td>113.4</td>
<td>110</td>
<td>dB</td>
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<td>Open loop Bandwidth</td>
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<td>1</td>
<td>Hz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>75</td>
<td>⋯</td>
<td>degrees</td>
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<td>Gain bandwidth product (GBW)</td>
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<td>Spectral Noise Density @ 1KHz</td>
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<td>⋯</td>
<td>nV/√Hz</td>
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<td>CMRR</td>
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<td>PSRR</td>
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<td>mm\textsuperscript{2}</td>
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Table 7.1: Comparison between the simulation and test results
Table 7.2: Comparison between the performance of the presented op amp and the previously published op amp

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>[23]</th>
<th>[3]</th>
<th>This Work</th>
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<td>Low Power Band-Pass Amplifier</td>
<td>Low-Power Low-Noise CMOS Amplifier</td>
<td>High Gain, Low Power CMOS Op amp</td>
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Figure 7.1: Setup for testing of proposed op amp
Figure 7.2: Setup for testing of open loop gain of proposed op amp
Chapter 8

Conclusion

This work demonstrates the feasibility of the composite cascode connection, operating in the subthreshold region, for the input differential stage of an op amp. The resulting amplifier has a high gain, low bandwidth and low quiescent power dissipation while eliminating the need for the addition of a compensation capacitor. The results also show that it has low nonlinear distortion and noise. When compared with previously published op amps for its application in the biomedical field, the proposed op amp showed appreciable performance in terms of power dissipation, gain and area. As mentioned in Chapter 5 and Chapter 7, the area could be further reduced with optimization of the layout and a better understanding of BSIM3 subthreshold models of devices. The significant use of such an amplifier can be found in biomedical applications where low power, low noise bio-signal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range are required. Low quiescent current amplifiers are also in demand for application in biomedical devices like the pulse oximeter. The high gain and the low power dissipation of the op amp also makes it an ideal candidate for use in neurophysiology laboratories, biomedical sensors such as heart rate sensors, ECG sensors, and EEG sensors.

8.1 Topics for future research

As mentioned in Chapter 7, the poor modeling of the devices in the subthreshold region in Cadence introduced unjustified results, a better understanding of these models can be helpful in predicting the behavior of these devices in subthreshold region. The op amp proposed in this thesis can drive a capacitive load of about 0.5 pF, further research can be done such that this op amp can drive a much larger capacitive load. The output voltage swing is about 2.1 V_{pp} with a power supply of 3 V. Further research in maximizing
this output voltage (rail-to-rail) will increase the op amp efficiency. With the elimination of the compensating capacitor, the slew rate should have been much higher than reported in Chapter 7, further research on this issue could be beneficial. The reported power dissipation of the op amp is about 21.3 µW, most of which is dissipating in the control circuit and the Class AB output stage, further research on the more efficient output stage could decrease the power dissipation.
Appendix A

A.1 Derivation of the small signal voltage gain of composite cascode stage with composite cascode load

Figure A.1: Small signal model of composite cascode stage with ideal current source load, R represents the effective resistance of ideal current source
From Fig. A.1, applying Kirchhoff node voltage rule at $V_X$ gives

$$\frac{V_X}{r_{01}} - g_{m1}V_{SG1} + \frac{V_X - V_{OUT}}{r_{ds2}} + g_{m2}V_{SG2} + g_{mb2}V_{S2} = 0, \quad (A.1)$$

$$V_X \left( \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} \right) - \frac{V_{OUT}}{r_{ds2}} - g_{m1}(-V_{IN}) + g_{m2}(V_X - V_{IN}) - g_{mb2}V_X = 0,$$

$$V_X \left( \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} + g_{mb2} \right) - \frac{V_{OUT}}{r_{ds2}} + (g_{m1} - g_{m2})V_{IN} = 0,$$

$$V_X = \frac{V_{OUT}}{r_{ds2}} - (g_{m1} - g_{m2})V_{IN} \left( \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} + g_{mb2} \right). \quad (A.2)$$

Again applying Kirchhoff node voltage rule at $V_{OUT}$ gives

$$\frac{V_{OUT}}{R} - g_{m2}V_{SG2} + \frac{V_{OUT} - V_X}{r_{ds2}} - g_{mb2}V_{S2} = 0, \quad (A.3)$$

$$V_{OUT} \left( \frac{1}{R} + \frac{1}{r_{ds2}} \right) - g_{m2}(V_X - V_{IN}) - \frac{V_X}{r_{ds2}} - g_{mb2}V_X = 0,$$

$$V_{OUT} \left( \frac{1}{R} + \frac{1}{r_{ds2}} \right) + g_{m2}V_{IN} = \left( (g_{m2} + g_{mb2}) + \frac{1}{r_{ds2}} \right) V_X.$$

Substituting for $V_X$ from Eq. A.2 and after some simplification,

$$V_{OUT} \left[ \frac{1}{R} \left( \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} + g_{m2} + g_{mb2} \right) \right] = -g_{m1}V_{IN} \left( g_{m2} + g_{mb2} + \frac{1}{r_{ds2}} \right) - \frac{g_{m2}V_{IN}}{r_{ds1}},$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{1}{\frac{1}{R} \frac{1}{r_{ds1} r_{ds2}} \left[ g_{m1} \left( g_{m2} + g_{mb2} + \frac{1}{r_{ds2}} \right) + \frac{g_{m2}}{r_{ds1}} \right]} \frac{1}{r_{ds1} r_{ds2}}, \quad (A.4)$$
Similarly, the voltage gain of the composite cascode stage with composite cascode load as in Fig. 4.3 can be derived to yield

$$A_{MB} = \frac{-[g_{m1}(g_{m2} + g_{mb2})r_{ds2} + g_{m1}r_{ds1} + g_{m2}r_{ds2}]}{1 + \frac{1}{R}[g_{m2} + g_{mb2})r_{ds1}r_{ds2} + r_{ds1} + r_{ds2}]}.$$  \hspace{1cm} (A.5)
Bibliography


