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Diode Properties of Nanotube Networks

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ABSTRACT

Single-walled carbon nanotubes (SWCNT) were prepared using iron catalysts deposited by indirect evaporation on silicon substrate covered with 500 nm-thick thermal oxide. Diode SWCNT devices have been fabricated using Au and Al, as the asymmetric metal contacts, and a random network of metallic and semiconducting nanotubes as the device channel. No effort was made to align the SWCNTs or to eliminate metallic nanotubes in our devices. Asymmetric voltage-current behavior was seen. Current rectification was observed in the source-drain bias range of -3 V to +3 V. Rectification was somewhat surprising since, although metallic tubes are in the minority (~ 1/3), they could potentially act as shunts and mask the electric properties of the semiconducting majority. No correlation between electrode spacing and current rectification was observed. The lowest leakage current measured was 1% of the maximum current carrying capacity. Maximum forward-biased current capacities range between 8 μA and 841 μA.

INTRODUCTION

Diodes and transistors are the building blocks of modern electronics. Ever since their invention, technologists have tried to put more and more transistors into smaller and smaller areas. Silicon is the standard material for building transistors, but it is being pushed to its limits. In order to continue progression into the nanoelectronic regime it is necessary to find a replacement for silicon [1].

Carbon nanotubes (CNTs) are an excellent replacement candidate for several reasons. One particularly promising characteristic of CNTs is their near ballistic transport [2], making them a very low-power alternative. Also, there is no chemical passivation necessary in CNTs as there is in silicon and many other materials [2]. This allows CNTs to be used with a variety of different insulators including flexible substrates [3]. Another advantage is the current densities CNTs can withstand. They have been shown to exhibit current densities as high as $10^9 A/cm^2$ as compared to $10^3 A/cm^2$ for silicon [2]. CNTs also have very large mobility which can lead to high-speed devices [4].

One major obstacle to the integration of nanotubes in electronics is the present inability to control their conduction properties during the growth process. One way to harness the compelling characteristics of CNTs without many of the difficulties associated with them is by utilizing CNT networks. No nanotube isolation or alignment is necessary. As-grown nanotube networks consist of 1/3 metallic tubes and 2/3 semiconducting tubes. In spite of their metallic components, the network as a whole acts as p-type semiconductor [3]. Additionally, very low CNT-CNT junction resistances between semiconducting tubes result in only minor reductions in current [5]. The following experiment shows that carbon nanotube networks provide a simple and inexpensive way to implement CNTs into macroelectronics. Five devices on two different chips were tested and their electronic properties characterized.

DEVICE FABRICATION

The device preparation process consists of three main steps: iron catalyst deposition, nanotube-mat growth, and electrical-contact deposition. The single-walled CNTs (SWCNTs) were grown using an iron catalyst, chemical vapor deposition (CVD) process. The devices were fabricated on a 1 cm^2 substrate of single crystal silicon (100) orientation with an approximate 500 nm-thick thermal oxide. As discussed below, the silicon substrate is degenerately doped and can be used as a gate electrode. This process was developed at the Goddard Space Flight Center (GSFC) but has been successfully replicated at Brigham Young University (BYU). The fabrication process is outlined in general and only important differences in processing between the two locations are noted.

In order to grow nanotubes a very thin layer of iron catalyst is required. This layer is on the order of 1 nm. Conventional thermal evaporation, with the substrate facing the source, presents several difficulties in achieving ultrathin films. In order to avoid the difficulty in obtaining ultra thin films associated with this method we employed a method developed at the GSFC known as indirect evaporation [6].

In contrast to traditional, direct thin-film evaporation, indirect evaporation was accomplished by orienting the targeted surface of the substrate *away* from the iron source. The direct path from the source to the substrate was blocked by the sample holder, and no shutter was used. Iron was evaporated at a rate of 0.05 nm/s to a thickness of 1-1.5 nm according to the thickness monitor, which was water cooled. Iron reached the targeted surface through collisions with nearby surfaces within the chamber and, to lesser extent from residual gas molecules. It should be noted that the thickness measured by the thickness monitor is necessarily much greater than the actual thickness on the targeted surface. The chamber pressure was approximately 1.3×10^{-4} Pa at the beginning of the iron deposition. This method has been implemented at

GSFC and at BYU, the robustness of the technique to variations in experimental conditions has been demonstrated. Growths have also been achieved with a wide range of different crystal-monitor thicknesses (1.5-8 nm).

Following the catalyst deposition, the nanotubes were grown in a CVD furnace by flowing carbon rich gases under high temperatures. The initial devices were fabricated at GSFC. The substrate was placed in a quartz boat, catalyst side up, and inserted into a 1" quartz tube in a 3-zone tube furnace (Lindberg, model number 55367) with a 58434-P temperature controller. Subsequent devices were fabricated entirely at BYU; the nanotubes for these devices were grown in a single-zone furnace using the same process. After purging atmospheric gases with flowing Ar, the substrate was heated to 950˚C [6]. After a 5-minute soak in a hydrogen atmosphere, SWCNT growth was achieved by flowing methane, ethylene, hydrogen and humid argon (bubbled through water) over the substrate for 5 minutes [7]. (Flow rates were 1200, 50, 2000 and 730 sccm, respectively). The resulting growth networks were then imaged via scanning electron microscopy (SEM), equipped with an in-lens detector, for qualitative comparisons. The in-lens detector is known to cause nanotubes to stand out but also exaggerate their width [8]. At GSFC a LEO Supra 50VP system was used, and at BYU we used a FEI XL30 SFEG. The reproducibility of the indirect catalyst deposition method suggests that it is an inexpensive and effective means of reliably growing carbon nanotube networks; the techniques and results shown herein are expected to be largely facility-independent. Figures 1a and 1b are SEM images of nanotube growths, from both facilities.

Following the nanotube growth and its verification through SEM, asymmetric metal contacts were deposited as reported in the literature [10]. We deposited aluminum to act as the rectifying contact and gold as the ohmic contact [11]. This combination has been shown to rectify current when a single SWNT was contacted between the two electrodes [10]. Our goal was to achieve similar rectifying behavior using a composite network of overlapping

semiconducting and metallic tubes. Using parallel-bar grids (Electron Microscopy Sciences) and covering half of the grid with a shadow mask, we deposited a set of aluminum electrodes using thermal evaporation. We then covered the other half of the grid in order to deposit a set of gold electrodes. Figures 2a, 2b and 2c are optical images of completed devices.

After device fabrication was complete we prepared the devices for electrical characterization. First we removed the nanotubes from the perimeter of the silicon chip to prevent electrical shorting from the nanotubes to the bare silicon when performing gate voltage dependence experiments. They can be removed simply by scratching a 3 mm perimeter around the edge of the silicon chip, taking care to avoid breaking through the oxide. The substrate was then attached to a chip carrier. We used silver paint in order to connect one of the inputs of the chip carrier to the substrate in order to use the silicon as a back gate. At GSFC we used a Kulicke & Soffa 3523A Digital Wire Bonder to contact the devices, while at BYU the electrodes were contacted directly using tungsten probes.

EXPERIMENT AND DISCUSSION

After the devices were fabricated we took pictures of the samples to relate devices' electronic properties with their physical characteristics. Using a probe station we plotted output current versus source-drain voltage in the range -3 V to 3 V. Two or three repeated sweeps were conducted to ensure reproducibility. This scan covers both the forward- and reverse-bias modes of these devices. Forward bias is defined as the case when the gold electrode is positive with respect to the aluminum electrode. We expected to see Schottky diode-like behavior similar to that reported in the literature [10]. Current rectification was observed but did not resemble typical nonlinear Schottky diode behavior. It was linear in forward bias.

Figure 4 shows the current-voltage characteristics of two devices from a single silicon chip (figure 2a). Device 1 has an electrode spacing of 289 μm. The ratio of the maximum forward-bias current to the maximum reverse-bias current is 20, commonly known as the on/off ratio.

The maximum forward-bias current is 8 μA. Device 2, with an electrode spacing of 219 μm, only exhibited an on/off ratio of 5 and a maximum forward-bias current of 22 μA.

In addition to the two devices fabricated at GSFC, four additional devices were fabricated at BYU on a single substrate (figures 2b and 2c). The processing on these devices was similar to the other devices but there are some important differences. The thicknesses of the aluminum and the gold are visibly thicker than those of previous devices regardless of the similar thicknesses reported by the thickness monitors (perhaps due to discrepancies in tooling factors). Additionally, the thickness of the gold and aluminum are not equal. There is about twice as much aluminum as gold based on comparing thickness monitor readings. This difference accounts for the poor focusing in figures 2b and 2c. None of these devices were wire bonded they were characterized using tungsten probe needles. Another difference between the two sets of devices is the nanotube network itself. The nanotube mat used for devices 3-6 is significantly less dense and there are larger iron-containing particles on the surface. These particles appear as bright spots when close to the conducting nanotubes and dark spots when farther away [6]. (Compare figures 1a and 1b). Lastly, the contacts were deposited so that the distance between the electrodes increased from top to bottom (See figure 2b and 2c). The higher on/off ratio for the larger electrode spacing in devices 1 and 2 above suggested that this parameter might be important. The current-voltage (I-V) plots of these devices are found in figures 4b and 4c.

Although none of the devices have I-V curves typical of conventional Schottky diodes, two distinct tests reinforce our conclusion that these are semiconducting devices. First, current rectification as displayed in figure 4, is indicative of the semiconducting nature of the two devices. Furthermore, device 1 exhibited gate-voltage dependence in the following experiment.

Applying a gate voltage to this device makes it act as a transistor. We applied a gate voltage by contacting the silicon and relying on the silicon dioxide layer to act as the isolating dielectric between the applied voltage on the back and the SWCNT device on the front (figure 3).

The I-V response of device 1 was measured by applying a variable gate voltage with a fixed source-drain voltage. All of the measurements were made at a constant source-drain voltage of +3 V. The gate voltage was varied from -10 V to 10 V.

Figure 5 shows the current as a function of gate voltage. As the gate voltage increases in the positive direction, the current decreases. The gate bias produces an electric field which depletes the semiconducting nanotube mat of carriers. Fewer carriers mean less current. As the voltage increases in the negative direction, more carriers are introduced and so the current increases. Another prominent feature in figure 5 is hysteresis. That the current-voltage relationship is multivalued is evidence of charge trapping in the nanotube structure [12].

Here, we estimate the carrier mobility of our nanotube network devices to quantify the degradation of device properties due to ensemble effects, compared to optimized device performance. We can determine the field effect mobility by examining the change in device conductance with gate voltage, according to

$$\mu = \frac{L}{c_g}\frac{\partial G}{\partial V_g}, \qquad (1)$$

where μ is the field effect mobility, L is the device length, c_g is the gate capacitance per unit length, G is the device conductance, and V_g is the gate voltage. For a single nanotube and a similar gate dielectric and geometry, c_g has been reported as190 fF/cm. The capacitance must be scaled according to the number of nanotubes, semiconducting and metallic, forming the device. Based on scanning electron micrographs, we estimate the average number of nanotubes contributing to the device to be of order 2000. Adding the parallel capacitances together, we obtain a total capacitance per unit device length to be 190 fF/cm x 2000 nanotubes = 380 pF/cm. For a device length of 300 μm, then, we can estimate that device 1 exhibits a field effect mobility of 0.268 cm^2/V-s which is comparable to other organic thin film transistors formed on an SiO_2 substrate [13].

CONCLUSION

Diode SWCNT devices have been fabricated using Au and Al, as the asymmetric metal contacts, and a random network of metallic and semiconducting nanotubes as the device channel. These devices exhibit current rectification and current output dependency on a back-gate voltage was observed. An on/off ratio of 108 was achieved in the best case, as well as current capacities as high as 841 μA for a source-drain bias in the range of -3 to +3 V. No correlation between electrode spacing and current rectification was observed.

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Figure 1: SEM micrograph of carbon nanotube network used to fabricate (a) devices 1 and 2 and (b) devices 3, 4, and 5, in which significantly lower density of nanotubes and large iron particles are found. Note that the in-lens configuration of the SEM is known to highlight nanotubes but their width is not well represented in the image.

Figure 2: Devices (a) 1 and 2, (b) 3 and 4, and (c) 5 are pictured. Al and Au electrodes are identified. The mat of nanotubes covers the entire pictured area and is below the deposited electrodes. Note the variation in spacing between the electrodes of the different devices.

Figure 3: Cross section of final device. The nanotube mat is not pictured but is a thin layer on top of the SiO_2 layer and beneath the Au and Al contacts. There are two modes for making electrical measurements using this structure. In the first mode, Au and Al electrodes (source-drain) are contacted and current is measured as the source-drain voltage is varied. In the second mode the underlying silicon is contacted and acts as a gate, setting up an electric field which depletes or injects current carriers into the nanotubes depending on its bias.

Figure 4: Electrical characterization of (a) devices 1 and 2; (b) devices 3, (c) device 4, and (d) device 5. On/off ratios of devices 1 and 2 were 20 and 5, and maximum current capacities 8 μA and 22 μA, respectively. On/off ratios of device 3 was 27 and maximum current capacity 679 μA. On/off ratios of 6 and 108, and maximum current capacities of 841 and 735 μA were obtained from two subsequent trials performed with device 4. Finally, on/off ratio of device 5 was difficult to determine because of the dramatic variations in the reverse bias region; the maximum current capacity is 794 μA.

Figure 5: Gate voltage dependence of diode device 1 (figure 1a).