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David J. Comer
comer.ee@byu.edu

Donald Comer

Aaron Shreeve

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Aaron M. Shreeve, David J. Comer and Donald T. Comer

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A. M. Shreeve is with AMI Semiconductor, American Fork, UT 84003 USA. (email: ashreeve@amis.com)

D. J. Comer and D. T. Comer are with the Department of Electrical and Computer Engineering, Brigham Young University, Provo, UT 84602 USA. (email: comer@ee.byu.edu)

Abstract

This paper investigates the linearity of submicron gate length CMOS devices and their behavior in open loop voltage to current (V-I) converters. Methods are developed to estimate the deviation from linearity in V-I converters due to short-channel effects. Using these methods, a converter is designed and fabricated on a 0.35 μ process. The measured deviation from linearity is less than 1% and the simulated bandwidth is 1 GHz.

1 Introduction

With the ability to perform at higher speeds and lower powers, current mode devices are becoming increasingly popular in analogue and mixed signal VLSI design. Current mode devices operate by sensing and controling currents rather than voltages. Voltage to current converters are used to interface between voltage mode and current mode circuits. It is generally required that the V-I con-

version be linear. With sufficient linearity and accuracy, V-I converters can be useful in analogue to digital converters (ADCs), digital to analogue converters (DACs), variable gain amplifiers (VGAs), multipliers, filters, modulators, mixers, and many other circuits that require high operating speeds (Surakampontorn *et al.* 1999, Seevinck and Wassenaar 1987).

Traditionally, MOS converters capitalized on the square-law variation of drain current with gate-to-source voltage to achieve linear conversion. Although excellent linearity can be achieved with converters that use square-law devices, modern short-channel devices, necessary for high-speed conversion, depart drastically from a second-order relationship between output current and input voltage. As channel length shrinks from 2 μ to 0.18 μ, the exponent relating drain current to effective gate voltage for n-channel devices decreases from 2 to approximately 1. An earlier paper (Sakurai and Newton 1990) shows an exponent of approximately 1 for nMOS and 1.2 for pMOS devices with 0.5 μ gate lengths. Although our work shows larger exponents for this channel length, the exponent is very close to unity for 0.18 μ devices of either type.

The departure from a square-law variation leads to nonlinearity in the voltage-current conversion. One purpose of this paper is to derive equations for the nonlinearities introduced by noninteger exponents and consider the limitations imposed on input signals to limit the nonlinearity to a fixed percentage. Whereas there are many definitions of linearity, we will use the parameter d_l, called the deviation from linearity. This parameter is defined in figure 1.

[Insert figure 1 about here]

As an input voltage is swept linearly over a given range, the output current will approximate a linear sweep. The ideal value at the end of the sweep is the value that would be reached if the slope of the current remained constant. The difference between this ideal value and the actual value is the error. The deviation from linearity is then defined as the error divided by the ideal value or

$$d_l = \frac{ideal\ current - actual\ current}{ideal\ current} = \frac{error}{ideal\ current} \tag{1}$$

It is to be noted that this definition of linearity results in larger errors than definitions such as best-fit straight line or end-point nonlinearity.

2 Drain Current vs. Gate-to-Source Voltage for Short-Channel Devices

The average electric field along the channel from source to drain is given by $\mathcal{E} = V_{DS}/L$ where L is the channel length and V_{DS} is the drain-to-source voltage. For larger channel lengths above about 2 μ, typical values of V_{DS} lead to relatively low electric field intensities. As $\mathcal{E}$ is increased, a proportional increase in carrier velocity occurs. As the channel lengths become smaller, the electric field intensity increases and the velocity does not show a proportional relationship with $\mathcal{E}$. For high values of $\mathcal{E}$, the velocity approaches a constant value referred to as the scattering-limited velocity (Gray *et al.* 2001).

For the low values of $\mathcal{E}$ present in longer channel devices, the drain current of an n-channel device for operation in strong inversion is given by

$$I_D = \frac{\mu C_{ox} W}{2L}\ [V_{GS} - V_t]^2 \tag{2}$$

if channel length modulation effects are ignored. In this equation, V_{GS} is the

gate-to-source voltage, μ is the carrier mobility, W is the width, and L is the length of the channel. The threshold voltage for this device is V_t.

For the higher values of $\mathcal{E}$ often present in short-channel devices, the drain current varies as (Gray *et al.* 2001)

$$I_D = \frac{\mu C_{ox} W}{2L(1 + \frac{V_{GS} - V_t}{\mathcal{E}_c L})} [V_{GS} - V_t]^2 \tag{3}$$

In this equation $\mathcal{E}_c$ is the critical electric field or the value that leads to a drift velocity that is one-half the velocity that would be reached with no limiting. For a typical n-channel device, this value is $\mathcal{E}_c = 1.5 \times 10^6$ V/m.

From (3) we can examine the extremes of long- and short- channel devices. The limiting case for long-channel devices, such that $\mathcal{E}_c L$ becomes much larger than $V_{GS} - V_t$, leads to the square-law variation of (2). Velocity limiting is not a factor in this situation. For the short-channel case, the value of L decreases so that $\mathcal{E}_c L$ is much smaller than $V_{GS} - V_t$. Equation (3) now reduces to

$$I_D = \frac{\mu C_{ox} W \mathcal{E}_c}{2} [V_{GS} - V_t] \tag{4}$$

This expression indicates a linear relationship between drain current and the effective voltage, $V_{eff} = V_{GS} - V_t$.

The difference in mobility between n- and p-channel devices leads to different exponents for these devices of equal sizes. For our p-channel devices, a channel length of 0.18 μ and a drain-to-source voltage of 1.6 V resulted in an exponent of 1.06 rather than unity. The exponent for the n-channel device approximated unity. A 0.35-μ channel length with a 2.2 V drain-to-source voltage resulted in an exponent of 1.5 for a p-channel device and 1.2 for an n-channel device.

While it is possible to derive the exponential variation between drain current and effective voltage, we will here cite the 1990 paper that demonstrates this

fact (Sakurai and Newton 1990).

3 Linearity Derivations

Voltage to current converters can be classified into two basic types; open loop converters, and closed loop converters. The closed loop converters are very accurate, but depend on highly accurate resistor values and are limited in speed of conversion. Most open loop linear V-I converters have been two quadrant circuits that use square-law devices with even power cancellation to achieve linearity (Seevinck and Wassenaar 1987, Vlassis and Siskos 1999, Vervoort and Wassenaar 1995).

3.1 A simple converter

The simple circuit of figure 2 indicates two identical p-channel devices with differential input voltages, V_1 and V_2. The sources of both devices are tied to the positive power supply voltage, V_{DD}, eliminating drain-to-source voltage changes.

[Insert figure 2 about here]

If the threshold voltages of the devices are assumed to be equal, the drain currents exiting the devices can be written as

$$I_{D1} = \frac{\mu C_{ox} W}{2L} \ [V_{DD} - V_1 - V_t]^n \tag{5}$$

and

$$I_{D2} = \frac{\mu C_{ox} W}{2L} \ [V_{DD} - V_2 - V_t]^n \tag{6}$$

The applied voltages are given by

$$V_1 = V_{dc} + v \tag{7}$$

and

$$V_2 = V_{dc} - v \tag{8}$$

Substituting these voltages into the drain current equations leads to a differential current of

$$I_{diff} = I_{D2} - I_{D1} = \frac{\mu C_{ox} W}{2L} \, (V_{DD} - V_{dc} - V_t)^n [(1+x)^n - (1-x)^n] \tag{9}$$

where

$$x = \frac{v}{V_{DD} - V_{dc} - V_t} \tag{10}$$

Using the binomial expansion for $(1+x)^n$ and $(1-x)^n$ results in a differential current of

$$I_{diff} = \frac{\mu C_{ox} W}{2L} \, (V_{DD} - V_{dc} - V_t)^n$$
$$\times 2nx \left[1 + \frac{(n-1)(n-2)x^2}{3} + \frac{(n-1)(n-2)(n-3)(n-4)x^4}{120} + \cdots \right] \tag{11}$$

For small values of x, the differential current varies linearly with x as

$$I_{diff} = \frac{\mu C_{ox} W}{2L} \, (V_{DD} - V_{dc} - V_t)^n \, 2nx \tag{12}$$

The corresponding equation in terms of input voltage, v, becomes

$$I_{diff} = \frac{\mu C_{ox} W}{2L} \, (V_{DD} - V_{dc} - V_t)^{n-1} \, 2nv \tag{13}$$

The overall transconductance of the circuit is found by differentiating I_{diff} with respect to v to get

$$G_m = \frac{\mu C_{ox} W}{2L} \, (V_{DD} - V_{dc} - V_t)^{n-1} \, 2n \tag{14}$$

As x increases, the deviation from linearity in I_{diff} is

$$d_l = \frac{(n-1)(n-2)x^2}{3} + \frac{(n-1)(n-2)(n-3)(n-4)x^4}{120} + \cdots \qquad (15)$$

Each error term in (15) becomes much smaller than the preceding term, thus the use of one or two terms is sufficient to calculate d_l, depending on the maximum value of x.

Note that the deviation from linearity goes to zero if $n = 1$ or $n = 2$. Ignoring channel-length modulation effects, the differential current is perfectly linear with x or v when the drain current varies as either the second or first power of V_{eff}. This explains why the older, long-channel devices exhibited good linearity of voltage to current conversion. It also implies that very short channel devices, for example, 0.18-μ devices will perform a conversion with little linearity error. This has been demonstrated in two recent US patent applications by Intel (Comer *et al.*a, b).

It can easily be shown that the maximum deviation from linearity occurs for devices with $n = 1.5$. Using only the first term in (15) to approximate the deviation from linearity gives

$$d_l = \frac{(0.5)(-0.5)x^2}{6} = -0.0417x^2 \qquad (16)$$

This equation allows a limit to be placed on the value of x to achieve a given deviation from linearity. Solving for the value of x gives

$$x = 4.90\sqrt{|d_l|} \qquad (17)$$

For example, if the desired value of d_l is 2% or 0.02, the maximum value of x is 0.683. From (10),

$$x = \frac{v}{V_{DD} - V_{dc} - V_t}$$

the input voltage swing v can be maximized by choosing V_{dc} to be as small as possible, assuming V_{DD} and V_t are fixed. If only positive gate voltages are allowed, then V_{dc} should equal v to maximize the allowable value of v. If $V_{DD} = 1.6$ V and $V_t = 0.55$ V, a deviation from linearity of 2% allows a maximum value for v of 0.43 V.

3.2 A practical converter

A more practical converter is shown in figure 3. In this converter, the output currents are directed to the inputs of current mirror stages that mirror these currents to the output lines.

[Insert figure 3 about here]

If all devices are assumed to have the same exponential variation of drain current with effective voltage, an analysis similar to that of the previous paragraphs gives a variation of differential output current with input voltage of

$$I_{diff} = \frac{n\mu C_{ox} W_3}{L_3 \left[1 + \left(\frac{W_3 L_1}{L_3 W_1}\right)^{1/n}\right]^n} (V_{DD} - V_{dc} - 2V_t)^n \, x \tag{18}$$

where

$$x = \frac{v}{V_{DD} - V_{dc} - 2V_t} \tag{19}$$

In terms of input voltage, v, this equation becomes

$$I_{diff} = \frac{n\mu C_{ox} W_3}{L_3 \left[1 + \left(\frac{W_3 L_1}{L_3 W_1}\right)^{1/n}\right]^n} (V_{DD} - V_{dc} - 2V_t)^{n-1} \, v \tag{20}$$

The overall transconductance is given by

$$G_m = \frac{n\mu C_{ox} W_3}{L_3 \left[1 + \left(\frac{W_3 L_1}{L_3 W_1}\right)^{1/n}\right]^n} (V_{DD} - V_{dc} - 2V_t)^{n-1} \tag{21}$$

The deviation from linearity in I_{diff} is found to be

$$d_l = \frac{n(n-1)(n-2)x^2}{3} + \frac{n(n-1)(n-2)(n-3)(n-4)x^4}{60} \tag{22}$$

Again it is seen that this error vanishes for $n = 1$ or $n = 2$. The deviation from linearity is maximum for $n = 1.58$.

For a specified maximum deviation from linearity when $n = 1.5$, the maximum values of x and input voltage,v, can be found from

$$x = 2.83\sqrt{|d_l|} \tag{23}$$

Once the maximum value of x is found, the maximum value of v can be calculated from (19). Values of $V_{DD} = 3.3$ V, $V_t = 0.55$ V and $V_{dc} = v$ lead to a maximum value of $v = 0.63$ V for a deviation from linearity of 2%.

These results do not account for the channel-length modulation effect that accompanies the drain-to-source voltage changes in this circuit, but later simulations show that this effect is relatively small compared to the nonlinearity from the noninteger value of exponent n.

It is possible to exchange operating speed for accuracy over a rather limited range. The linearity of the circuit improves if the current mirror devices have a longer channel length and a higher value of n. Although the derivation of this result is difficult, simulations show that changing n from 1.5 to 2 lowers the deviation from linearity by a factor of approximately 2. The longer channel lengths of the current mirror devices that lead to $n = 2$ also decrease the overall operating speed of the converter due to increased capacitances.

4 Design of a V-I Converter

The guidelines developed in the previous section can be applied to the design of an actual converter. A converter is to be constructed using the AMI Semiconductor 0.35-μ process. The deviation from linearity is to be 1% or less over a differential input swing of 1.0 V or $v = 0.5$ V using a power supply of 3.3 V. The 3-dB bandwidth of the converter must exceed 500 MHz.

The basic circuit configuration of figure 3 is chosen for this design. The maximum input swing that will satisfy the linearity specification is first checked with the aid of (23). Using nominal threshold voltages for this process of $V_t = 0.55$ V leads to a maximum value of $x = 0.283$ and a corresponding maximum input swing of $v = 0.485$ V. Nonlinearities due to channel-length modulation would further limit this maximum input voltage. Thus, it appears that the basic design will not satisfy the specifications.

The input volotage swing can be increased by using longer channel devices for the current mirror and by using an attenuator circuit on the input signal. The final circuit schematic is shown in figure 4 and the layout is shown in figure 5.

[Insert figure 4 about here]

[Insert figure 5 about here]

Devices M7, M8, M9, and M10 form the attenuator circuits that attenuate the input signals by a factor of approximately 4. While the use of attenuator circuits will increase the linear input voltage range, additional nonlinearities will

be introduced by these components. Fortunately, the highest component of non-linear distortion in the attenuators is second-order distortion that is cancelled by the differential arrangement of the converter.

After fabrication, the deviation from linearity was measured to be less than 1% for input voltages up to 0.55 V. For this value of input signal, the incremental input voltage reaching the converter is about $v = 0.14$ V and the dc voltage is $V_{dc} = 1$ V. From (22), this would predict a deviation from linearity of 0.2%. However, the additional distortion introduced by the attenuator and channel length modulation effects increase the actual measured value (1%) over the theoretical value. The overall transconductance of the converter was measured to be $G_m = 115\ \mu AV^{-1}$.

It is difficult to measure the frequency performance of the converter when driving other on-chip circuits. However, the frequency response of the converter was simulated using BSIM3v3 models for the MOS devices. The 3-dB bandwidth of the converter when driving a zero load impedance was found to be 1 GHz. The total harmonic distortion (THD) at this bandwidth was 0.21%.

The frequency response of the converter can be improved at the expense of overall transconductance. If the current mirror devices are decreased in width from 25 μ to 8 μ, the transconductance decreases from 115 μAV^{-1} to 49 μAV^{-1}. Equation (21) with $n = 1.5$ predicts this exact change even though the current mirror devices have a value of n that approaches 2. Accompanying this change in width is an increase in bandwidth to 5 GHz. This is due to the decrease in current mirror capacitance. This decrease occurs as a result of two factors. The obvious factor is the decreased channel width and lowered drain-to-substrate capacitance. A less obvious factor is the increased voltage drop across the current

mirror devices with a narrower channel. The drain-to-substrate capacitance decreases as the drain-to-substrate voltage increases. The overall decrease in capacitance increases the bandwidth by a factor of 5.

Of course, the speed of conversion increases as the channel lengths become smaller. Newer converters using 0.18 μ or 0.1 μ will exceed the speed of this converter with a minimum gate length of 0.35 μ. In order to demonstrate this speed increase, the converter of this work is compared to two older converters (Vervoort and Wassenaar 1995, Maloberti and Rivoir 1996).

Table 1 shows a comparison between the published simulations of these two V-I converters and the converter discussed in this paper. It can be noted that the converter described in this paper has a markedly higher bandwidth than either of the other two comparators. The speed advantage would become even more marked if the current mirrors used the smaller channel widths.

[Insert table 1 about here]

5 Conclusions

MOS devices with gate lengths smaller than 2 μ depart from the second order variation of drain current with effective gate-to-source voltage. The exponent decreases as gate length decreases due to velocity limiting of carriers in the channel. The exponent varies from 2 toward 1 as the gate length reaches 0.18 μ. When the exponent is either 2 or 1, the differential current output of a converter can be approximately linear with input voltage. For noninteger exponents, more nonlinearity is introduced into the conversion. This paper demonstrates how to

approximate the deviation from linearity for circuits using noninteger exponents and how to design simple converters with a specified deviation from linearity. A converter fabricated on a 0.35 μ process is reported. The deviation from linearity of this device is less than 1% and the conversion rate can exceed 1 GHz.

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Figure Captions

Figure 1 Deviation from linearity.

Figure 2 A simple V-I converter.

Figure 3 Basic V-I converter schematic.

Figure 4 V-I converter with attenuators added.

Figure 5 Converter layout.

Table caption

Table 1. Converter comparisons

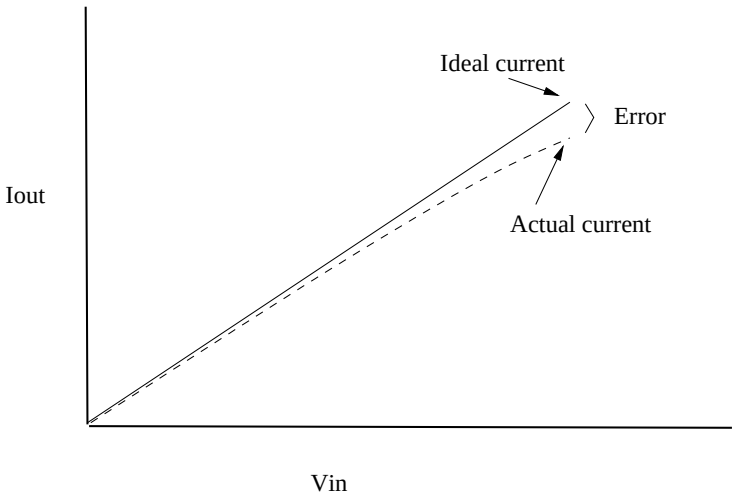

Figure 1: Deviation from linearity.

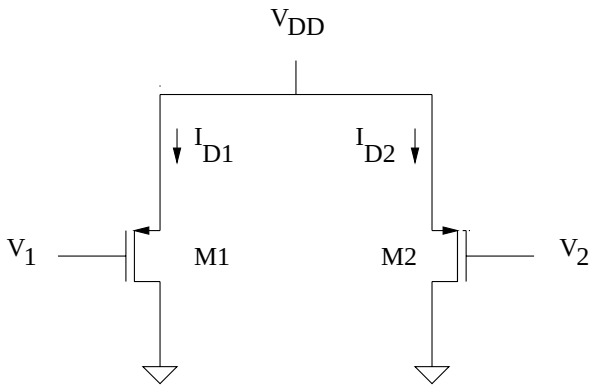

Figure 2: A simple V-I converter

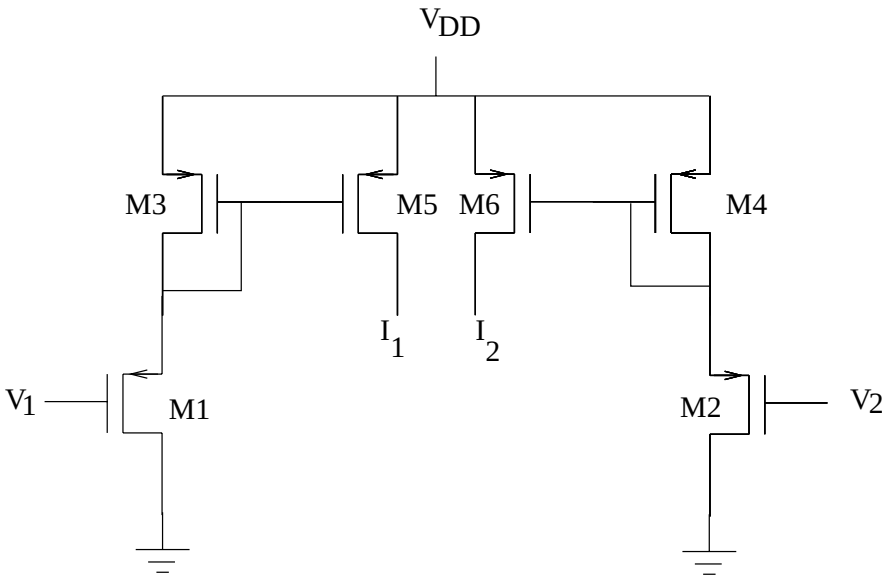

Figure 3: Basic V-I converter schematic

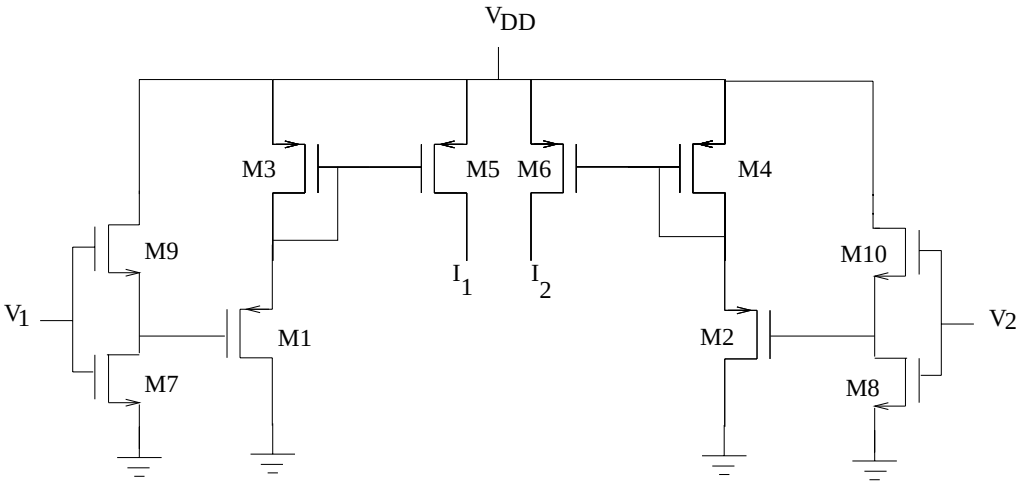

Figure 4: V-I converter with attenuators added.

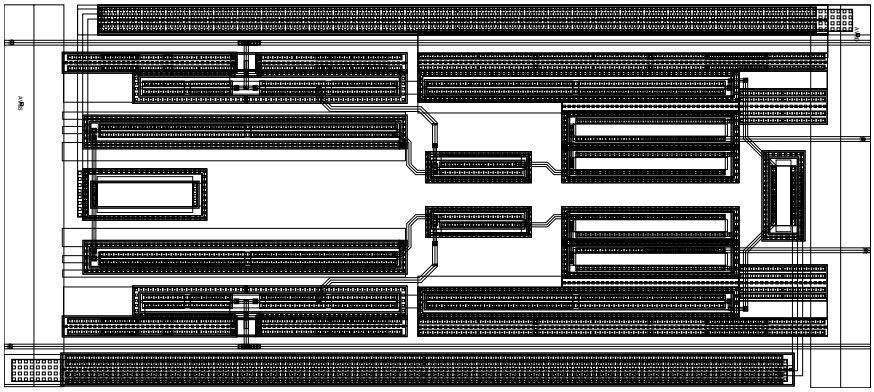

Figure 5: Converter layout

Table 1: CONVERTER COMPARISONS

Parameter	Vervoort	Shreeve	Maloberti	Units
DC Transconductance	116	115	512	μA/V
Bandwidth	4.8	1000	54	MHz
THD at V_{in} =400mV	0.14	0.07	0.1	%
VDD	2.2	3.3	5	Volts
CMIR	O-VDD	1.8	0.5	Volts
Supply Current	0.3-0.4	2.0-2.5	2.5-2.9	mA