2007-05-31

Band discontinuity measurements of the wafer bonded InGaAs/Si heterojunction

Aaron R. Hawkins
hawkins@ee.byu.edu

Kyle S. McKay

Felix P. Lu

Jungsang Kim

Changhyun Yi

See next page for additional authors

Original Publication Citation

Mckay, Kyle S., Felix P. Lu, Jungsang Kim, Changhyun Yi, April S. Brown, and Aaron R. Hawkins. "Band discontinuity measurements of the wafer bonded InGaAs/Si heterojunction." Applied Physics Letters 9 (27)

Band discontinuity measurements of the wafer bonded InGaAs/Si heterojunction

Kyle S. McKay,[a] Felix P. Lu, Jungsang Kim, Changhyun Yi, and April S. Brown
Fitzpatrick Institute for Photonics, Electrical and Computer Engineering Department, Duke University, Durham, North Carolina 27708

Aaron R. Hawkins
Electrical and Computer Engineering Department, Brigham Young University, 459 Clyde Building, Provo, Utah 84602

(Received 24 January 2007; accepted 9 May 2007; published online 31 May 2007)

p-type InGaAs/Si heterojunctions were fabricated through a wafer fusion bonding process. The relative band alignment between the two materials at the heterointerface was determined using current-voltage (*I-V*) measurements and applying thermionic emission-diffusion theory. The valence and conduction band discontinuities for the InGaAs/Si interface were determined to be 0.48 and −0.1 eV, respectively, indicating a type-II band alignment. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2745254]

$In_{0.53}Ga_{0.47}As$ (InGaAs) lattice matched to InP has a direct band gap of ~0.74 eV at room temperature, corresponding to a photon wavelength of 1.68 μm.[1] It is an ideal semiconductor material for realizing photodetectors in the near infrared wavelength range relevant for optical fiber communications at 1.31 and 1.55 μm. Si, which has excellent carrier multiplication properties, has been integrated with InGaAs to create high performance photodiodes at these wavelengths.[2–6] Due to the large mismatch in the lattice constants (~7.7%) and coefficients of thermal expansion (CTE) of InGaAs and Si, low defect epitaxial growth of InGaAs on Si is very difficult. The wafer fusion process allows materials with different lattice constants and CTE to be permanently joined with a relatively low defect density and low oxide content at the heterointerface. This process was employed to fabricate the photodiodes cited above, as well as other solid state devices.[7] The band discontinuities are critical for understanding the carrier transport properties of the heterointerface and are essential to the optimal design of these and future devices. The measured valence band discontinuity of the wafer fused InGaAs/Si interface is reported in this letter.

p-type heterojunctions were fabricated to investigate the hole transport properties across the InGaAs/Si interface. We used boron doped, mirror polished, *p*-type (100) Si wafers with a resistivity of ~4.5 Ω cm (3×10^{15} cm^{-3}). The InGaAs structures were grown using solid source molecular beam epitaxy on a semi-insulating (100) InP substrate with a highly doped 1000 Å InGaAs contact layer ($>10^{19}$ cm^{-3}), a 5000 Å moderately doped InGaAs active layer (5×10^{16} cm^{-3}), and a 1000 Å InAlAs cap layer. The InAlAs cap layer is a sacrificial protective layer that is removed before bonding.

Si wafers were cleaved into 8×8 mm^2 pieces and cleaned using the standard RCA process (NH_4OH:H_2O_2:H_2O 1:1:5, RCA1; and HCl:H_2O_2:H_2O 1:1:5, RCA2) to remove any organic and metallic contaminations from the wafer surface.[8] The InGaAs wafers were cleaved into 7×7 mm^2 pieces, and then a hydrochloric acid solution (HCl:H_2O 3:1) was used to remove the InAlAs cap layer. The InGaAs pieces were patterned with a 300×300 μm^2 square grid with 10 μm channels etched using an InGaAs selective etch (H_3PO_4:H_2O_2:H_2O 1:1:11). The channels were etched to allow any trapped gases that may form during the high temperature annealing to escape from the interface.[7] The Si and InGaAs wafer pieces were then cleaned in acetone and isopropanol until a microscope inspection revealed a clean surface free from particulate contaminants. The wafers were then transferred to a nitrogen glovebox for bonding.

In the nitrogen ambient, both wafer pieces were dipped into a 5% hydrofluoric acid (HF) solution to remove any surface oxides. The InGaAs piece was then pressed onto the Si, visually aligned to match crystallographic orientation, and then pressure was applied while the sample was dried with a nitrogen gun. The nitrogen glovebox, where the Si and InGaAs were bonded together, had an oxygen concentration of <1 ppm and a moisture content of <10 ppm. The HF dip and the low oxygen concentration ensured that minimal oxides were present at the interface. After contact, the bonded pair was loaded into a graphite fixture and transported in nitrogen to the annealing furnace, where it encountered room air for about 1 min before the furnace was pumped down and backfilled with nitrogen or hydrogen. The bonded sample was then subjected to a two-stage annealing.[6] The first stage started with a slow ramp (2 °C/min) up to 300 °C, and the sample was then annealed for 1 h to allow any gas at the interface to escape through the channels etched into the InGaAs. The second stage consisted of a faster ramp (6 °C/min) up to 650 °C and held for 1 h during which covalent bonds were formed between Si and InGaAs. After the annealing, the InP substrate was removed from the bonded sample in a HCl solution (HCl:H_2O 3:1). Through this process, the InGaAs layers were bonded and transferred to the Si surface for device processing.

The valence band discontinuity of the heterojunction was characterized by measuring *I-V* characteristics and applying thermionic emission-diffusion theory[9,10] to calculate the barrier height.[11,12] Devices of different shapes and sizes were fabricated to measure the impact of surface and edge effects on the *I-V* measurements. Ohmic contacts (70 Å

[a]Electronic mail: ksm18@duke.edu

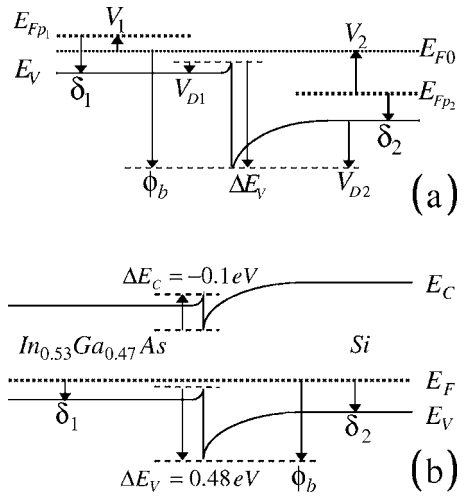

FIG. 1. (a) Definitions of selected terms for the valence band referred to in this letter. E_V is the valence band, E_{F0} is the equilibrium Fermi level, E_{FP1} and E_{FP2} are the quasi-Fermi levels, δ_1 and δ_2 are the energy differences between the Fermi level and valence band, V_1 and V_2 are the fractions of the applied voltage supported in each semiconductor, V_{D1} and V_{D2} are the diffusion potentials, ΔE_V is the valence band discontinuity, and ϕ_b is the barrier height. (b) Band alignment of the *p*-type InGaAs/Si heterojunction. The valence band discontinuity is determined to be 0.48 eV, while the conduction band discontinuity is −0.1 eV. E_C and E_V are the conduction and valence bands, E_F is the Fermi level, and ΔE_C and ΔE_V are the conduction and valence band discontinuities.

Cr/3000 Å Au) in square and circle shapes with characteristic sizes ranging from 100 to 250 μm were evaporated onto the transferred InGaAs. The Cr/Au contacts were used as self-aligned masks for subsequent wet etching of the InGaAs layers that defined the size of the devices. Aluminum was evaporated on the back side of the Si to provide a substrate ohmic contact. *I-V* measurements were taken over a range of temperatures using a semiconductor parameter analyzer (Keithley 4200).

Current transport across a barrier can be described by thermionic emission-diffusion theory for the moderate temperatures and bias values of our heterojunction. In semiconductor materials with low doping levels or low mobility, the carrier transport properties in the space charge regions dominate, and the current density J reduces to

$$J \cong qN_C\mu E \exp\left(\frac{-q\phi_b}{k_BT}\right)\left[\exp\left(\frac{qV_1}{nk_BT}\right) - \exp\left(\frac{-qV_2}{nk_BT}\right)\right], \tag{1}$$

where q is the electronic charge, N_C is the majority carrier concentration, μ is the hole mobility, E is the electric field near the interface, ϕ_b is the barrier height, n is the ideality factor, k_B is Boltzmann constant, T is the temperature, and V_1 and V_2 are the fractions of voltage supported in each material in the junction where the applied voltage $V=V_1+V_2$ [Fig. 1(a)].[9]

The current density as a function of applied voltage is shown in Fig. 2 where the InGaAs is biased with respect to grounded Si. The curve has three regions of interest. The first region extends from −2 to −0.3 V and is a region where series resistance effects dominate. The second region is the region from −0.3 to 0 V where the current density is exponentially dependent on the applied voltage [second term in Eq. (1)]. The third is the positively biased region where the dependence on the applied voltage is weak [first term in Eq. (1)]. The strong exponential voltage dependence for hole injection from Si to InGaAs as compared to the weak voltage dependence for hole injection from InGaAs to Si is a result of the difference in the V_1 and V_2 terms in Eq. (1). The relationship between V_1 and V_2 is determined from the continuity of electric displacement at the interface,[9] and in this heterojunction V_2 is $\sim 20V_1$.

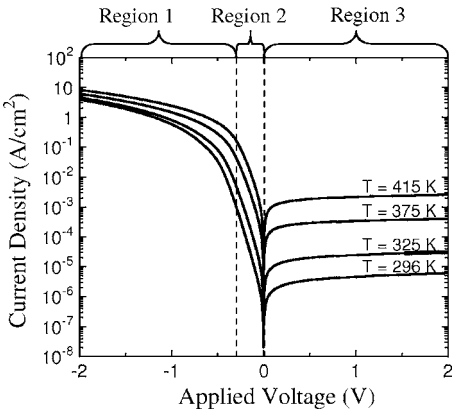

FIG. 2. *J-V* Plot for a *p*-type sample bonded and annealed in a N_2 environment. In region 1 (−2 to −0.3 V), the current density is limited by series resistance effects. In region 2 (−0.3 to 0 V), the current density has an exponential relation to the applied voltage. In region 3 (0–2 V), the current density has a weak dependence on the applied voltage.

In order to find the barrier height, the current density in region 2 was fitted to the second term in Eq. (1), ignoring the first term in the limit of positive bias. The barrier height was then extracted from the temperature dependence.[11] The barrier height was determined to be 0.59 with a standard deviation of 0.04 eV, as shown in Fig. 3. The reduced scatter in the data points at larger device area suggests that edge and surface effects are responsible for some of the variations in the barrier height.

The valence band discontinuity ΔE_V can be deduced from the measurement of the barrier height using the relationship

$$\Delta E_V = qV_D - \delta_1 + \delta_2, \tag{2}$$

where V_D is the diffusion potential ($V_D=V_{D1}+V_{D2}$) and δ_1 and δ_2 are the distances from the valence band edge to the Fermi level for InGaAs and Si, respectively [Fig. 1(a)].[12] The diffusion potentials are determined from the calculated barrier heights and from boundary conditions imposed by the continuity of the electric displacement field.[9] The valence

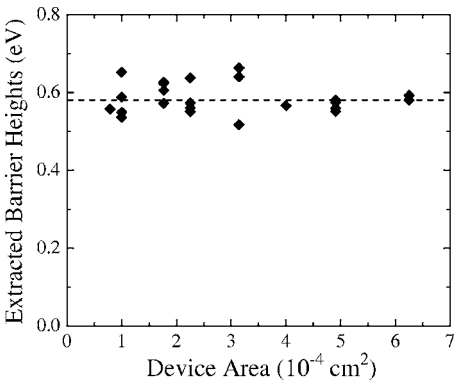

FIG. 3. Extracted barrier heights for measured devices. The dashed line indicates the average barrier height of 0.59 eV.

band discontinuity ΔE_V is determined to be $0.48 \pm .04$ eV at room temperature. The corresponding conduction band discontinuity is determined using the differences in the band gaps of the two materials to be −0.1 eV, indicating type-II alignment for the heterojunction [Fig. 1(b)].

Due to the lattice mismatch between InGaAs and Si, a large number of dangling bonds are expected at the heterointerface. In the bonding process adopted in our approach, most of these are passivated by hydrogen due to the HF treatment prior to bonding. Previous work has shown that a nearly ideal interface, free from significant charge trapping, can be fabricated between InGaAs and Si even in the presence of these defects.[13] While the presence of trapped charge at the interface will affect the current density measurements by increasing the ideality factor in Eq. (1), this does not significantly affect the measurement of the valence band discontinuity. It is known that the presence of hydrogen at the interface can lead to significant changes in the relative band alignment of the Si/SiO_2 heterojunction, and similar impact might be present in our bonded interface.[14] More work will have to be done to determine the effects of interfacial hydrogen on the band discontinuities.

In summary, we fabricated wafer bonded *p*-type InGaAs/Si heterojunctions to measure the hole transport properties of the interface. Thermionic emission-diffusion theory was used to extract barrier height information from *I-V* measurements. A valence band discontinuity of 0.48 eV and a conduction band discontinuity of −0.1 eV indicated a type-II alignment for the wafer bonded heterojunction fabricated by the above process. InGaAs/Si heterojunctions will play an important role in optoelectronic applications, especially photodetectors operating in the near infrared wavelengths.

[1] Pallab Bhattacharya, *Semiconductor Optoelectronic Devices*, 2nd ed. (Prentice Hall, Upper Saddle River, 1997) p. 549.
[2] F. E. Ejeckam, C. L. Chua, Z. H. Zhu, Y. H. Lo, M. Hong, and R. Bhat, Appl. Phys. Lett. **67**, 3936 (1995).
[3] A. R. Hawkins, T. E. Reynolds, D. R. England, D. I. Babic, M. J. Mondry, K. Streubel, and J. E. Bowers, Appl. Phys. Lett. **68**, 3692 (1996).
[4] Y. Kang, P. Mages, A. R. Clawson, S. S. Lau, Y. H. Lo, P. K. L. Yu, A. Pauchard, Z. Zhu, and Y. Zhou, Appl. Phys. Lett. **79**, 970 (2001).
[5] B. F. Levine, C. J. Pinzone, S. Hui, C. A. King, R. E. Leibenguth, D. R. Zolnowski, D. V. Lang, H. W. Krautter, and M. Geva, Appl. Phys. Lett. **75**, 2141 (1999).
[6] P. Mages, Ph.D. thesis, University of California, San Diego, 2003.
[7] A. Black, A. R. Hawkins, N. M. Margalit, D. I. Babic, A. L. Holmes, Y. L. Chang, P. Abraham, J. E. Bowers, and E. L. Hu, IEEE J. Quantum Electron. **3**, 943 (1997).
[8] Q.-Y. Tong and U. Gosele, *Seminconductor Wafer Bonding* (Wiley, New York, 1999) Chap. 4 pp. 49–54.
[9] S. M. Sze, *Physics of Semiconductor Devices* 2nd ed. (Wiley, New York, 1981) Chap. 2 and 5.
[10] R. J. Schuelke and M. S. Lundstrom, Solid-State Electron. **27**, 1111 (1984).
[11] H. Wada, Y. Ogawa, and T. Kamijoh, Appl. Phys. Lett. **62**, 738 (1993).
[12] Y. C. Zhou, Z. H. Zhu, D. Crouse, and Y. H. Lo, Appl. Phys. Lett. **73**, 2337 (1998).
[13] B. F. Levine, A. R. Hawkins, S. Hiu, B. J. Tseng, C. A. King, L. A. Gruezke, R. W. Johnson, D. R. Zolnowski, and J. E. Bowers, Appl. Phys. Lett. **70**, 2449 (1997).
[14] P. Perfetti, C. Quaresima, C. Coluzza, C. Fortunato, and G. Margaritondo, Phys. Rev. Lett. **57**, 2065 (1986).