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Low-Photoluminescence Hollow Waveguide Platforms for

High-Sensitivity Integrated Optical Sensors

Yue Zhao

A dissertation submitted to the faculty of
Brigham Young University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

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ABSTRACT

Low-Photoluminescence Hollow Waveguide Platforms for
High-sensitivity Integrated Optical Sensors

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Doctor of Philosophy

This dissertation presents research on the fabrication of optofluidic sensor platforms, which consist of integrated hollow waveguides and solid waveguides. Antiresonant reflecting optical waveguides (ARROWs) filled with liquids or gases, can be used for high-sensitivity sensing in applications of biotechnology, chemical synthesis, and analytical chemistry. The fabrication method developed for integrated ARROW sensing platforms utilizes standard microfabrication processes and materials. Dielectric cladding layers are deposited on a silicon wafer using plasma-enhanced chemical vapor deposition (PECVD) or sputtering. A sacrificial material is then patterned over the bottom cladding layers by photolithography. Additional dielectric layers are deposited around the core, forming the structure of the waveguides. Integrated solid-core waveguides can be easily created by etching a ridge into the topmost dielectric cladding layer. The hollow core waveguides are then formed by wet etching the sacrificial core material.

The coupling efficiency between solid core and hollow core waveguides is extremely important for the platform's overall sensitivity. Efficiencies can be enhanced from 18% to 67% by adjusting the thickness of the thick top oxide. Experimental results prove that optical throughput was improved by 17.1× with this improved interface transmission. Sputtered films were investigated as an alternative to for producing cladding layers. The experimental results reveal that sputtered layers show poor adhesion and mechanical strength which make them unreliable for hollow waveguides with small dimension. High-sensitivity ARROW platforms were obtained by employing hybrid layers (PECVD SiO_2 and sputtered Ta_2O_5) as claddings and building waveguides on self-aligned pedestals. The photolumiscence background was only 1/10 that of previous devices made with SiO_2/SiN and the average signal-to-noise ratio was improved by 12×.

Keywords: hollow waveguides, sputter, photolumiscence, PECVD, plasma etching, signal-to-noise ratio

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1 INTRODUCTION

1.1 Integrated Optofluidic Devices

Optofluidics refers to an emergent research field that combines microfluidics and integrated optical systems. Miniaturization and configurability are two major advantages associated with optofluidics. The implementation of optics in the microfluidic platform enables an unprecedented level of integration. Moreover, optofluidic devices are easily and highly reconfigurable, which can be a significant advantage for manipulating and handling biological samples. The use of fluid as a medium for transport is appropriate for a significant class of clinically important biological entities [1], ranging from DNA strands, viruses, and bacteria to cells and microorganisms.

Optofluidic can be categorized according to three broad categories of interactions: fluid–solid interfaces, purely fluidic interfaces (L^2), and colloidal suspensions [2]. For the first type, interfaces between solid and liquid materials can be used to synthesize optofluidic devices. This can be done by fabricating a solid structure with voids whose dimensions are larger than the wavelength of light. The reflection and transmission of light through the void is then modified by the insertion of liquids in the voids. Examples can be found in the microfluidic refractometer [3], fiber Bragg grating refractive-index sensors [4], adaptive lenses [5], optofluidic microscopes [6], etc. L^2 waveguides, which belong to the second type - L^2 interfaces, are perfect examples of configurability as in this case control over the fluidic properties allows modification of the optical performance. This dynamic tuning ability is the biggest strength of the L^2 waveguide

approach. Several interesting optofluidic devices, including an optical switch [7], a fluorescent light source [8], optical splitters [9], and wavelength filters [9], have been demonstrated. The third category of optofluidic devices deals with the introduction of solid particles in a fluid. Such colloidal optofluidic systems can enable large changes in the optical properties of the resulting medium. Recently developed crescent-shaped nanoparticles have enhanced Raman scattering cross-sections and other optically interesting properties. In addition, there are several methods for optically manipulating the particles, for example optical tweezing.

Optofluidic devices have quickly found a broad range of applications, such as biotechnology, chemical synthesis, and analytical chemistry, which have been described in a few published recently articles and books [2, 10-12]. One of the major research focuses in optofluidic fluorescence detection is to improve the confinement and guiding of light in low index buffer solution (composed mainly of water) where analytes reside, which enhances the light-fluorophore interaction and fluorescence collection efficiency for a better detection limit. The research group I worked in at BYU has developed a fully planar integrated optofluidic platform [13-33] that permits single particle detection, manipulation and analysis on a chip. Liquid-core optical waveguides guide both light and fluids in the same volume. They are integrated with fluidic reservoirs and solid-core optical waveguides to define sub-picoliter excitation volumes and collect the optical signal, resulting in fully planar beam geometries. The small dimensions and fluid volumes of optofluidic waveguides make them ideal for fluorescence-based single molecule detection [34].

1.2 Contributions

The research presented in this dissertation has been aided the collaboration between the Microengineering Research Group led by Dr. Aaron Hawkins at BYU and the Applied Optics

group led by Dr. Holger Schmidt at the University of California Santa Cruz (UCSC). All device fabrication describe here was conducted exclusively in the Integrated Microfabrication Laboratory (IML) at BYU. A portion of the optical design and testing of finished devices was conducted at UCSC.

This dissertation focuses mainly on the fabrication processes for integrated ARROW sensing platforms. My specific contributions to the overall development of this class of devices include: (1) Investigating hollow channels made with low-cost and low temperature sputtered layers meant to replace PECVD films; (2) Introducing sputtered Ta_2O_5 as a replacement for SiN films, resulting in reduced background noise and improved SNR for ARROW chips, these high-sensitivity platforms were applied as ultra-sensitive nucleic acid biosensor (3) Applying a novel method to characterize the optical transmission of ARROW chips and waveguide interfaces (4) Integrating on-chip filters with low temperature films deposited by sputtering. To date, portions of my research results have been published in four peer-reviewed journal articles (with another in review) and included in five conference presentations (see Appendix A). Although my research work already makes an important contribution to the general body of knowledge, hollow ARROW waveguide-based sensors still have potential for further improvements and many additional applications.

1.3 Organization

This dissertation describes the fabrication of liquid core ARROW waveguides and the platforms for high-sensitivity optical sensing. Chapter 2 discusses the characteristics of several different types of hollow waveguides, presenting theories and fabrication methods. The ARROW waveguide is emphasized and analyzed. ARROW-based sensing platform is also introduced in Chapter 2. Chapter 3 gives an overview of the fabrication processes of planar ARROW

waveguides, including detailed descriptions of the individual processes involved and their optimization for ARROW device fabrication. The properties of materials for ARROWs are also described in this chapter. Chapter 4 discusses the sources contributing to the optical loss of the ARROW chip from edge to edge. A method is proposed and applied to improve the optical throughput by enhancing the solid-to-liquid interface coupling efficiency. Chapter 4 also introduces a novel method to characterize the performance of the hollow core ARROW waveguides. ARROW waveguides made with sputtered films are described and evaluated in Chapter 5. In Chapter 6, the details of hollow ARROW waveguide with optimized structure and ideal material system are described, including fabrication processes, optical characterization, and experimental fluorescence testing results for sensor platform. Chapter 6 also discusses an annealing method which can further suppress the PL noise background and improve the signal-to-noise ratio of the ARROW chip. Chapter 7 summarizes my contributions to the ARROW project and describes the direction of future efforts for ARROW platform improvement. Following the body of the dissertation, several appendices are included. Appendix A lists my publications and conference presentations that have documented a portion of my work. Appendix B contains detailed descriptions of each process employed in ARROW fabrication. Appendix C contains the specific ARROW layer designs used in this work.

2 LIQUID CORE WAVEGUIDES

This chapter describes the theory of various liquid core waveguides. First, an overview of index guided waveguides is given, including the descriptions of Teflon AF waveguides [35-38], nanoporous waveguides [39-44], and slot waveguides [45-47]. Alternative methods of waveguiding based on interference are also discussed in this chapter. There are several types of interference-based liquid core waveguides, such as one-dimensional (1D) Bragg waveguides [48-52] and two-dimensional photonic crystal (2D-PC) waveguides [53-56]. The ARROW waveguide which also works on the interference principle is emphasized and investigated here. The detailed theory, basic fabrication process and sensing platform for ARROW waveguides are described and discussed.

2.1 Index Guiding Waveguides

Figure 2-1 shows how conventional optical waveguides work based on the total internal reflection (TIR) principle. The waveguides confine the light in a high-refractive index core (n_1) surrounded by a lower index cladding material (n_2). When light propagates along the z direction, rays are incident on the core-cladding interface at an angle θ_1. The light is partially reflected and partially transmitted. The refractive light has an angle of θ_2. Snell's law (Equation (2-1)) is used to determine the direction of reflected rays and transmitted rays, when θ_1 is above than the critical angle θ_c (Equation (2-2)), total internal reflection takes place. Under TIR conditions, the

light cannot propagate in the claddings and all the energy will be confined within the waveguide core.

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 . \qquad (2\text{-}1)$$

$$\theta_1 \geq \theta_c = \sin^{-1}(\frac{n_2}{n_1}) . \qquad (2\text{-}2)$$

Consequently, TIR-based waveguides require that the cladding materials have lower indices than the core materials. This is easy for solid core waveguides. However, it is a big challenge for optofluidic waveguides that utilize fluid cores because there are only very limited materials have a reflective index lower than water (n=1.33). Several low-index claddings for optofluidic waveguides are discussed in the following sections.

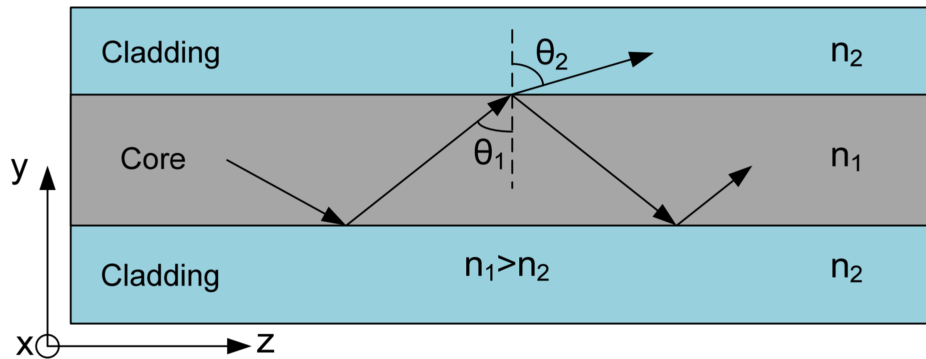


Figure 2-1: Index waveguiding with total internal reflection

2.1.1 Teflon AF Waveguides

In the 1990s, DuPont introduced a line of Teflon AF (copolymers of 2, 2-bistrifluoromenthyl-4, 5-difluoro-1, 3-dioxole and tetrafluoroethylene) resins with available index of refractions of 1.31 (Teflon AF 1600) and 1.29 (Teflon AF 2400) [57]. Both two types of Teflon AF have indices below 1.33 and they have been used for liquid core waveguides (LCW).

Rectangular waveguides with a dimension of 400μm×60μm were coated with Teflon AF for microanalysis systems in 2003 [37] and 200μm×70μm waveguides were reported in 2009 [38]. However, relatively large fluctuations of coating thicknesses make Teflon AF unsuitable for LCW with small dimensions, especially for submicron waveguides. Another challenge when using Teflon® AF is that it has poor adhesion to commonly-used substrates (silicon, glass, etc.), requiring that additional adhesion-promoting steps [36, 37] be added in fabrication, which further increases the difficulty of integration with waveguides.

2.1.2 Nanoporous Waveguides

Nanoporous dielectrics provide another way to make TIR-based LCWs (Figure 2-2). Compared with Teflon AF, nanoporous dielectrics adhere well to common substrates without additional surface treatment. By introducing air bubbles to the high-index materials (for example, silicon [39, 40, 42]), the porosity of claddings can be changed and then the refractive index can be tuned in the range of 1.15~1.37 [43]. Nanoporous films have been used as cladding layers for liquid-core slab [43] and 2D waveguides [44] with low propagation losses. If a way to create a lateral nanoporous cladding for complete mode confinement can be developed, this can be a very promising technology due to the existence of low-loss modes and the wide tuning range of the cladding refractive index.

2.1.3 Slot Waveguides

A slot-waveguide guides light in a subwavelength-scale low refractive index region by total internal reflection. As shown in Figure 2-3, a slot-waveguide is formed by embedding a low-index (n_c) subwavelength-scale slot in two high-index strips or slabs (n_w) and then surrounding by low-refractive-index (n_h) cladding materials. If x-polarized light is applied, the

major component of the electric field of the quasi-TE mode E_x is perpendicular to the walls of the slot, thereby producing a strong discontinuity at the interfaces, with much higher amplitude in the low-index slot. The ratio between the values of E_x at slots and slabs is equal to n_w^2/n_c^2. When the dimensions of the slot are smaller than the penetration depth (δ) of the evanescent wave from the interface into the low-index slot, the electric field remains high within the slot. Planar slot-waveguides have been demonstrated in several different material systems. A slot 150 nm wide and 250 nm thick was reported using Si/SiO_2 [45, 46]. Due to the high index contrast between Si and SiO_2, strong optical confinement and high integration can be achieved. However, for the same reason, a Si/SiO_2 slot-waveguide is more sensitive to interface roughness between the high-index-contrast materials, and the slot region must be on the order of 100 nm or less at telecomm wavelengths, which makes fabrication challenging. Si_3N_4 has lower refractive index than Si but still higher than that of SiO_2, allowing the implementation of photonic devices less sensitive to surface roughness and higher tolerance to dimensions deviations during fabrication while keeping a reasonable level of integration (small size). Si_3N_4/SiO_2 can be used to make a slot waveguide with a wider slot region (~200nm for 1260-1370nm laser source) due to a weaker optical confinement compared to Si/SiO_2 [47]. The small dimensions for interaction area and tight confinement make slot waveguides a very promising candidate for optofluidic measurements.

2.2 Interference Based Waveguides

Interference-based waveguides are another way to realize optofluidic waveguides. In this case, light is guided in the low-index liquid core surrounded by high-index cladding layers. As a result, light propagates in the interface based waveguides with a leaky mode. The cladding consists of film stacks which were designed to create multiple reflections of the electric field of

the light that can interfere destructively or constructively. Each film layer partially reflects a portion of light. Near-perfect reflection into the low-index core can be achieved if a large number of periodical cladding layers are employed.

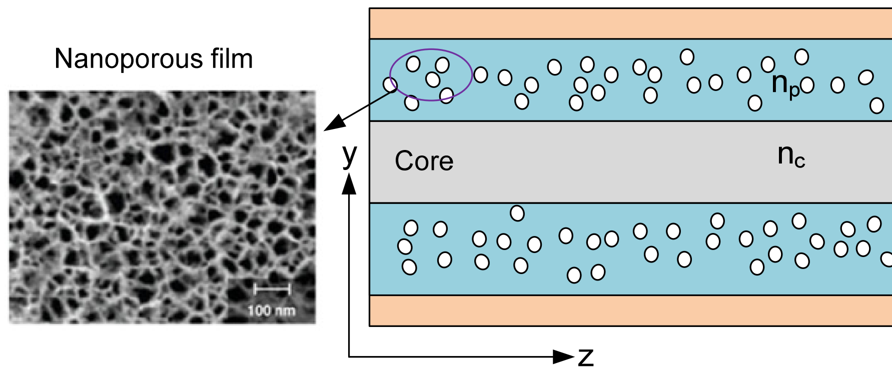


Figure 2-2: Diagram of nanoporous waveguides

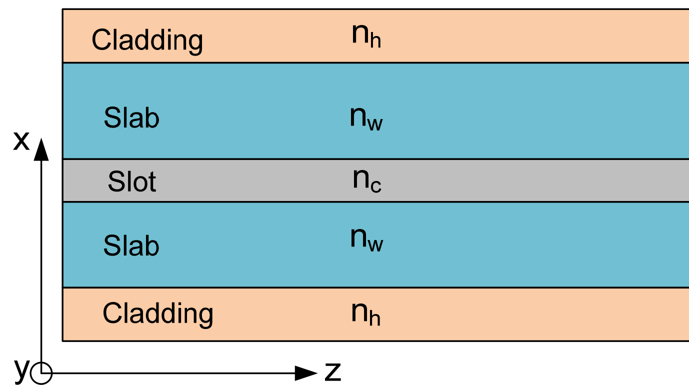


Figure 2-3: Diagram of slot waveguides

2.2.1 Bragg Fibers and Bragg Slab Waveguides

The theory of Bragg reflection waveguides and Bragg fibers was first proposed by Yeh and Yariv in 1976 [48] and analyzed in 1978 [49]. For interface-based waveguides, if the

cladding layers are repeated periodically and extend to infinity, the partial reflections are then equivalent to Bragg reflections. A Bragg lattice can also be referred to as a 1D photonic crystal (PC). Photonic crystals are wavelength scale, periodic, dielectric microstructures. Their periodic patterning creates photonic band gaps which forbid the propagation of light of a specific wavelength range through the structure.

Bragg waveguides are demonstrated in Figure 2-4(a) in which Bragg reflection relies on a structure which usually consists of an alternating sequence of layers of two different optical materials. Each layer reflects a portion of an optical wave. The thickness of each layer is carefully designed for a certain wavelength and so the film stacks act as a high-quality reflector for a band of wavelengths. To make low loss hollow core waveguides, the Bragg layers need to have large periodicity. For example, 19 pairs of GaAs (n=3.4)/AlAs (n=2.9) have been used to fabricate Bragg reflectors for air core waveguides at 1558nm [51]. The need for large numbers of layers, makes Bragg reflector microfabrication challenging.

The Bragg waveguide idea can also be applied to cylindrical cross sections, such as a Bragg fiber. Figure 2-4(b) illustrates how periodic layers surround a circular low index core resulting in an index profile that depends on the radial distance from the core center. The first experimental demonstrations of light guiding in an air-core Bragg fiber were given in 1999 [52]. Liquid core Bragg fibers have not been reported yet and their translation to a planar substrate is hard to imagine.

2.2.2 2D HC-PCF and PC Waveguides

2D Photonic-crystal fiber (PCF) and PC waveguides work base on the properties of photonic crystals. In a 2D crystal composed of parallel high-refractive index rods in a low-index background a line defect can be formed by removing a row of these rods, which can act as a

waveguide for frequencies in the bandgap of the crystal [58-60]. This term for PCF was stated by Russell in 2003 [53]. Photonic crystal fibers can be divided into two modes of operation, according to their mechanism for confinement: Solid core and hollow core (Figure 2-5(a-b)). They are typically made of silica. The spatial structure of the air/silica index variation determines if the core is solid or hollow. Solid core PCF works based on TIR principle like a convention fiber. The advantage is that such kind of solid core waveguides can have a much higher effective refractive index contrast between core and cladding, and therefore results in much stronger optical confinement. Waveguiding in liquid-core HC-PCFs has successfully been demonstrated by several groups [54, 55]. The main areas of concern for using HC-PCFs in commercial sensors are side access to the fibers and the multimode nature for propagation. The number of modes can be reduced by filling the cladding holes with a suitable liquid. Neither of the Bragg fibers and 2D HC-PCF can be monolithically integrated on a planar optofluidic platform in a straightforward way.

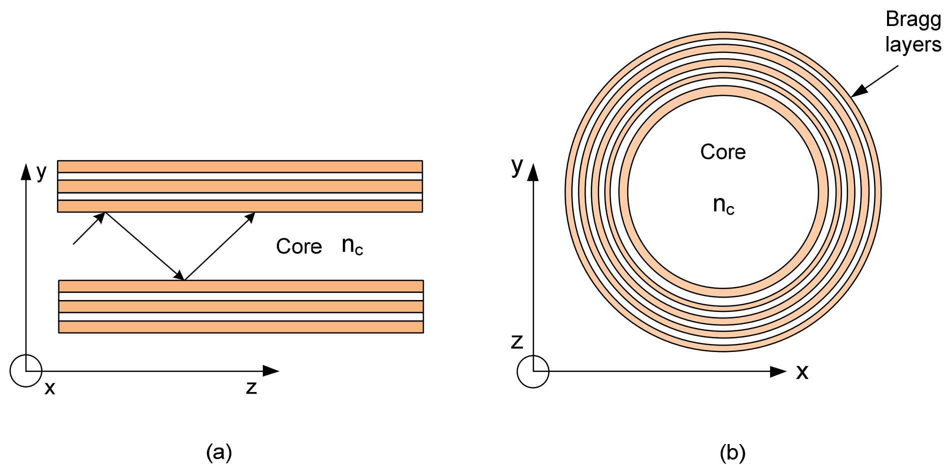


Figure 2-4: Cross section of (a) Bragg waveguides (b) Bragg fiber

2D PC waveguides [56] are not restricted to holy fibers which have cylinder cores. As depicted in Figure 2-5(c), light propagates along the z+ direction in the x-z plane which is confined by PC in x direction and index guiding in y direction. The concept was first realized using a central solid core silicon waveguide surrounded by periodic air holes to facilitate light guiding around tight bends [61]. A compelling feature of these PC waveguides compared to their fiber counterparts is their planarity, which is highly attractive for planar optofluidic integration. So far, 2D PC waveguides have not yet been applied with liquid core channels, it is a possible approach to the analysis of sample analytes in the LCW although.

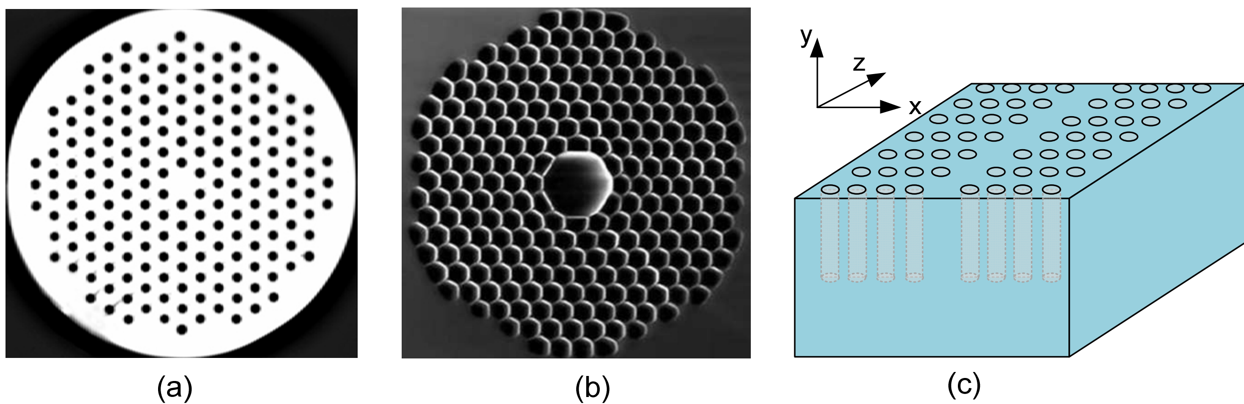


Figure 2-5: Cross section of PCF (a) solid core and (b) hollow core fiber, (c) 2D PC waveguides

2.3 ARROW Waveguides

2.3.1 Introduction

Antiresonant reflecting optical waveguides (ARROWs) is another type of interference-based waveguides. Antiresonance is a well-known effect in Fabry-Pérot interferometers: light is in antiresonance when it interferes destructively with itself inside a Fabry-Pérot cavity. ARROW waveguides work as an anti-resonant Fabry-Pérot reflector, using antisonance effect to confine

the light in the low-index core. The side view of an ARROW waveguide is shown Figure 2-6. n_c and d_c are the refractive index and the thickness of the core respectively. The light propagates along z direction in the y-z plane with a propagation constant β confined in x and y direction by the cladding layers. To perform as a Fabry-Pérot reflector, the cladding layers have to fulfill the antiresonance condition, which is given by

$$\Phi = 2t_j k_T + \Phi_r = (2m+1)\pi\,, \tag{2-3}$$

where m is an integer, t_j is the thickness in the j-th layer and Φ_r is the total phase shift from reflection at the two interfaces with the adjacent layers. The thickness of the j-th layer can be solved to be

$$t_j = \frac{\lambda}{4n_j^2} m \left[1 - \frac{n_c^2}{n_j^2} + \frac{\lambda^2}{4n_j^2 d_c^2}\right]^{-0.5} \approx \frac{\lambda}{4} m \left[n_j^2 - n_c^2\right]^{-0.5}. \tag{2-4}$$

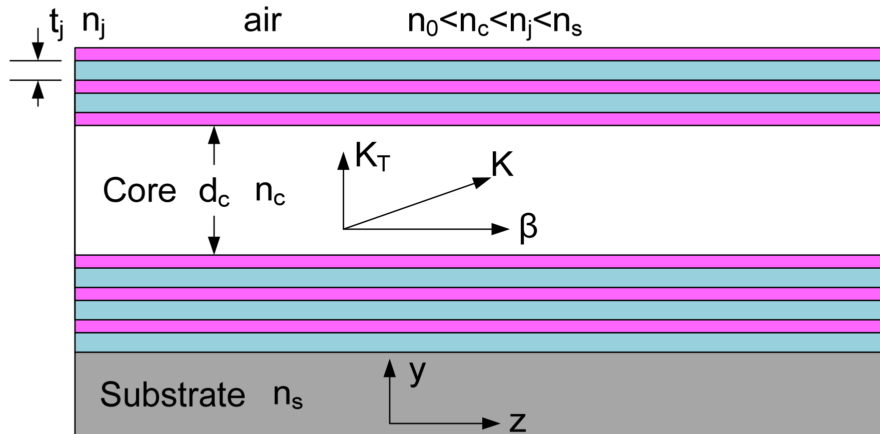


Figure 2-6: Side view of a hollow core ARROW waveguide

For a rectangular-core ARROW waveguides structure shown in Figure 2-7 (a-b), the optical wave is regarded as being confined in both transverse (y) and lateral (x) direction. A ray

model commonly referred to as the “transfer matrix method” or “2x2 matrix formulations” is used to solve the amplitudes of electromagnetic fields in the cladding layers of the ARROW waveguide. The field amplitudes are then used to calculate the reflection and transmission through the ARROW cladding layers, which allow us to estimate the optical loss. The minimum TE and TM loss for an ARROW waveguide (n_1 and n_2 are refractive indices of alternating layers, $n_c<n_2<n_1$) is given by [62]

$$\alpha_{TE,min} = \left(\frac{n_2^2-n_c^2}{n_1^2-n_c^2}\right)^{\frac{N}{2}} \alpha_0 \; , \tag{2-5}$$

$$\alpha_{TM,min} = \left(\frac{n_1}{n_2}\right)^{2N} \frac{n_1^2}{n_c^2} \alpha_{TE,min} \; , \tag{2-6}$$

where N is the number of antiresonant layers and for mode order m=0, 1, 2, 3……..,

$$\alpha_0 = \frac{\lambda_D^2 (m+1)^2}{n_c d_c^3 \sqrt{n_1^2-n_c^2}} \; . \tag{2-7}$$

From the above equations, it can be seen that the waveguide loss depends on the polarization of the incident light. The total loss will depends on the structure of the waveguide. For a 2D rectangular ARROW waveguide shown in Figure 2-7(a-b), the total loss can be approximated very well by using two separate 1D loss calculations and adding the resulting 1D-losses [14, 63]. This approximation has shown to agree very well with full 2D simulations with commercial modeling software such as FIMMWAVE (Photon Design) [19]. In the common case, if x-polarized light propagates along the z direction of the ARROW waveguide as illustrated in Figure 2-6, the vertical structures contributes to TE loss and the horizontal structure contributes TM loss (Figure 2-7(c-d)). The polarization dependence for ARROW waveguides arises from the fact that TM reflections are significantly lower than TE reflections, by the same phenomenon which gives rise to the Brewster angle [64], and this leads to higher losses for TM modes. This can be also explained by Equation (2-5) and (2-6). Because of this, the waveguide

should generally be wider along the x direction to minimize this contribution and decrease the waveguide loss. For example, for an x-polarized light propagating, the dimension of ARROW waveguide in the x direction has to be larger than that in the y direction. Simulations show that the loss decreases with increasing core width [22]. The maximum width of the waveguides is essentially determined by the fabrication yield of the devices, with wider waveguide channels more susceptible to breakage during sacrificial core removal. In order to obtain low-loss single-mode waveguides with high fabrication yield for x-polarized incident light, the optimal waveguide sizes were determined to be 5-6 μm in height and 12-15 μm in width.

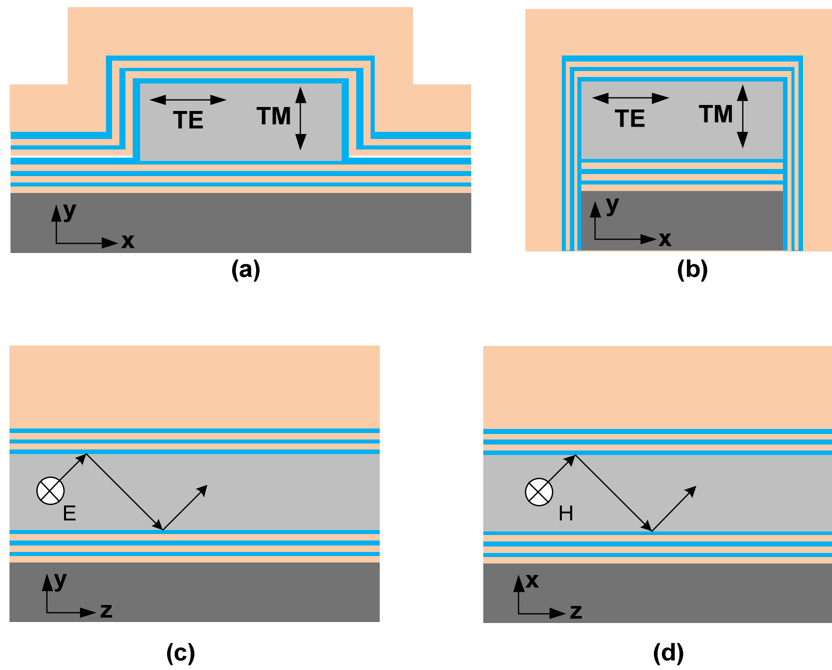


Figure 2-7: (a) Regular ARROWs built on a flat substrate, (b) self-aligned pedestal ARROWs, (c) vertical structure with transverse electric light incident and (d) horizontal structure with transverse magnetic light incident

Low-loss ARROW waveguides can be built without relying on the periodicity of the layer structure. To function as an antiresonant layer, each cladding layer must only satisfy the

antiresonant condition stated above, regardless of the number of cladding layers employed. While only a single antiresonant cladding layer below the core is necessary to confine most of the optical power to the core, higher confinement is produced and the waveguide loss is reduced with additional antiresonant layers. For each additional pair of layers, the loss decreases by ~3× which is shown in Figure 2-8. This suggests a design tradeoff between waveguide loss and fabrication complexity. The waveguides discussed in this dissertation use three pairs of layers around the core. For the topmost silicon oxide, this layer is much thicker than other layers because it mainly provides structural support for the hollow waveguide and creates a layer where solid core waveguides can later be etched.

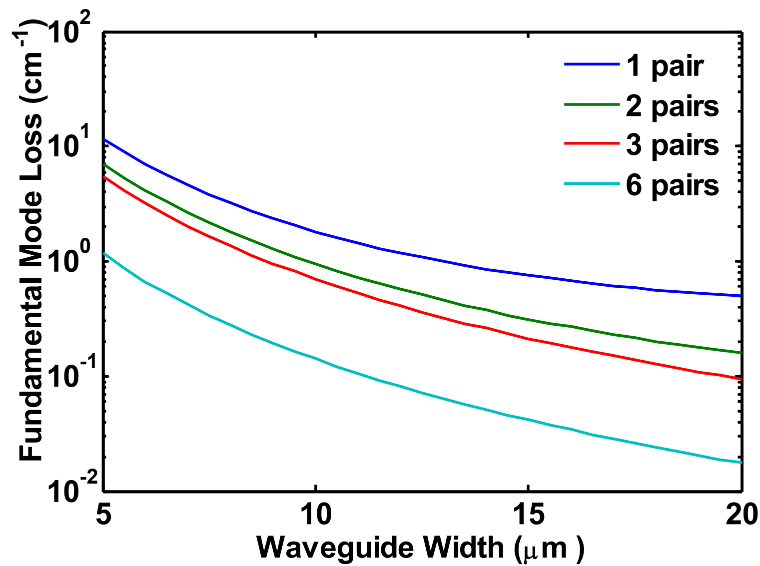


Figure 2-8: The waveguide losses for different numbers of cladding layer periods surrounding the water filled core (designed for 690nm).

Using these assumptions, calculations for different waveguide parameters can be made to determine the losses of the rectangular ARROW structures shown in Figure 2-7(a). The optimal antiresonant layer thicknesses for SiO_2/Ta_2O_5 ARROWs are calculated and listed in Appendix C.

Figure 2-9 shows the calculated loss through a hollow ARROW versus wavelength. From this graph, it can be seen that the transmission of ARROWs can be quite spectrally broad, which is to be expected because ARROWs use the relatively broad antiresonant regions of a Fabry-Perot cavity. For the ARROW waveguides considered here, the tolerance is on the order of λ/10 [63], which corresponds to 60-100 nm for the visible to near IR range. Simulations show that a 5% deviation in thickness in a single layer will increase the loss by ~1% [65]. The sensitivity of loss to thickness variation decreases slightly for the outmost layers. A 5% variation on all layers can increase the loss by 8%. As a result, the fabrication tolerances are not very stringent which lessens the controls necessary in microfabrication steps.

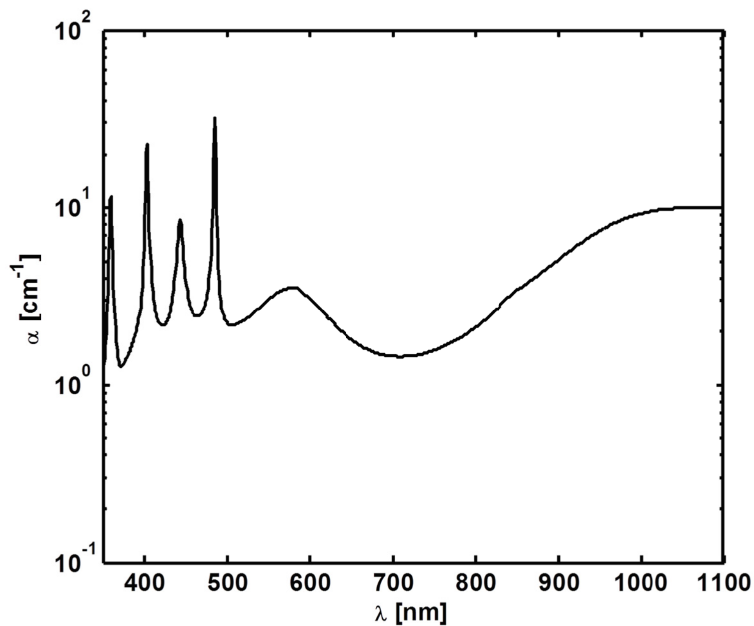


Figure 2-9: ARROW waveguide loss calculated for 3 periods of antiresonant layers (SiO_2/Ta_2O_5) surrounding a core

Comparing with the ARROW structures in Figure 2-7 (a) , the optical loss of a self-aligned pedestal (SAP) ARROW structure (Figure 2-7 (b)) is significantly decreased since the

device has air boundaries horizontally and vertically (ideally). For the x-polarized light, the vertical structure (the core height) which confines the TE mode contributes more to the total loss. This is conversely true for y-polarized light. Using the design in Appendix C, the loss of SAP SOC ARROWs with TaO/SiO is shown in Figure 2-10.

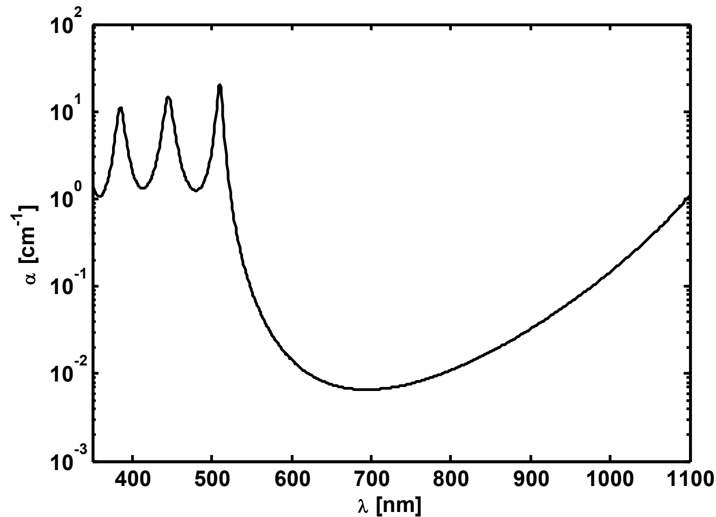


Figure 2-10: SAP ARROW ((SiO_2/Ta_2O_5)) waveguide loss calculated with the design layer thicknesses

2.3.2 ARROW Fabrication Basics

The ARROW concept was first implemented in solid-state waveguides to guide light using SiO_2/Si [64] and InGaAs/InP [66] material systems. The use of hollow core ARROW waveguides were first reported in 1995 using TiO_2/SiO_2 [67] as alternating ARROW layers with a 20×20 μm^2 core dimension. Recently, other material systems were proposed to make ARROWs, such as SiO_2/Si_3N_4 [14, 68-70] and SiO_2/Ta_2O_5 [71]. The compatibility of these materials with standard microfabrication processes make them attractive for making optofluidic platforms.

For the most parts, hollow core ARROW waveguides have been demonstrated using either wafer bonding or sacrificial etching approaches. In the former case (Figure 2-11), hollow core channels were fabricated by first dry etching deep trenches into a silicon wafer (lower wafer). Dielectric layers, serving as claddings, were deposited on the etched wafer as well as a flat wafer and the two were then bonded. Using the wafer bonding technique, a multimode ARROW waveguide which has a cross section of 130µm×130µm was fabricated by Bernini et al. in 2007 [70]. More recently, an ARROW waveguides (core dimension <10µm) of single mode were fabricated successfully based on wafer bonding technique after atomic layer deposition (ALD) was introduced into the process for the deposition of the dielectric layers [72].

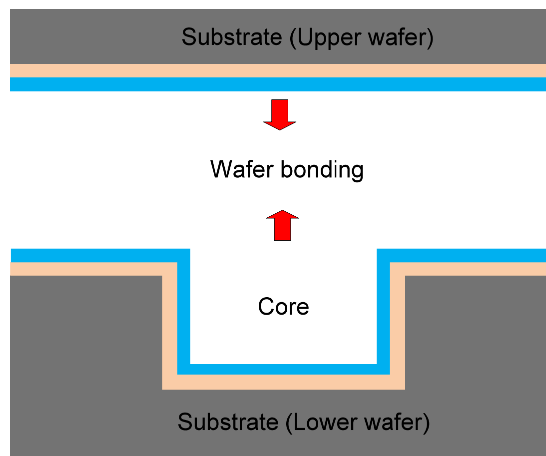


Figure 2-11: Hollow core waveguides fabricated with wafer bonding techniques.

Figure 2-12 shows the standard fabrication process of a rectangular-core ARROW waveguide using sacrificial etching and thin film deposition techniques. Yin et al. reported the design and fabrication of this (quasi)single mode ARROW in 2004 [14]. This design provides great flexibility for integration of hollow core ARROW waveguides with solid core waveguides,

fluid reservoirs, and electrical elements on the same platform. Liquid-core ARROWs with small cross sections can be used for a variety of spectroscopic applications, including the fluorescence detection of dye molecules, liposomes, and virus particles [27, 33, 73, 74].

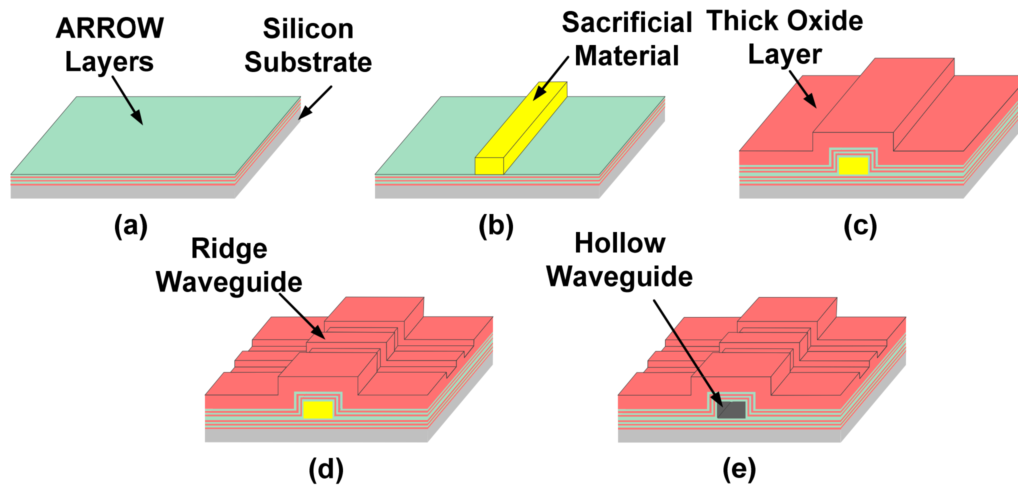


Figure 2-12: The fabrication process of hollow core ARROW waveguide using sacrificial etching method.

2.3.3 ARROW-based Sensing Platform

The platform with intersecting waveguides was proposed by Schmidt et al. in 2005 [19] and their use for single molecule detection (Alexa 647 dye molecules) using planar beam geometry was demonstrated in 2006 [23]. To build an on-chip ARROW platform shown in Figure 2-13(a), solid core waveguides are created on the same substrate to propagate optical signals on and off the chip and into and out of the hollow waveguides. The structure consists of the layers employed to create hollow core ARROWs (Figure 2-13(b)), including the thick SiO_2 layer used to increase the structural strength of the hollow waveguides. Ridges are then formed by plasma etching this topmost SiO_2 layer. Light is guided in this layer, confined by ARROW layers beneath and air on top and on the sides. The air-SiO_2 interfaces provide total internal

reflection (Figure 2-13(c)). Design rules were shown to optimize the ideal transmittance of the ARROW to greater than 98% and satisfy loss requirements [33]. Figure 2-13(a) demonstrates how an ARROW-based sensing platform for single molecule detection works. The solid core waveguides insect liquid cores perpendicularly. When the particles with fluorophores arrive in the intersection area, the excitation beam comes through the perpendicular solid core waveguides. Then the fluorescence signals are passed through the solid core waveguides and collected by the detector at the end of the chip. This configuration has two benefits. First, the excitation and fluorescence collection paths are spatially separated, leading to a substantial reduction in the number of background counts on the detector. Secondly, the excitation volume is lithographically confined on the micro-scale in all three dimensions by the LC-ARROW solid core waveguide intersection area. With this kind of configuration, the LC-ARROWs can still have two openings, where fluid reservoirs hold liquids with analytes can be attached. Electrodes can also be set up in the two reservoirs, so the sample material can be moved into the excitation volume due to the electrokinetic movement by applying a voltage. The ARROW platform has been demonstrated for both fluorescence [27] and surface-enhance Raman scattering (SERS) [75] detection.

To get a high-sensitivity ARROW-based sensor described above, the whole ARROW chip should have high edge-to-edge transmission from input to output. This ensures enough fluorescence signals can be detected by the detector. In order to design integrated ARROW platforms with interfacing between solid and hollow core ARROW waveguides, the ARROW design process is altered slightly from the design for only hollow-core waveguides. This process begins with calculating the minimum antiresonant layer thickness for the cladding materials and core size. After this, the thickness of the cladding layers on the sides and top of the core are

varied to account for the deposition thickness difference on these surfaces (see Chapter 3). The layer thicknesses on the sides and the top of a rectangular waveguide are related through a different ratio for Ta_2O_5 and SiO_2 layers.

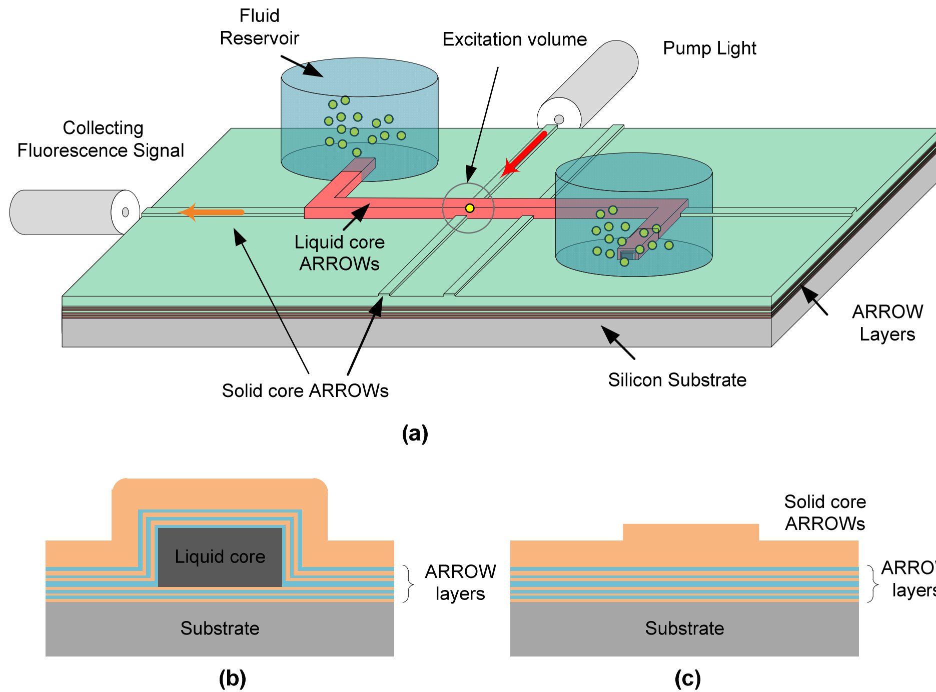


Figure 2-13: Diagram of (a) ARROW sensing platform, (b)hollow core ARROW waveguide (c) solid core ARROW waveguide

In addition, noise from the environment also plays a significant role in the detection system. There are several important sources for this noise. One important source of noise is the photoluminescence (PL) of the cladding materials. PL is produced in the ARROW waveguide when cladding materials absorb photons from the excitation beam and then re-radiate photons which form the beam with a red-shift compared to the excitation beam. Quantum mechanically, this can be described as an excitation to a higher energy state and then a return to a lower energy state accompanied by the emission of a photon. Typically, the relevant photoluminescence range

for cladding materials is from 660nm to 700nm for bimolecular detection on ARROWs with a pump beam of 633nm. PL at other wavelengths can be removed with a band pass filter.

3 ARROW FABRICATION PROCESS

3.1 General Process Preview

As discussed in Chapter 2, the objective of the research described in this dissertation was to develop a robust method to integrate a sensing platform with hollow ARROW waveguides and solid ARROW waveguides on planar substrates (Figure 2-13). The fabrication methods were designed to utilize standard semiconductor processes and equipment available in the BYU Integrated Microfabrication Laboratory (IML). The optical design and some measurements for the ARROW chips were performed at UC Santa Cruz, while the fabrication process was carried out entirely at BYU.

Silicon substrates with <100> orientation were chosen to create optical facets with both solid and hollow-core waveguides. With <100> silicon wafers, the orientation of the silicon crystal lead to perpendicular breaks as the wafer is cleaved, which is desired for creating high-quality optical facets for optical waveguides. All silicon substrates used in this work were 4 inches in diameter. The basic process flow for hollow-core ARROW waveguide fabrication is shown in Figure 3-1. First, alternating antiresonant layers consisting of silicon dioxide (SiO_2) and silicon nitride (SiN) or SiO_2 and tantalum oxide (Ta_2O_5) are deposited by plasma-enhanced chemical vapor deposition (PECVD) system or sputtering on the silicon substrate to keep light from leaking into the high-index silicon substrate (Figure 3-1(a)). Next, the sacrificial core is deposited and patterned by photolithography (Figure 3-1(b)). The core material is typically SU-8

or positive photoresist. The choice of core material affects the geometry of the hollow-core waveguide as well as the etchant used for core removal. Different types of core materials will be discussed in subsequent chapters.

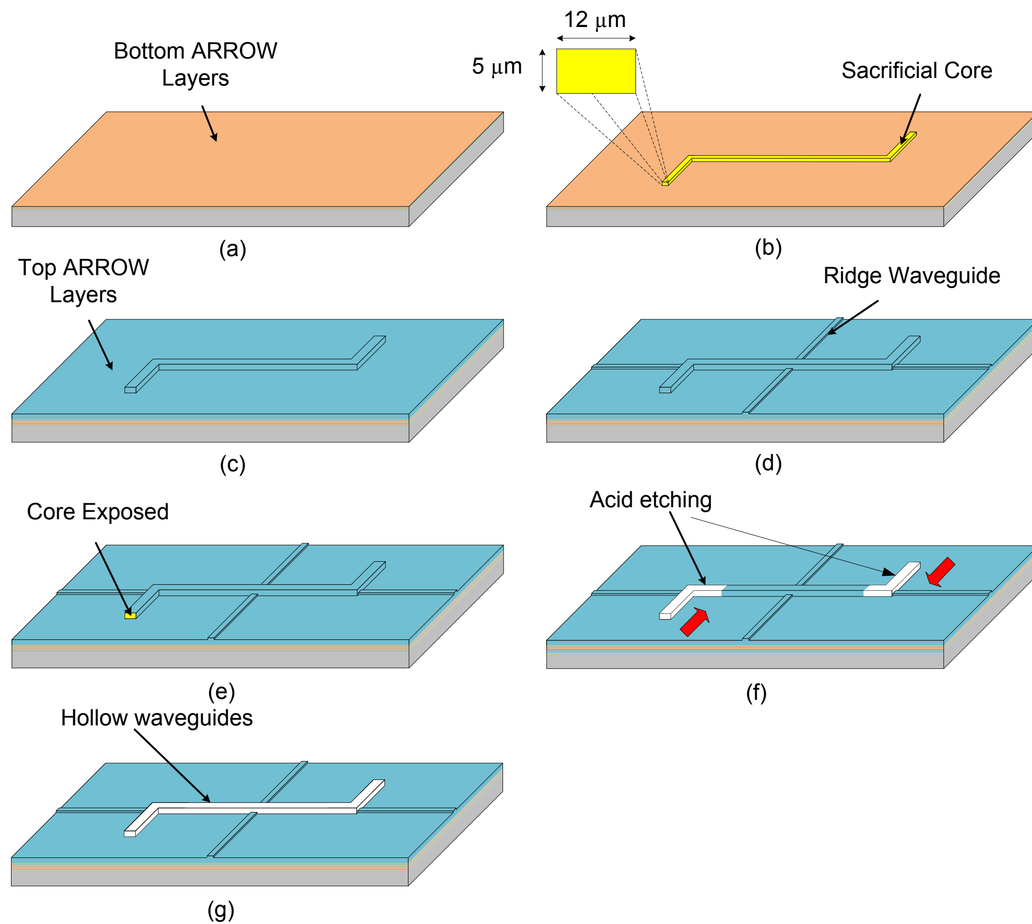


Figure 3-1: Basic process flow for ARROW platform fabrication (a) antiresonant layers deposited on a silicon substrate, (b) sacrificial core material patterned, (c) top antiresonant layers deposited, (d) ridge waveguides defined, (e) two openings etched at the ends of hollow waveguides, (f) acid etching from the two openings, (g) sacrificial core removed

After the sacrificial core is deposited and defined, the top antiresonant layers are deposited (Figure 3-1(c)) to provide light confinement on the sides and top of the waveguide as described in Chapter 2. The topmost layer is deposited thicker than the other layers (typically 3-

4μm) to provide mechanical strength for the hollow core waveguides and solid core waveguides is formed in this thick oxide.

Following the completion of hollow core waveguides as described above, ridge waveguides are then formed by dry etching the topmost SiO_2 layer (Figure 3-1(d)). Light is guided in this layer, confined by ARROW layers beneath and air on top and on the sides (the air-SiO_2 interfaces provide total internal reflection).

Finally, the ends of the sacrificial core material are exposed by plasma etching through the top layers (Figure 3-1(e)), and the sacrificial material is removed by acid etching (Figure 3-1(f)), completing the hollow waveguide (Figure 3-1(g)). Each of the processes employed in the fabrication of ARROW waveguides is described in detail in this chapter.

3.2 Sputtering

3.2.1 Introduction

Physical vapour deposition (PVD) is a common deposition method for metallic and dielectric thin-film deposition. The general idea of PVD is material ejection from a solid target material and transport in vacuum to the substrate surface.

Sputter deposition is a physical vapor deposition (PVD) method of depositing thin films by sputtering, that is dislodging atoms from target material and then depositing onto a substrate as a result of collisions of high-energy particles (Figure 3-2). The sputtering gas is usually an inert gas. Argon gas is applied on the Denton Sputter system. The sputter profiles depend on substrate temperature, working pressure, power, etc. In IML, sputter deposition is investigated for depositing various films, including metallic films and dielectric layers. In chapter 3, I will discuss how sputtered SiO_2/SiN/Ta_2O_5 films were used for ARROW waveguides. Comparing

with other techniques such as CVD, sputtering is an easier method for research because all the parameters can be adjusted independently.

A basic Denton sputterer system is demonstrated in Figure 3-3. As shown in the schematic diagram, the system is equipped with a power supply (DC or RF), an automatic matching network, and a coating chamber with three RF cathodes attached to sputtering targets.

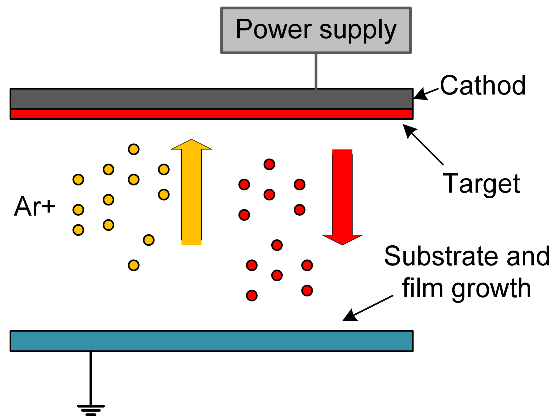


Figure 3-2: The principle of sputter deposition in a vacuum system

3.2.2 DC Sputter

The cathodes and substrate are planar plates. In the simplest case, one of the three cathodes is connected to DC voltage, while the substrate and chamber walls are grounded. So basically cathodes and substrates are two electrodes which make up a simple reactor for plasma. The target materials are installed on the cathodes. In a vacuum system, the chamber is maintained at low pressure, typically at 1mTorr~1Torr. In a chamber full of argon gas, several hundred of volts or several thousand of volts potentials are applied between the cathode and substrate. A small fraction of the population of argon atoms is initially ionized through random

processes (for example, thermal collisions among atoms). The ions (positively charged) are driven towards the cathode by the electric potential, and the electrons are driven towards the substrate by the same potential. Electrical breakdown of the argon gas in the reactor chamber occurs when electrons, accelerated in the existing field, transfer an amount of kinetic energy greater than the argon ionization potential to the argon neutrals. Such collisions generate a second free electron and a positive ion for each successful strike. The continuous generation of those new electrons prompts a sustained current and a stable plasma. Some collisions do not ionize the argon atoms which will strike the cathode with the kinetic energy. Bombardments from the argon atoms or ions on a cathode redistribute the energy until a portion of the cathode is ejected in the form of free atoms and secondary electrons. The free atoms with momentum from target materials will then deposit on the substrate, forming a thin film. It should be noted that the breakdown voltage (V_b) of working gas relies on the pressure (p) and distance (d) between electrodes according to the Paschen curve (Figure 3-4). The minimum value of V_b is achieved for a given p-d. The distance is usually ~10 cm for reactor chambers, so the pressure has to be high enough to achieve a low V_b or the applying voltage must be high enough to sustain plasma.

Since the ionization potential for most metal species is lower (e.g. 6~7 eV) than argon ionization potential (15.8 eV), the metal atoms can be easily ionized in the high-density argon plasma. DC sputtering systems work effectively for metals, including aluminum, gold, chrome, gold, nickel, etc.

3.2.3 RF Sputter

Before RF sputter is introduced, the concept of CCP (Capacitively Coupled Plasma) should be firstly described here. A typical CCP system, which consists of two electrodes separated by a small distance, is driven by a radio-frequency (RF) power supply

(typically at 13.56 MHz). One of two electrodes is connected to the power supply through a capacitor, and the other one is grounded. Driven by the RF power, electrons can quickly react to the high-frequency electric field but massive ions cannot. Electrons accumulated near the electrodes form a sheath region, which expels electrons and attracts ions. The powered electrode therefore automatically develops a negative DC bias because the capacitor does not allow electrons to discharge to ground. These energetic ions are exploited in many microfabrication processes (PECVD, sputter, and plasma etching) by placing a substrate on one of the electrodes.

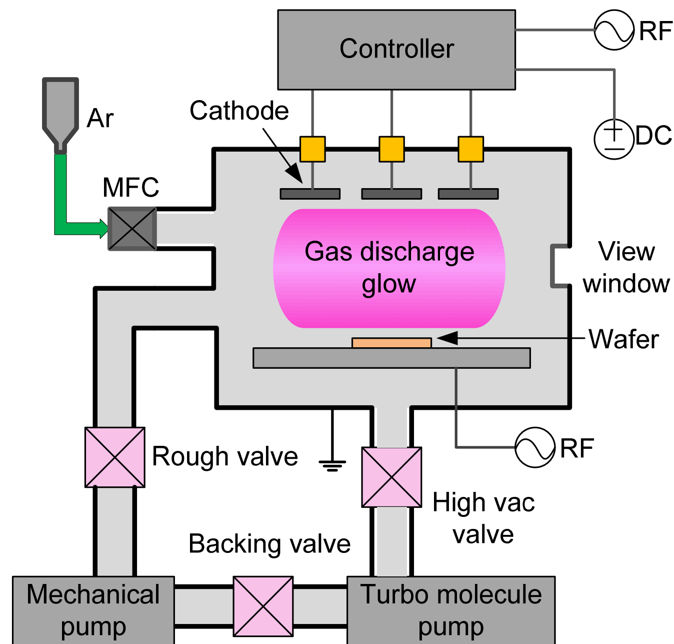


Figure 3-3: Diagram of Denton sputter system

For the Denton sputterer, argon gas is introduced into the chamber and an automatic pressure control valve can be adjusted to maintain the chamber pressure at the process set point in the range of 1~10 mTorr. The target materials are set up on cathodes, which are connected to a

RF power. The whole chamber wall makes up the other electrode which is grounded. The RF power applied between the two electrodes causes the free electrons to oscillate and to collide with gas molecules leading to sustainable plasma. RF-excited discharges can be sustained without relying on the emission of secondary electrons from the target. Electrons pick up enough energy during oscillation in an RF field to cause ionization, thus sustaining the plasma at relative low pressure. The tool uses a RF generator that supplies up to 350 W at 13.56 MHz. A matching network is placed between the RF generator and the chamber and provides automatic tuning to match the impedance of the load (the plasma chamber) to the impedance of the RF generator and cable. This is necessary to minimize the reflected RF power, which prolongs the life of the RF generator and allows for as much of the RF power as possible to be coupled into the plasma.

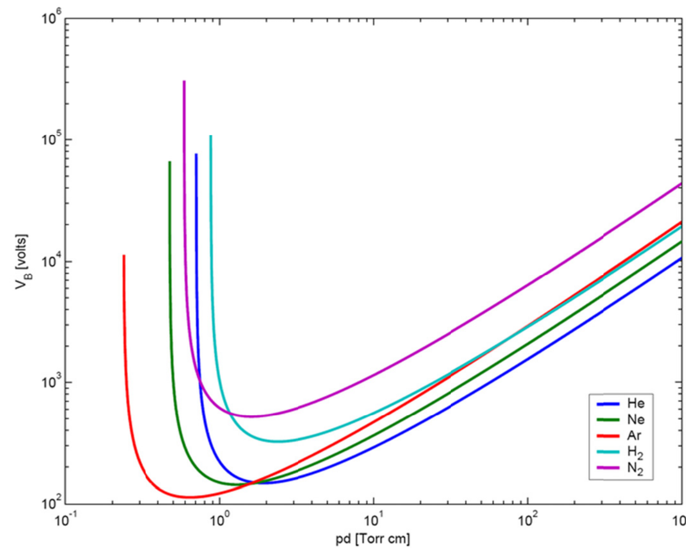


Figure 3-4: Paschen curve for different gases (Reprint from Wiki)

During the ARROWs fabrication process, CCP is necessary for deposition of dielectric films, including SiO_2, Si_3N_4, Ta_2O_5, etc. If a DC power is applied on these insulating materials,

positive charges will build up on the targets weakening the electric field and stopping sputtering eventually. High-frequency alternating current is introduced to the cathode so that the target is alternatively bombarded by positive ions and negatively electrons. The charges are neutralized avoiding the charge building up.

The wafer is placed on a rotating susceptor plate, which can be adjusted from room temperature up to 350 °C. The heat from the susceptor plate is transferred very evenly throughout the silicon wafer because of the high thermal conductivity of silicon. The rotating setup helps to improve the uniformity of sputtered films.

3.2.3.1 Low Temperature Deposition

During sputtering process, ion bombardment does not require high temperature and substrate temperature can be set to as low as room temperature. This provides more flexibility for the microfabrication process which is temperature-sensitive. The benefits of the lower temperature deposition make sputtered films attractive for many applications. The lower processing temperature of sputter allows for processing to be compatible with a much broader range of materials, including organic materials such as photoresist, which is necessary for the upper antiresonant ARROW layers. The ARROW waveguides with an arch-shaped cross section made with photoresist and low temperature sputtered layers will be discussed in Chapter 3.

The bombardments towards the cathodes could cause much heat, so water cooling is necessary for cathodes. Besides, parts of secondary electrons emitted by the cathodes due to ion bombardment are collected by the substrate which could cause unplanned heat on substrate. This is critical for low temperature deposition. Since there is no cooling line connected to the substrate, decreasing the power is a method to avoid overheating.

3.2.3.2 Adhesion

Adhesion is a critical issue for thin film depositions. As discussed above, top antiresonant layers of hollow ARROW waveguides are coated after the core is defined. So the adhesion between top layers and bottom layers is one of the most important factors that determine the yield of the devices. The devices get broken if the adhesion is poor.

The adhesion of materials to substrates depend on several factors, such as the properties of materials and substrates, substrate surface conditions, stresses in the film, contamination in the interface, roughness of the substrate, and the pre-cleaning chemical.

Pre-sputter cleaning promotes adhesion, especially for metal deposition. Before sputtering, the substrate can be sputter etched at a low power for a few seconds by connecting it to the negative pole of the power supply. In my research, a RF power of 50w is always applied to the substrate for around 15 seconds before any layers are deposited.

In addition, substrate heating and high RF power is beneficial for good adhesion because the absorbed atoms can have more energy to move around at the surfaces and fill in the voids so that they can make a film with high quality and density.

Furthermore, sputtering at low gas pressure leads to improved film adhesion. The mean free path of a molecule, λ, is given by:

$$\lambda = \frac{k_B T}{2^{1/2} P_T \pi d^2}, \quad (3\text{-}1)$$

$$\lambda \approx \frac{5\times10^{-3}}{P_T(torr)} cm \; at \; 300K, \quad (3\text{-}2)$$

where P_T is the total pressure, d is the molecular diameter, T is the reactor temperature, k_B is the Boltzmann constant. During the sputtering process with fixed temperature, the pressure ranges from 1~10 mTorr. According to Equation (3-1), λ (0.5~5cm) is shorter than the distance D (around 10 cm) between the target and the substrate. So the particles have to experience multiple

collisions before arriving at the substrate. At low pressure, sputtered atoms have much fewer scatterings and then they can gain more kinetic energy to move around on the substrate.

3.2.3.3 Conformality

Step coverage or conformality is the ability of a thin film coating to replicate the surface topography of the underlying substrate. It is defined as the ratio of film thickness along the sidewalls of a step feature to the film thickness at the bottom of the step. Achieving good sputtered layer conformality is critical for creating robust hollow waveguides because the structure is formed by encapsulating the sacrificial core with the alternating dielectric layers. A perfectly-conformal film would equally coat all sides of any topographical feature, including the rectangular sacrificial cores used for ARROW waveguide fabrication.

The step coverage of deposited films can be limited due to the shadowing effect as shown in Figure 3-5. The atoms approach the substrate at a large incident angle θ, they deposit on the outermost part of the surface while the walls and the lower part of the surface are shadowed by neighboring material.

As explained earlier, the atoms have to experience multiple collisions even at relative low pressure in a sputtering system, so the atoms arrive at the substrate with random incident angles which result in a better step coverage compared to evaporation. Furthermore, the sputtering target is very broad (3 inch for our Denton Sputter system) compared to an evaporation point source, the shadowing effect during the deposition decreases. Additionally, three sputtering targets are arranged in a specific circular pattern with a small tilt angle off the rotating substrate (Figure 3-6(a)).The tilt angle is chosen such that the particles obliquely incident on the patterned substrate can reach the sidewalls and bottom corners, therefore decreasing shadowing effect.

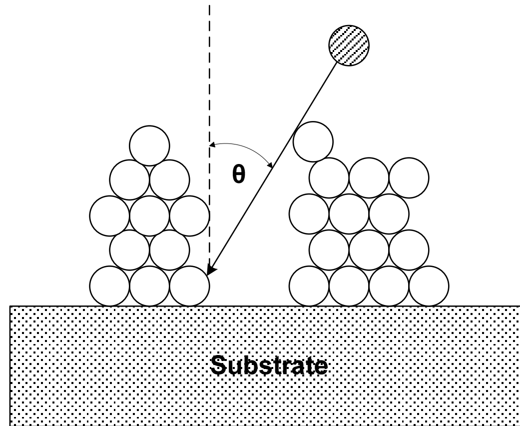


Figure 3-5: Illustration of the shadowing effect during thin film deposition. As angle θ increases, incoming atoms collide with the top of a trench and cannot create films on the trench's bottom and sides

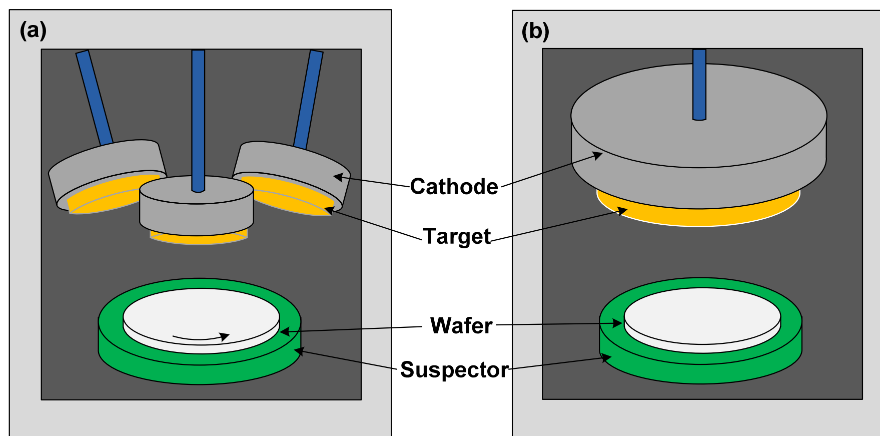


Figure 3-6: Configuration of sputter system (a) Denton sputterer - planetary position for targets, (b) direct sputterer - parallel position

In theory, the coating should be perfectly conformal if the particles have enough energy left for rapid surface migration before a bond is established with the underlying substrate (Figure 3-7(a)). This usually arises from fast surface diffusion at relatively high temperature (>700°C). However, the films deposited by evaporation, sputtering and PECVD often have similar profiles as shown in Figure 3-7 (b) because of their relative low deposition temperature. Although the

conformality of sputter is better than evaporation, it is not perfect for ARROW waveguides fabrication, especially at corners. The top layers of this profile over the core of hollow waveguides will introduce more optical loss and even lead to the low yield.

The conformality can be enhanced by increasing substrate temperature. Sputter at 250°C is preferred for rectangular-shaped ARROW fabrication. Optimized structures can also make up for the loss resulted from the non-conformal coatings which will be discussed later in Chapter 4 and Chapter 6 respectively.

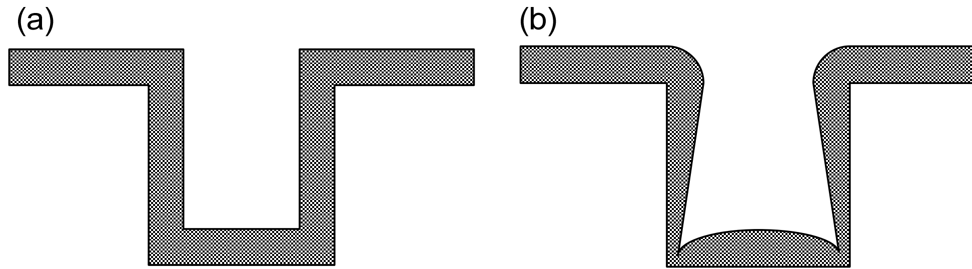


Figure 3-7: Profiles of deposition on rotated and heated substrate (a) ideally uniform coating due to rapid surface migration, (b) nonconformal coating for long mean free path and insufficient surface migration

Additionally, higher pressure leads to better step coverage. In order to characterize the relation between conformality and deposition pressure of sputtered films, three wafers were coated with a single TaO film of at 120w and room temperature over 5μm-high SU-8 cores with varying pressures. As illustrated in Figure 3-8, the cross sections of waveguides were imaged using SEM to measure the thickness ratio (dt/ds) of the films on the horizontal surfaces to that on the sidewalls of the rectangular core. The results are listed in Table 3-1. Although high pressure helps to enhance the conformality slightly, it results in worse adhesion and a rougher film. The pressure of 5 mTorr is typically chosen for ARROW layers deposition.

Because the conformality ratio can be found out by measuring the thicknesses of deposited film using SEM images, it can then be taken into consideration in the ARROW design to account for the unequal film deposition thicknesses. Designs are tailored to give the correct thickness of the vertical layers for a given horizontal film deposition thickness, since the loss is more affected by thickness variations in the side layers than in the top layers, as discussed in Chapter 2.

Table 3-1: The Conformality Ratio of Sputtered Ta_2O_5 at Different Pressure

RF power(w)	*Temperature (°C)*	*Pressure (mTorr)*	*Conformality ratio*
120	RT	1	1.81
120	RT	4	1.79
120	RT	10	1.77

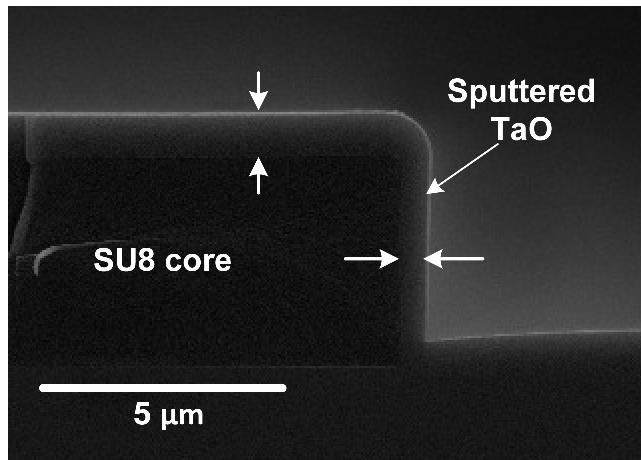


Figure 3-8: SEM images of sputtered TaO film deposited over a SU8 rectangular shaped sacrificial core with conformalities of 1.79

3.2.3.4 Uniformity and Repeatability

To make a low-loss ARROW chip, the refractive index and growth rate of cladding layers are expected to be as stable as possible. These parameters for sputtered films, especially

for Ta_2O_5 and SiN are very dependent on the deposition chamber conditions. As a result, the chamber is conditioned or seasoning of SiN or Ta_2O_5 to coat the walls of the chamber before they are deposited for a real ARROW wafer. The RF supply for sputter deposition is turned on when the chamber pressure is less than 5×10^{-6} Torr. Low backing pressure ensures that less contamination takes place in the process. This chamber seasoning must be performed if the chamber pressure is within 10^{-7} range (usually after pumping down for more than 10 hours).

The optimized recipes are shown in Table 3-2. The deposition temperature depends on the core material and the deposition rate mostly relies on the power. As described earlier in this chapter, ion bombardments towards the cathodes generate heat on them. Therefore if the RF power is too high, the cathodes cannot be sufficiently cooled down by the water cooling system, the targets, especially for insulating materials can be damaged. A thin silver paste layer is always applied between the targets and the cathodes, helping to dispense the heat generated during the deposition. The power for SiO_2 and SiN is recommended to be 300w and 120w for Ta_2O_5. The deposition rate is approximately 5~6 nm per minute. At this growth rate, substrate and cathode do not get too much heat. This growth rate is acceptable since the layers are not very thick in the ARROW designs. Actually, low deposition rate is beneficial for precise control of layer thickness.

Table 3-2: Recipes for Sputtered SiO_2, Si_3N_4 and Ta_2O_5

	Argon pressure (mTorr)	*Gas flow (sccm)*	*Temperature (°C)*	*RF Power (w)*	*Deposition Rate (nm/min)*
SiO_2/Si_3N_4	5	88.5	RT~250	300	5~6
Ta_2O_5	5	88.5	RT~250	120	5~6

As demonstrated in the configuration of Figure 3-6(a), three 3-inch sputtering sources are aimed at a common focal point. When a substrate is placed in the vicinity of this focal point

and rotated on its own axis, it is possible to deposit highly uniform and relative conformal single layers or multi-layers which are very important for ARROW fabrication. In other systems, the substrate can be positioned or moving directly in front of and parallel to the sputtering source targets (Figure 3-6(b)). Comparing with the former configuration, the target diameters should be about 20% to 30% larger than the substrate to achieve reasonable uniformity. Although this configuration is much less flexible and generally more expensive than con-focal sputtering, it has its place in production applications which require maximum deposition rates (semiconductor wafer metallization), applications which utilize large substrates (e.g. flat panel displays) and a few techniques that demand "line-of-sight deposition" (e.g. "lift-off").

To characterize the repeatability and uniformity of deposited films, a total of five 4-inch wafers were run through the sputter and then were measured on the ellipsometer to determine the run-to-run variability of the films. Multiple measurements were taken at several different positions across a wafer as shown in Figure 3-9. Repeated measurements of the same location on a wafer give the same result, implying that the repeatability of the ellipsometer is good enough for our applications.

Before growing the tantalum oxide films, a chamber seasoning was performed for 15 minutes. After seasoning, each of 5 wafers was deposited for 12 minutes consecutively by using the recipe provided in Table 3-2, getting a nominal film thickness of 70 nm. The normal film thickness chosen give high measurement sensitivity in the ellipsometer, and are the test wafer thickness used to determine growth rates during the actual ARROW fabrication process.

The results for sputtered Ta_2O_5 are demonstrated in Figure 3-10 and Figure 3-11. From the two figures, it can be concluded that the thickness and refractive index of Ta_2O_5 maintain

relatively stable. It is found that variability of thickness from wafer to wafer is less than 2.5% and that of refractive index is less than 0.04%.

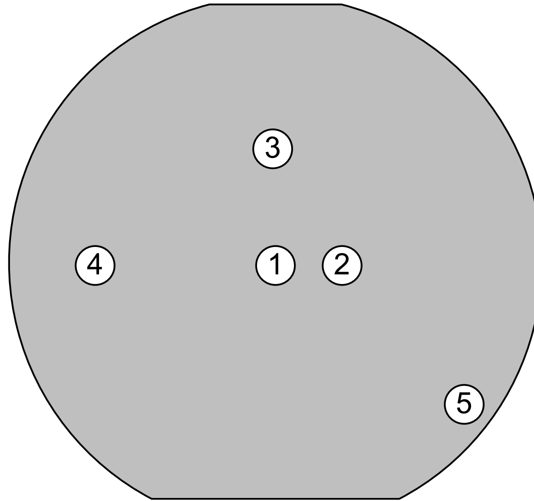


Figure 3-9: Measurement locations for sputtered test wafers

In addition, the uniformity of sputtered Ta_2O_5 films is quite good. Multiple measurements for one test wafer were performed at different positions (Figure 3-9). The thickness values vary by less than 3.1% across a wafer, while the refractive index varies approximately 1.2% across the wafer.

With the same method, the measured results of SiO_2 are shown in Figure 3-12 and Figure 3-13 with a nominal film thickness of 120nm. The thickness values vary by less than 2.9% across a wafer, while the refractive index varies approximately 1.0% across the wafer. The variability of thickness from run to run is less than 2.5% and that of refractive index are less than 0.7%. These results indicate that Ta_2O_5 and SiO_2 uniformity across a wafer is well within acceptable limits based on the tolerance of ARROW waveguides to thickness variations discussed in Chapter 2.

Figure 3-14 and Figure 3-15 illustrate the uniformity of sputtered Si_3N_4 films. Compared SiO_2 and Ta_2O_5, sputtered SiN films has more variation for the refractive index as shown in Table 3-3. This is because the amorphous SiN films tend to incorporate oxygen in the film at low concentrations and the index is very sensitive to the Si:O:N ratio. The relative large variation from run to run makes SiN films inferior to TaO films for ARROW waveguides because it is challenging to make ARROW waveguides within acceptable tolerances.

From all the graphs above, it can be seen that the variability of thickness and index follow the same pattern for each wafer according to the measurement locations. As the distance between measurement locations to the center increases, the thickness of films decreases. I believe this is caused by the configuration of sputtering sources.

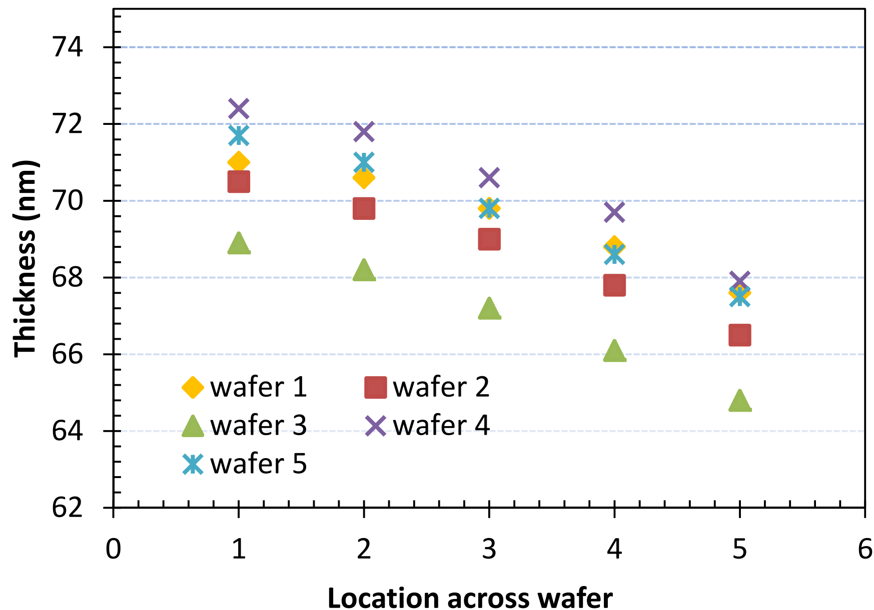


Figure 3-10: Measurements for thickness of 5 sputtered Ta_2O_5 films (RT) at different locations

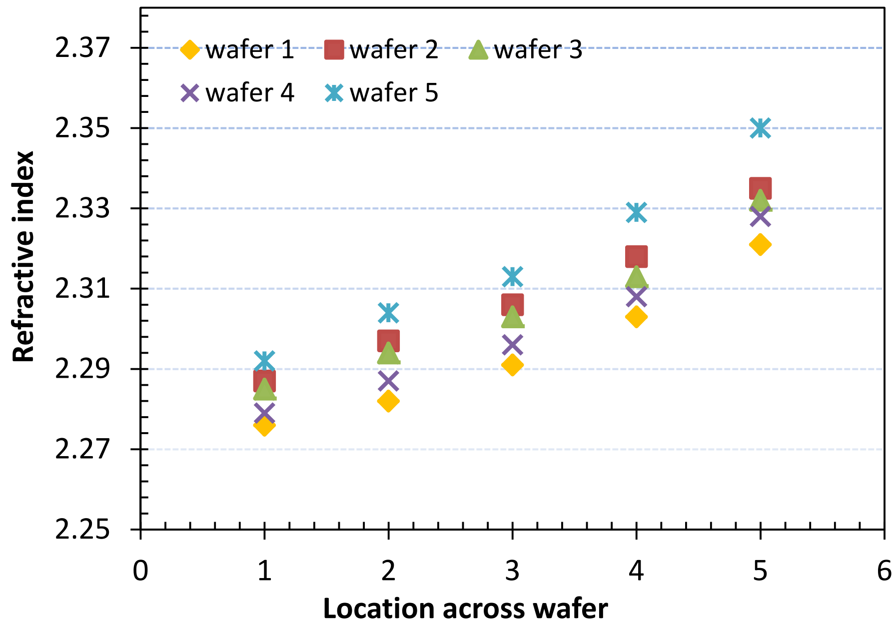


Figure 3-11: Measurements for refractive index of 5 sputtered Ta_2O_5 films (RT) at different locations

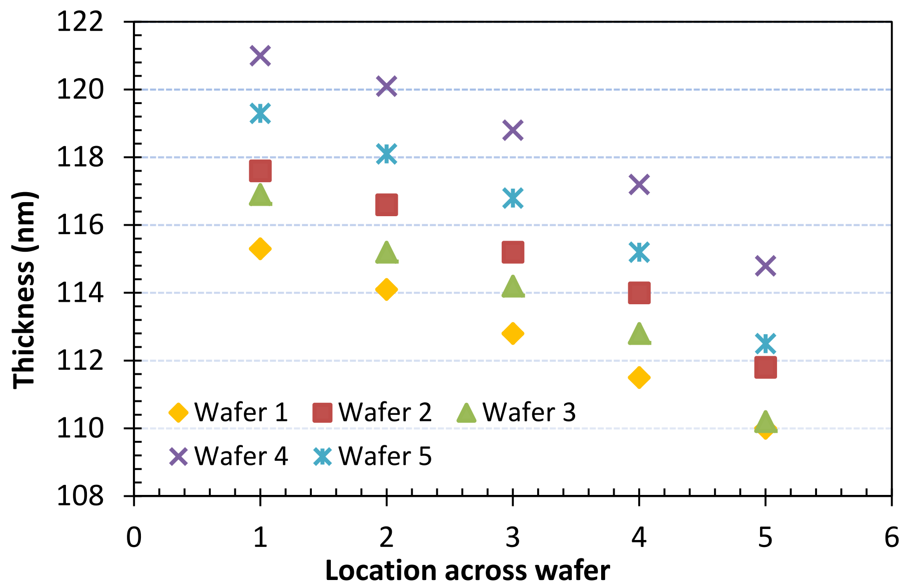


Figure 3-12: Measurements for thickness of 5 sputtered SiO_2 films (RT) at different locations

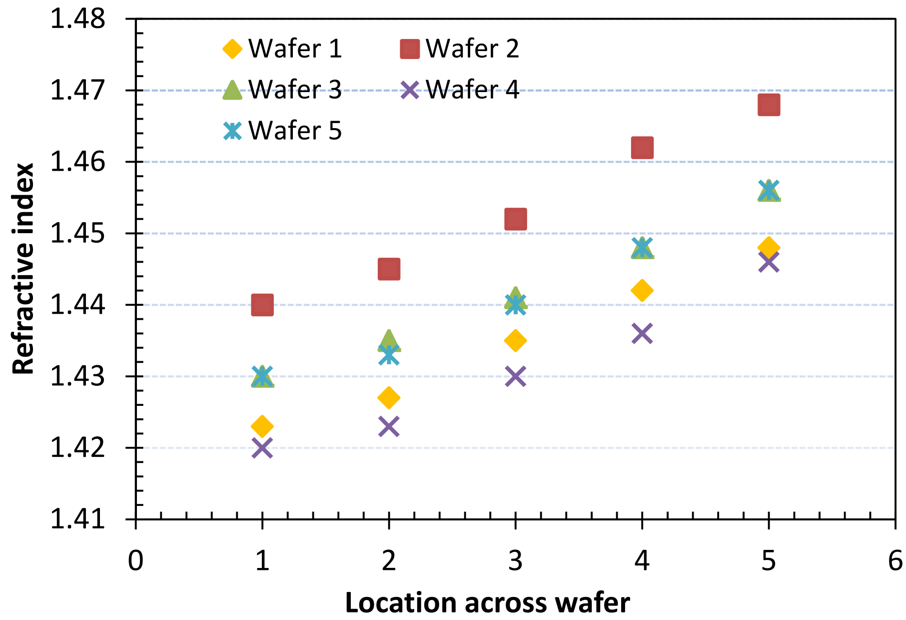


Figure 3-13: Measurements for refractive index of 5 sputtered SiO_2 films (RT) at different locations

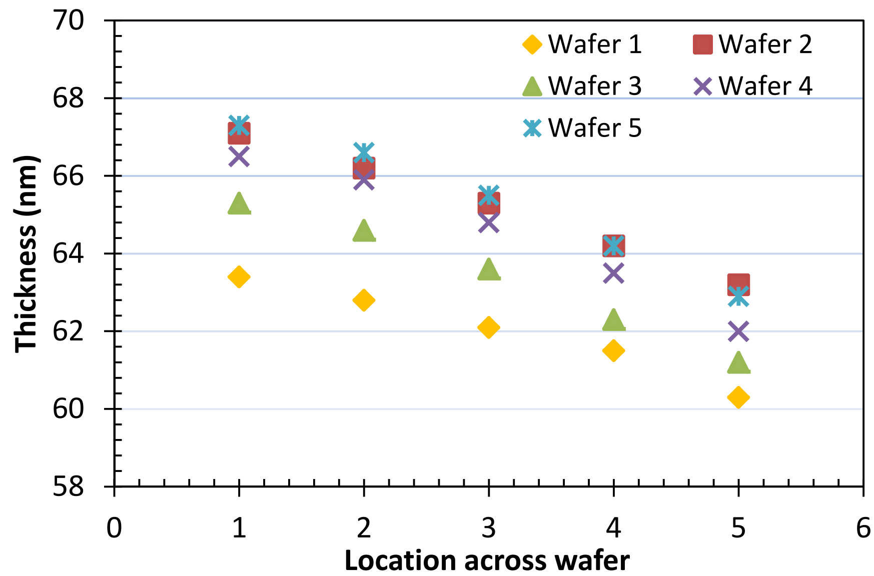


Figure 3-14: Measurements for thickness of 5 sputtered Si_3N_4 films (RT) at different locations

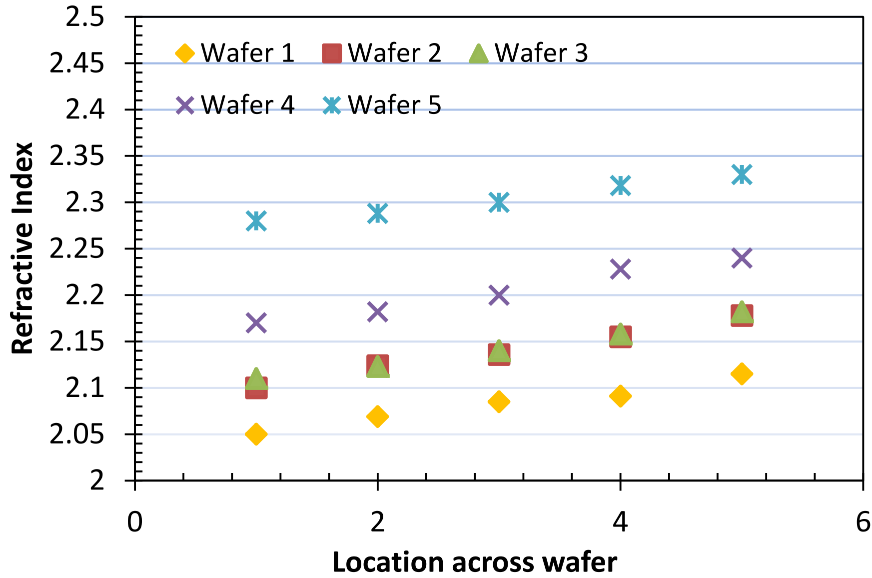


Figure 3-15: Measurements for refractive index of 5 sputtered Si_3N_4 films (RT) at different locations

The same experiments were carried out at different temperatures using the recipe in Table 3-2. For the Denton sputterer in our IML, the growth rate and refractive index are very stable.

Table 3-3: Comparison of Uniformity and Variability for Sputtered Ta_2O_5, SiO_2 and Si_3N_4

Name	*Nominal film thickness (nm)*	*Uniformity*		*Variability from run to run*	
		Thickness	*Refractive Index*	*Thickness*	*Refractive Index*
Ta_2O_5	70	3.1%	1.2%	2.5%	0.04%
SiO_2	120	2.9%	1.0%	2.5%	0.7%
Si_3N_4	70	3.4%	1.8%	3.0%	5.9%

3.3 PECVD

3.3.1 Introduction

Chemical vapor deposition (CVD) is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films.

Figure 3-16 schematically illustrates the basic reaction mechanisms in a CVD process. The reactants enter the chamber through the gas inlet and are distributed evenly by the shower head before they begin to react. The reactions are maintained by the energy from RF power and heat. The precursors, byproducts and reactant gases are then adsorbed on the surface of the substrate. On the heated surface, the atoms can move around with a certain kinetic energy and then are incorporated as film constituents into the growing film. The by-products of the reactions transport from the surfaces toward the reactor exit.

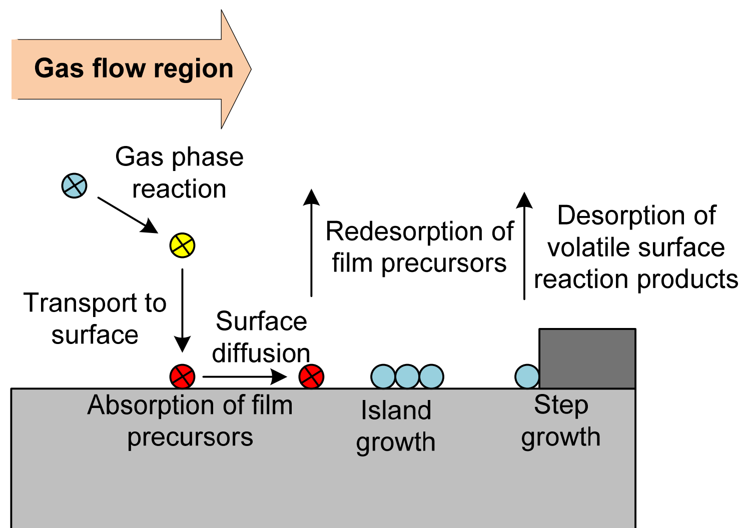


Figure 3-16: Schematic of transport and reaction mechanisms for a CVD process

Energy which is used to drive reactions can be supplied by several methods, such as thermal, photons, plasma, etc. Plasma-enhanced chemical vapor deposition (PECVD) is a process that utilizes plasma to enhance chemical reaction rates of process gases. Figure 3-17 demonstrates the typical reactor system for PECVD in our IML. In this setup, a capacitively coupled plasma transfers energy into the reactant gases, allowing the substrate to remain at lower

temperatures than in atmospheric pressure CVD (APCVD) and low-pressure CVD (LPCVD). The energy for the PECVD process is provided by plasma rather than heat, so it allows deposition at low temperature (typically between 200°C~300°C). Compared with sputter deposition, PECVD films usually have good adhesion, low pinhole density, good step coverage, and compatibility with fine line-width pattern transfer processes have led to wide use of PECVD in VLSI.

3.3.2 PECVD SiO_2 and SiN

The most commonly used films deposited by PECVD include silicon dioxide (SiO_2) and silicon nitride (SiN) which are applied for electrical isolation, passivation, optical waveguides, and optical coatings. As described earlier, PECVD SiO_2 and SiN are used to seal the core material during the process of making ARROW waveguides. While very high-quality SiO_2 and SiN films can be grown using thermal oxidation (~1150°C) or low pressure CVD (LPCVD) (500-900 °C), those process require very high temperature which is not compatible with the following step of hollow waveguides.

SiH_4 (silane)/He and N_2O serve as the reaction gases to form silicon oxide films. Equation (3-3) describes how these precursors react in a PECVD chamber. Actually PECVD oxide is amorphous and non-stoichiometric. This means that instead of growing stoichiometric SiO_2, what really is deposited is SiO_xH_y, with the hydrogen coming from the precursor gas silane. Because of this, the film has lower density than thermally grown SiO_2. PECVD oxide is not as a good electrical insulator as thermal oxide. It is noted that only a slight portion of hydrogen is incorporated into the film so that the whole reaction is more like Equation(3-3). The typical refractive index of PECVD oxide is between 1.45 and 1.47. The index is maintained very

stable unless silicon-rich SiO_2 films are deposited with indexes as high as 1.58 by dramatically increasing the ratio of the silane to nitrous oxide (N_2O) source gases.

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2 \ . \qquad (3\text{-}3)$$

For SiO_2 deposition, the hydrogen and nitrogen present in the process is not incorporated into the growing film because oxygen atoms can readily locate silicon atoms within the amorphous film [76] and the oxygen atoms fill up the silicon bonding sites before the nitrogen can bond. Helium is not incorporated into the films because it is an inert gas. But helium might be trapped in voids in the films. However, the small size of the helium atom allows for it to easily escape from the low-density porous PECVD films.

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \ . \qquad (3\text{-}4)$$

Equation (3-4) describes the chemical reaction in making a silicon nitride film in a PECVD chamber. Changes in the Si:N ratio are manifest as variations in the refractive index of the nitride films. This ratio relies on many factors, including power, pressure, temperature, and gas flows. A lower ammonia flow can yield a higher refractive index (silicon-rich film) [77]. PECVD deposition of silicon nitride in our temperature range (250-300°C) has a large degree of hydrogen incorporation, with the hydrogen terminating uncompensated binding sites on both the silicon and nitrogen. Because of this, the amorphous deposited SiN film is often described as a ternary solid-solution alloy SiNH. In addition, oxygen is also incorporated in the nitride film at low concentrations. Oxygen can enter process gas mixture through leaks or by desorption from the chamber walls. Any oxygen contamination causes the deposition of SiON [78], which decrease the refractive index of the film [79]. To maintain the refractive index stable for ARROW fabrication, it is necessary to pump down the chamber for about 5 minutes before deposition. Since the film characteristics of SiN and SiO_2 are very dependent on the chamber

conditions, the chamber has to be conditioned or seasoned by pre-deposition of oxide or nitride to coat the walls of the chamber before any film is deposited for ARROW fabrication. This standard chamber seasoning procedures not only improve the stability of the refractive index, especially for nitrides, but also enhance the stability of the growth rate and film uniformity.

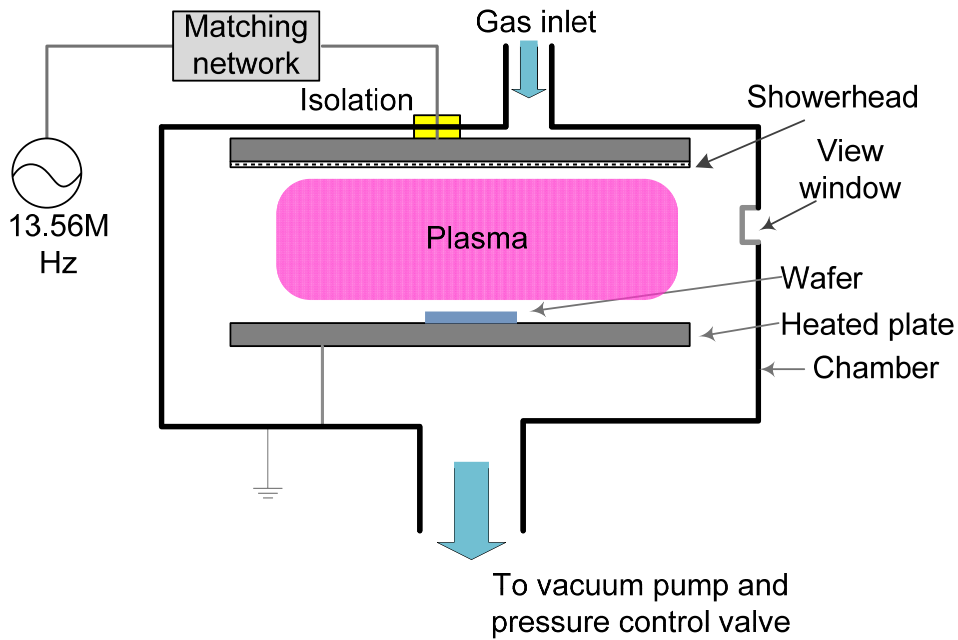


Figure 3-17: Diagram of PECVD

3.3.3 Uniformity and Conformality

As discussed in sputter section, PECVD films have similar step coverage profiles as sputtered films due to the shadowing effect. The conformality ratio of PECVD SiN films grown with PECVD 1 tool in IML is around 1.35. The conformality of SiO_2 films deposited with our PECVD 2 tool has more variation than that of SiN films (Figure 3-18(a-b)). For ARROW waveguides, good confomality is required for top layers over the core, especially for thick top

silicon oxide. With poor conformality, deep crevices form at the two corners of ARROW waveguides as shown in Figure 3-19. This leads to the cracks along the corners, result in device breaking during the wet etching process.

In addition, deep crevices decrease the coupling efficiency between solid core and liquid core waveguides due to the mode mismatching. This can be partially compensated by depositing a thicker top oxide which will be discussed in Chapter 4.

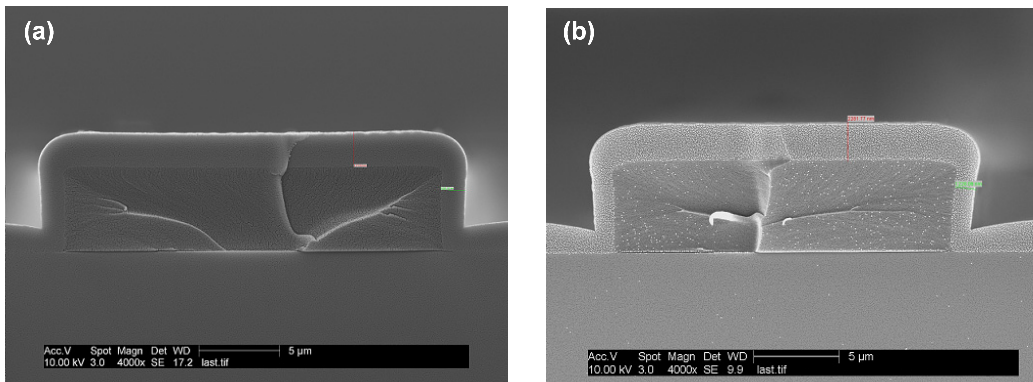


Figure 3-18: SEM images of SiO_2 PECVD films deposited over a SU8 core with conformalities of (a) 1.41, (b) 1.84

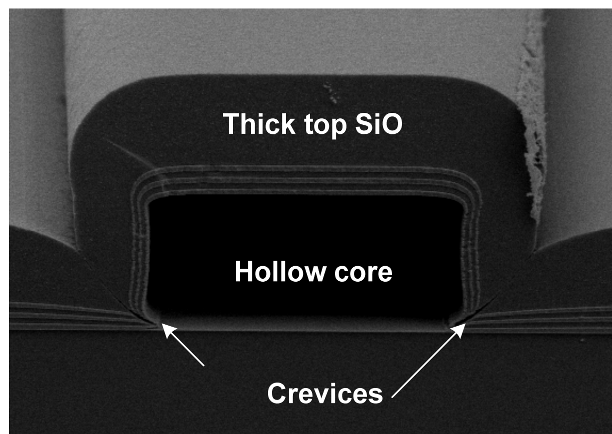


Figure 3-19: SEM image of a cross section of ARROW waveguide with crevices and cracks

A series of experiments show that a more conformal film can be deposited under high pressures and low RF powers. However a more uniform film has to be deposited under low pressure and low power. As a result, there is a trade-off between the conformality and uniformity of SiO_2 films. Table 3-4 shows two typical recipes for depositing of SiO_2 for ARROW waveguides. The SiO film deposited with Recipe 1 has higher uniformity but lower conformality than that made with Recipe 2. So Recipe 1 has been used to make ARROW layers beneath the core which do not require good conformality, while Recipe 2 has been used to make layers over the core, including the thick top SiO.

Table 3-4: The PECVD SiN and SiO_2 Feposition Recipes for ARROW Waveguides.

	Pressure (mTorr)	*Power (w)*	*Gas (sccm)*		*Conformality Ratio*	*Variation*	*Growth Rate (nm/min)*
			SiH_4/He	*N_2O*			
1	600	19.5	119	34	1.7	2%	45
2	1100	23	132	9	1.4	7%	35

3.4 Photolithography

Photolithography is an optical means to transfer patterns onto a substrate. It is essentially the same process that is used in lithographic printing. Lithography relies upon a light-sensitive material, called photoresist that is deposited on clean substrates. Typically, UV light is used to chemically alter solubility to a developer solution (development). A simplified diagram of the photolithography process is shown in Figure 3-20. Selective exposure of the photoresist with UV light through a photomask transfers the pattern from a mask into the photoresist. Two different types of photoresist are used: negative and positive, and they are named for their behavior upon exposure to light. A positive photoresist becomes more soluble after UV exposure, while a negative photoresist becomes less soluble due to the chemical-linking. After dissolving away the

unwanted portion of the resist in the developing chemical, the completed pattern emerges. As shown in Figure 3-20, the same photomask pattern can produce inverted images with the two types of photoresist.

Since photoresists are light-sensitive, they have to be kept in non-transparent or brown bottles to avoid exposure to the light sources. Besides, the room for lithography in IML is equipped with special yellow lights that filter out UV light, allowing for handling and processing of photoresists safely. The detailed photolithography procedure is demonstrated in Figure 3-21 step by step.

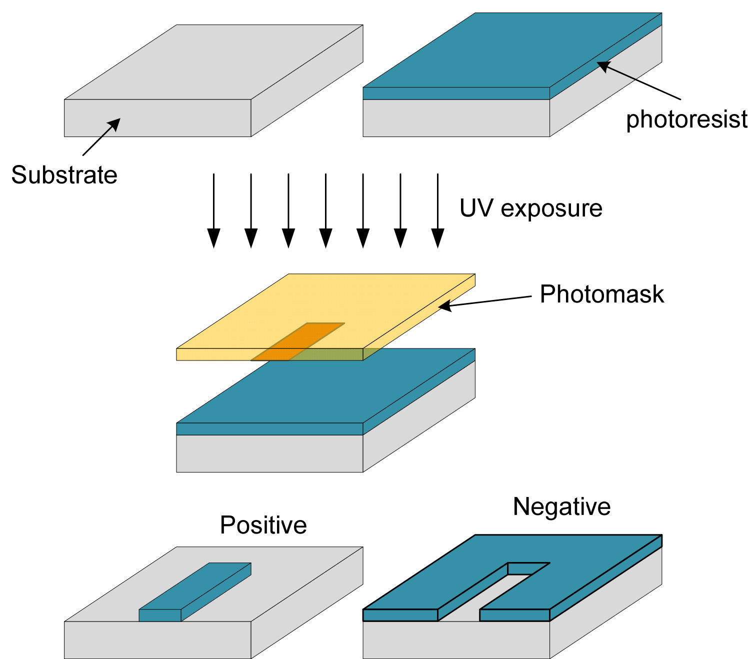


Figure 3-20: Details of lithographic pattern transfer process with positive and negative photoresist

First, before applying the resist, the substrate must be cleaned with BOE (buffered HF solution) to remove a layer of silicon dioxide formed by a wet or dry oxidation process. Then piranha (H_2SO_4 + H_2O_2) is used to remove any trace of contamination such as dust, organic,

ionic and metallic compounds from the surface of the wafer. The surface is further cleaned using oxygen plasma for a few seconds. After this, the wafers are dehydrated at 150 °C in a clean oven for at least 15 minutes to completely remove any moisture which may interfere with the photoresist adhesion. An adhesion promoter, such as hexamethyldisilazane (HMDS), is often used to prime the substrate surface and improve adhesion of the photoresist pattern to the wafer. This step is very important, especially for very fine patterns or for surfaces such as glass, where photoresist adhesion is naturally very poor.

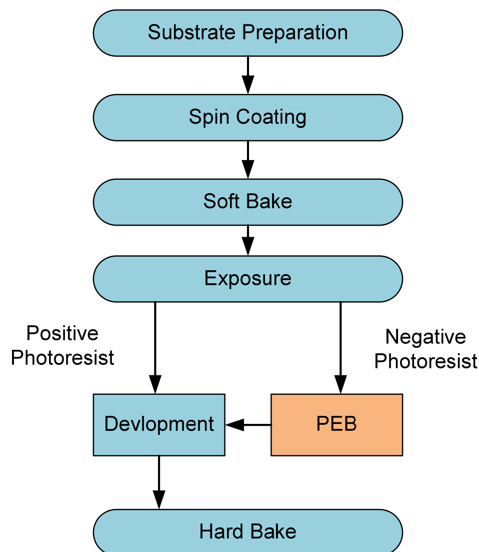


Figure 3-21: Standard procedure of photolithography

Subsequently, the photoresit is applied on the wafer surface using a spin-coating machine. A small puddle of liquid photoresist is poured on the center of the wafer, and the wafer is spun at high speed to spread the photoresist evenly. This spinning process can produce a very uniform coating of photoresist on the wafer surface, where the speed and time of spinning affect the thickness of the film. Then the wafer is heated on a hot plate for a few minutes to evaporate

the resist solvent and to partially solidify the resist. This step is called soft-bake. If soft-bake time is too long, the resist will become more densified and less photo-sensitive. If the time is too short, the wafer will possibly stick on the mask during the UV exposure step.

After soft baking, the photoresist film is ready for UV exposure step. The Karl Suss MA150 contact aligners (Karl Suss, Waterbury, VT) which are calibrated to deliver 10 mW/cm^2 at 365 nm (i line) are used in our IML. The photo masks used are glass with chrome reflective layers, where the chrome has been selectively removed to create the mask pattern. The photomask is placed in contact with the resist-coated wafer and exposed with UV light to transfer the pattern to the resist. The required exposure dose depends upon the type of photoresist and the thickness of the film. For MA 150 aligners, there are four modes: proximity, soft contact, hard contact, and vacuum contact in order of decreasing gap (Figure 3-22). In general, large gaps during exposure tend to result in diffraction and can lead to widening or shrinking of the photoresist features. They can also change the profile of the photoresist features. In comparison, smaller gaps produce higher fidelity pattern transfer. However, overly small gaps may cause defects on the patterns of the wafer. Besides, the diffraction of lithography is also affected by the properties of photoresist, especially the thickness of photoresist. From the discussion above, high-resolution lithography can be achieved by applying small gaps, deep UV light source, and proper resists. Alignment of the mask is critical and must be achieved in for x-y as well as rotationally. Continuous step or single step down to 1 micron for mask and/or microscope adjustmen can be realized by using Joystick control on MA-150 aligners.

After exposure, the wafer with positive photoresist is immersed in a chemical developer which can remove the exposed portion of the resist. This is followed by rinsing with DI water and drying with nitrogen, revealing the completed pattern. For negative photoresist, UV

exposure initiates the cross-linking process, which makes the exposed portions of the resist less soluble in the developer. It is then necessary to post-exposure bake (PEB) the resist to complete these cross-linking reactions between molecules. After PEB, the unexposed portion of resist is removed by dissolution in the developer, and the pattern is transferred from the photomask to the wafer.

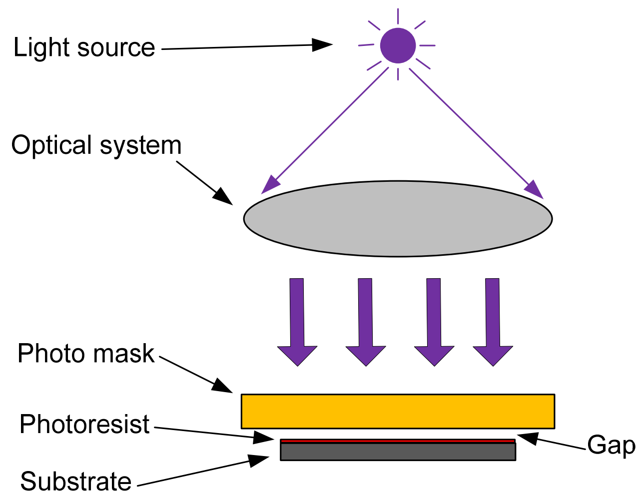


Figure 3-22: Illustration of photolithography.

The final processing step is hard baking, which is used to further promote the adhesion of the resists and increase its thermal and chemical stability. Hard baking is particularly important if the photoresist will be used as an etch mask for the following wet or dry etching processes. The high temperatures used (120°C - 180°C) crosslink the resin polymer in the photoresist, thus making the image more thermally stable. If the temperature used is too high, the resist will flow causing degradation of the image. The temperature at which flow begins is related to the glass transition temperature and is a measure of the thermal stability of the resist. In addition to cross-linking, the postbake can remove residual solvent, water, and gasses and will usually improve

adhesion of the resist to the substrate. Other methods have been proposed to harden a photoresist image. Exposure to high intensity deep-UV (below 300nm) light crosslinks the resin at the surface of the resist and then a tough skin around the pattern is formed. Deep-UV hardened photoresist can withstand temperatures in excess of 200°C without dimensional deformation. Although it is commonly thought that the deep-UV radiation causes the crosslinking reaction directly, there is some evidence to suggest that ozone generated by the interaction of the light with atmospheric oxygen may cause (or enhance) the crosslinking reaction. Plasma treatments and electron beam bombardment have also been shown to effectively harden photoresist.

In this dissertation, several typical types of photoresist are discussed. The positive photoresists includes AZ3330, AZP4620 (AZ Electronic Materials, Somerville, NJ) and (Rohm and Haas Electronic Materials, Philadelphia, PA). The typical negative resist includes SU-8 series (MicroChem Corp., Newton, MA). The properties and specific processing for each of these photoresist applications are described later in this dissertation.

3.5 Evaporation and Lift-off

Electron beam evaporation is a form of physical vapor deposition in which a target anode is bombarded with an electron beam emitted by a charged tungsten filament under high vacuum. As shown in Figure 3-23, the source materials are heated in high vacuum until they are evaporated. Evaporated atoms rise from the source in a cone-shaped vapor cloud and then condense back into a solid state when they encounter a surface. Substrate wavers are typically placed at specific angles so that condensing vapor deposits almost uniformly across their surfaces. To increase film uniformity, a planetary system can also be used that spins the wafers with two degrees of rotation within the evaporant cloud.

There are two primary types of evaporation: thermal and e-beam evaporation. In the thermal evaporation system Joule heating via a refractory metal element melts the metal source. A wide variety of materials can be deposited by evaporation, such as gold, aluminum, chrome, nickel, etc. Advantages of evaporation include its simplicity and low cost to implement. Most metals can be evaporated along with a select number of insulators. Downsides to evaporation relate to the melting of the source materials. At the high temperatures as required, the source is easily contaminated.

As discussed earlier, evaporated films are poor at step coverage. Even with the planetary setup, evaporation cannot form continuous films for aspect ratios (AR=step height/step width) greater than 1. This actually makes it convenient for lift-off process. Lift-off process creates structures of a target material on the surface of a substrate by using a sacrificial material. As shown in Figure 3-24, photoresist serving as a sacrificial layer is defined by photolithography. Then the target material (usually a thin metal layer) is deposited (on the whole surface of the wafer). The metal is evaporated over the whole area of the wafer. The metal over the photoresist is then lifted-off by dissolve the photoresist. After the lift-off, the metal remains only in the regions where it had a direct contact with the substrate. If the metal deposition is a conformal process, the metal will cover horizontal surfaces and sidewalls, forming a continuous film everywhere. "Ears" can be formed after lift-off process. These are made of the metal along the sidewall which will be standing upwards from the surface. Also, it is possible that these ears will fall over on the surface, causing an unwanted shape on the substrate. Evaporation with bad step coverage is a perfect tool for lift-off metals. lift-off is applied in ARROW fabrication, especially in self-aligned pedestal (SAP) ARROW structure and micropore fabrication. The details will be discussed in Chapter 6.

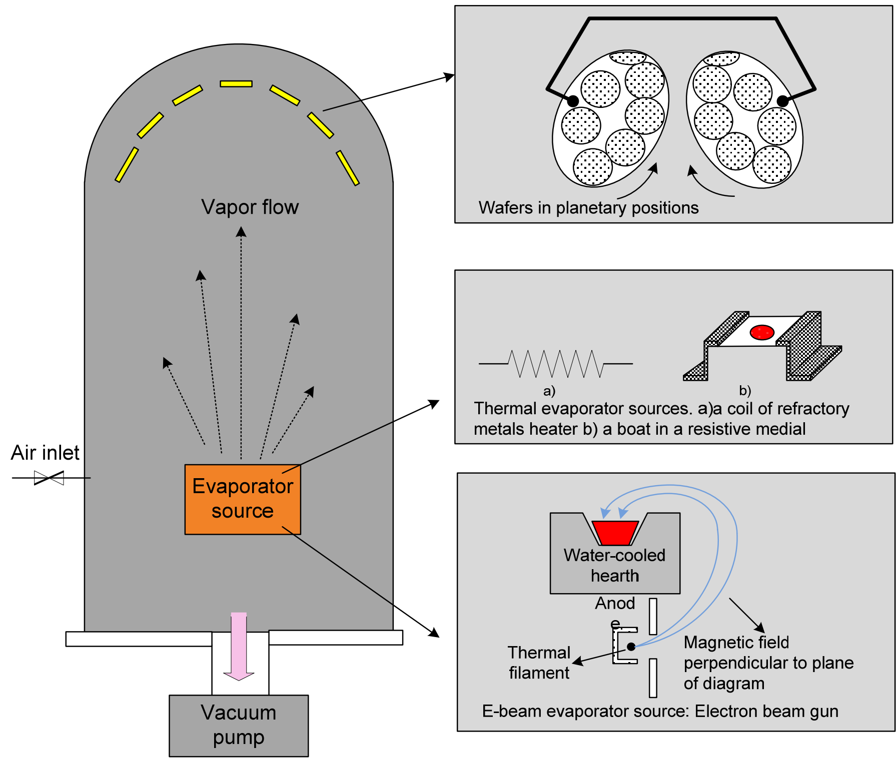


Figure 3-23: Diagram of evaporation system

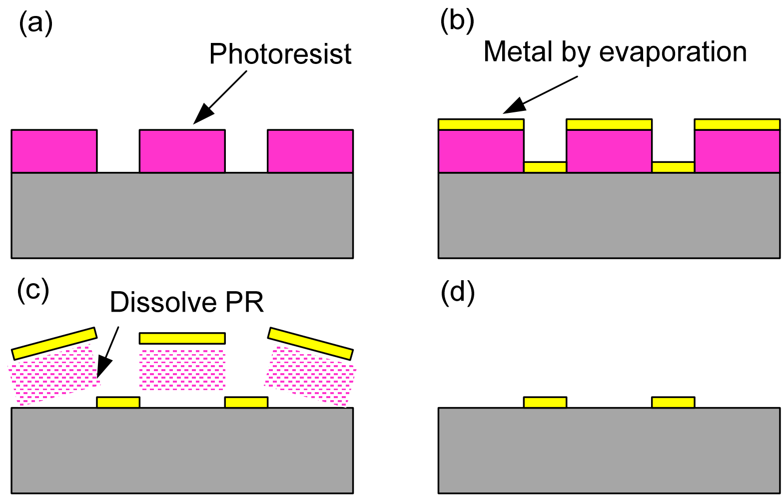


Figure 3-24: Lift-off process

3.6 Etching

3.6.1 Introduction

Etching is often divided into two categories: wet etching and plasma etching. After the lithographic resist patterning step, the subsequent etching of the underlying material is used to complete the pattern transfer process. For wet etching, solid materials react with liquid etchant and then form soluble products which can be rinsed by DI water. Plasma etching makes solid materials react with gaseous etchant and then produce volatile products which can be pumped out from the system.

3.6.2 Wet Etching

Wet etching completely relies on chemical reactions. All the task consists here in finding chemical products or combinations so that the target is etched faster than the mask disappears. Several important factors, including etching rate, etch rate selectivity, etching uniformity, sensitivity to over-time etch, safety and cost of etchants, need to be considered when selecting a proper wet etching process.

Etching rate is dependent on the temperature of etchants. Most of the time, increased temperature provides more energy to molecules to react, and accelerates the etching process. In fact, some reactions need to be done with thermal heating. For example, KOH etching of silicon is generally done at 80°C. Another example of heating use is the process of removing sacrificial core for ARROW fabrication. At room temperature, it is very slow to remove photoresist using any solvent or even acid. The removing process becomes fast and convenient under light heating. This will be discussed in detail in Chapter 5. On the other hand, there are limitations of increasing temperature for practical processes. For example, some solvents (acetone) could ignite and cannot be overly heated.

Selectivity is the ratio of the etch rate for the targeted material to of the etch rate for non-intended materials such as mask layers. The selectivity should be as large as possible. For the KOH example, the highest selectivity is achieved for particular concentration and temperature. For ARROW fabrication process, the cladding materials for ARROWs are selected to ensure they have high selectivity compared with sacrificial core in the etchant.

Geometry can also affect the etching rate at a local level. Large areas are always etched slightly faster than very small patterns because the former one can have more zones exposed to etchants.

Wet chemical etching methods can result in varying degrees of smoothness of surfaces and defects. As shown in Figure 3-25, byproducts could be left on the surfaces of devices after chemical etching. The smoothness is important for many devices, including ARROW waveguides because it can affect its optical performance severely. So it is very important to choose right methods for wet etching process. After chemical reaction, correspondent cleaning steps should be developed to remove possible byproducts or residues on the surfaces.

According to the etching profiles, the etching process can be classified to isotropic etching and anisotropic etching. Because the etch profile is rounded (Figure 3-26(a)), isotropic etching cannot be used to make fine features. Undercut is similar to vertical etched depth. Most wet etchants result in an isotropic profile. The advantage of isotropic wet etching is that the process is inexpensive, simple and fast. If the profiles are not considered, isotropic etching is the best way to removing the layers unwanted. For example, BHF (buffered HF) is applied to etch the SiO_2:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \; . \qquad (3\text{-}5)$$

The etching rate of PECVD SiO_2 is about 300nm/min at room temperature.

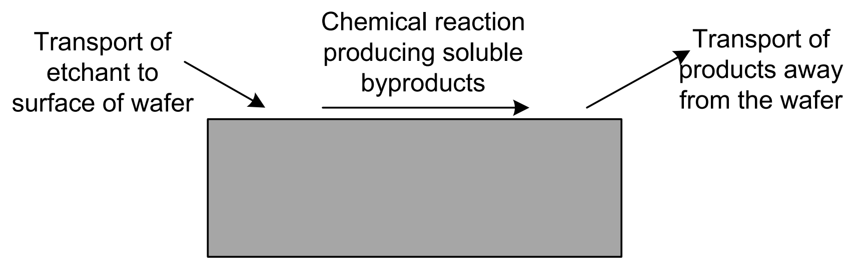


Figure 3-25: Demonstration of wet etching process

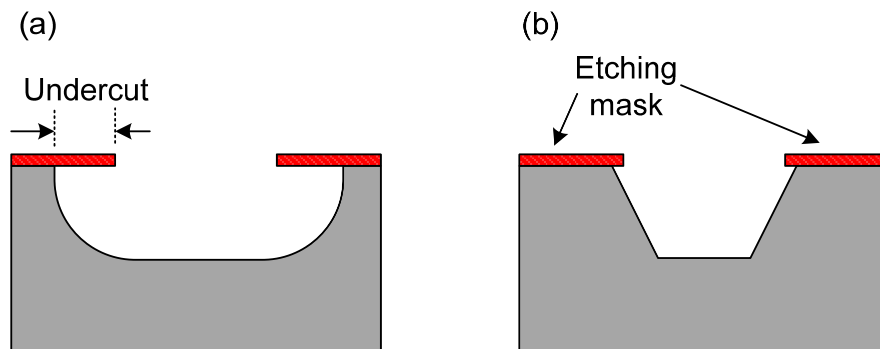


Figure 3-26: Profiles of wet etching (a) isotropic etching, (b) anisotropic etching

The etching of silicon in KOH is a typical example of anisotropic etching. The unique etching profiles are made possible because in the silicon crystal lattice, the (111)-plane has more available bonds per unit area than the (110)- and (100)-planes; therefore the etch rate is slower for the (111) plane. In respect to (100)-plane, the etching is at an angle of 54.7 ° as shown in Figure 3-27(a). If the window of the mask is large enough or the etch time is short, a U-shaped groove will be formed.

As discussed in Chapter 2, creating ARROWs on pedestals allows for more desirable waveguide geometries and lower propagation losses. One type of ARROW waveguide-single

over coating (SOC) ARROWs was created by wet etching a pedestal of 5 μm into silicon underneath the core and bottom antiresonant layers (Figure 3-27(b)).

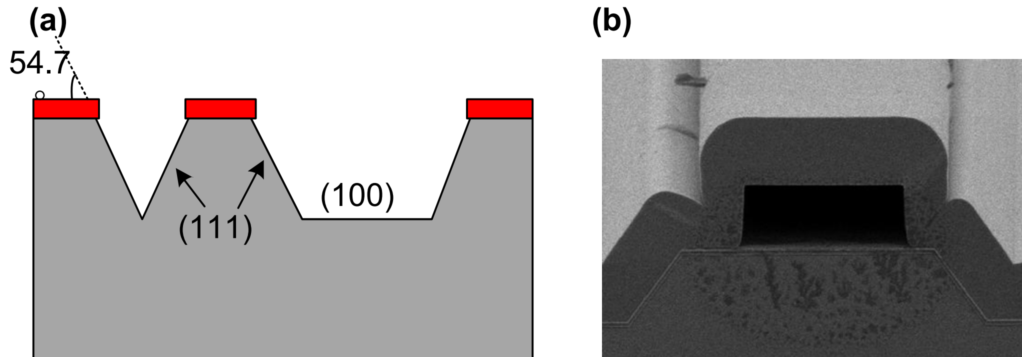


Figure 3-27: (a) KOH etching of silicon and (b) SEM picture of a SOC ARROWs with a pedestal etched by KOH

3.6.3 Oxygen Plasma Etching

Similar to PECVD and Denton sputterer, the Planar Etch II (PE2) machine also employs capacitively coupled plasma (CCP) as plasma source. As shown in Figure 3-28(a), the wafer is placed on an electrode connected to the ground and the other electrode is connected to RF power. With this configuration, ion-bombardments on the wafer can be at all directions. The ionization of the oxygen is done by RF excitation emitted by the top electrode. The pressure inside the chamber ranges from a few mTorr to a few hundreds of mTorr. The oscillating electric field of the RF signal provides the ionizing energy necessary for reactions (3-6) and (3-7) described below. In plasma etching, neutral oxygen radicals are formed as the products of two reactions [80] below. This etching system is actually another chemical etching method. It uses O_2 to ash organic contaminants.

$$O_2 + O^+ \rightarrow O_2^+ + O\ , \qquad (3\text{-}6)$$

$$O_2^+ + e^- \rightarrow O + O\ . \qquad (3\text{-}7)$$

Organic contaminants, for example photoresist, consist of carbon, hydrogen and oxygen. Exposure to oxygen atoms eventually removes them as volatiles. The products of ashing are CO_x and H_2O vapor which are volatile and can be pumped away by the vacuum system. In the process of photolithography, the developer solution can remove most unwanted parts except some tiny corners. PE2 is a perfect tool to discum the surface to remove the resist residue. During the stripping process in our IML, the oxygen flow rate of PE2 is around 100 sccm and the power always ranges from 0 to 250w. Low power and relative high pressure lead to isotropic features and lateral undercuts (Figure 3-28(b)).

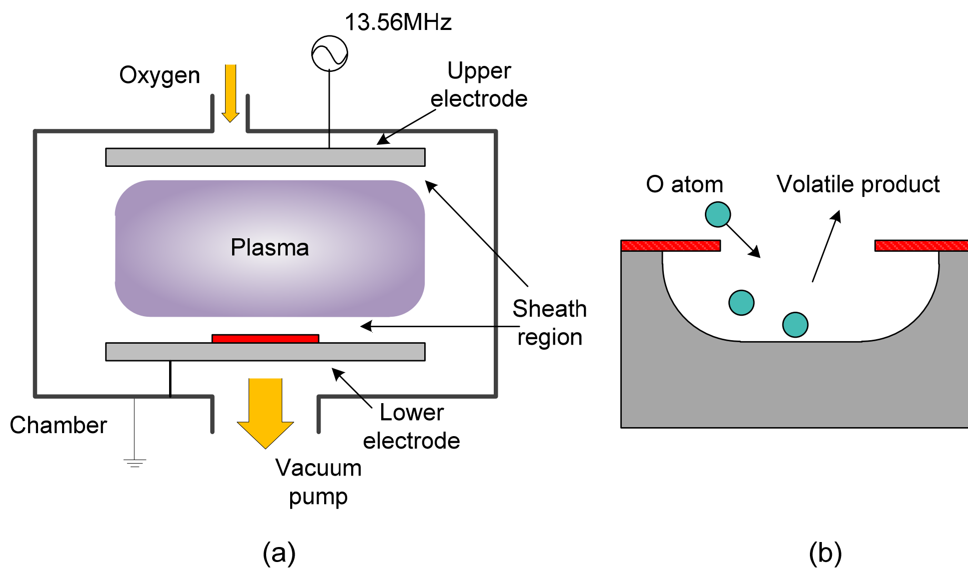


Figure 3-28: (a) Diagram of PEII and (b) oxygen chemical etching in a plasma

3.6.4 Reactive Ion Etching (Anelva RIE)

In our IML, Anelva reactive ion etcher (RIE) (Anelva Corporation) is always used to anisotropically and selectively etch SiN and SiO_2. The setup of the Anelva RIE tool in the IML is shown in Figure 3-29 (a). The wafer is connected to the RF signal instead of the ground in PE

case. A large upper electrode (grounded, including chamber wall) creates a bias potential across a big area where ions are accelerated to the substrate to achieve directional ion bombardment and anisotropic etching. In RIE process, reactant gases are introduced and excited into plasma using an RF voltage at 13.56 MHz. The sheath region produces accelerated ions toward the wafer, leading to the physical ion sputtering given the high ions velocity. The layer molecules are stripped away by the impact from the ions on the wafer. Physical etching is characterized, by a very low selectivity, but is highly anisotropic. In addition, proper process gases in the RIE system are selected so that the ion radicals chemically react with the etch surface without reacting significantly with an etch mask. Basically, the etching in RIE involves two major parts: physical ion bombardment and chemical ion etching (Figure 3-29(b)). RIE offers the possibility to set up anisotropic etching recipes. This depends on the type of material to etch. If it has a poor capacity to absorb electrons and polarize, RIE produces the same effects as PE does (not much difference). Dielectric materials have a poor electron adsorption capacity, semiconductors a higher one.

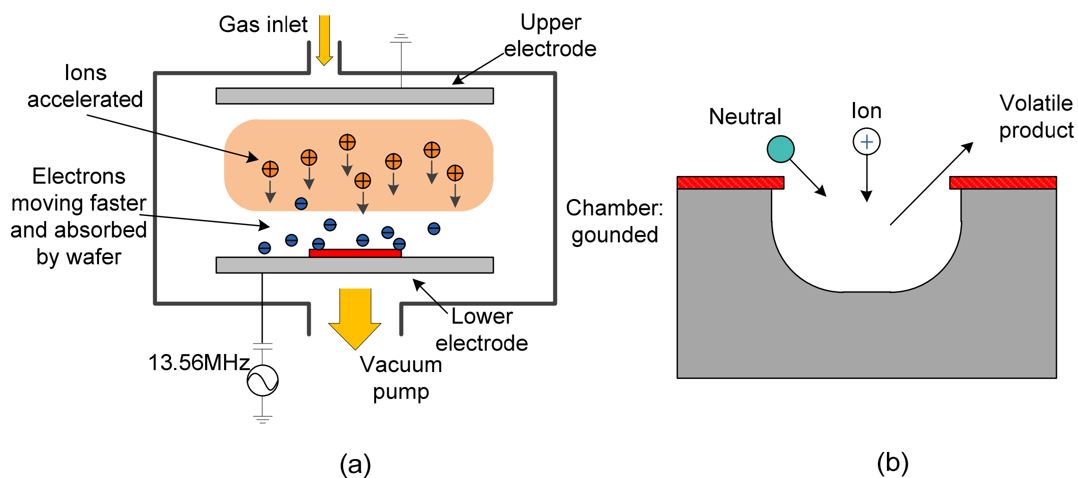
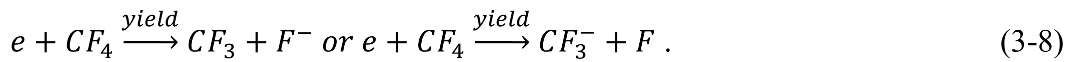


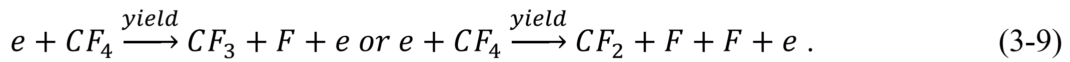
Figure 3-29: (a) Diagram of Anelva RIE system and (b) etching profile from RIE (chemical etching and ion bombardment)

For ARROW farbricatoin, solid-core waveguides are formed by dry etching the ridges into the topmost thick SiO_2 layer as described in Figure 3-1(d). Solid-core waveguides are very important to complete an ARROW platform because they allow for coupling light between optical fibers at the edge of the chip and the hollow waveguide. In addition, intersecting ridge waveguides are used to couple the excitation light and collect the fluorescence signals.

CF_4 is a typically used for SiO_2 etching. The plasma turns stable, unreactive gas (CF_4) into highly reactive radicals (CF_3, CF_2, F, etc.) through dissociation process (Equation (3-8) and (3-9) and (3-10)). The reaction between CF_x radicals and SiO_2 produces SiF_4 and CO_2 as etching products (Equation (3-11)). At surfaces other than SiO_2, CF_x radicals serve as polymer precursors which will lead to polymerization. This is desirable for ridge etching because photoresist rather than metals is applied as the etching mask since photoresist can protect the sidewalls and corners better than metals do for a 5μm-tall structure. The polymerizing determines the selectivity between SiO_2 and photoresist. However, a high negative DC bias increases the etching behavior over polymerization tendency. This effect is caused by the enhanced energy of the ions striking the surface, resulting in polymer sputtering.



$$e + CF_4 \xrightarrow{yield} CF_3 + F^- \ or \ e + CF_4 \xrightarrow{yield} CF_3^- + F \ . \quad (3\text{-}8)$$



$$e + CF_4 \xrightarrow{yield} CF_3 + F + e \ or \ e + CF_4 \xrightarrow{yield} CF_2 + F + F + e \ . \quad (3\text{-}9)$$

$$e + CF_4 \xrightarrow{yield} CF_3^+ + F + e + e \ . \quad (3\text{-}10)$$

$$CF_x + SiO_2 \xrightarrow{yield} SiF_x + CO_x \ . \quad (3\text{-}11)$$

As described earlier, the height of hollow waveguide is about 5 μm. Simulations have shown that coupling efficiency between the solid and hollow waveguides is maximized when the ridge etch depth is half of the thickness of the top SiO_2 layer [62]. So an etching mask has to be coated thick enough to protect the rest parts of ARROw chip. SU8-10 is spun on the devices to

pattern the solid-core waveguides (See Appendix B.2. In the following, the ridge can be etched by the Anelva RIE or the Trion ICP/RIE. The Anelva etching recipe is listed in Table 3-5. It has been noted that the SU8 has to be cured well, otherwise etch rates may change. Figure 3-30 shows SEM pictures of completed solid core waveguides of ARROW chips.

Table 3-5: Etching Recipe in Anelva for Ridge Waveguide (SiO_2)

Pessure (mTorr)	*RIE (w)*	*CF4 (sccm)*	*Etching rate (nm/s)*	*Uniformity (%)*	*Selectivity ($SU8:SiO_2$)*
100	300	25	2.05	20~30	2.116

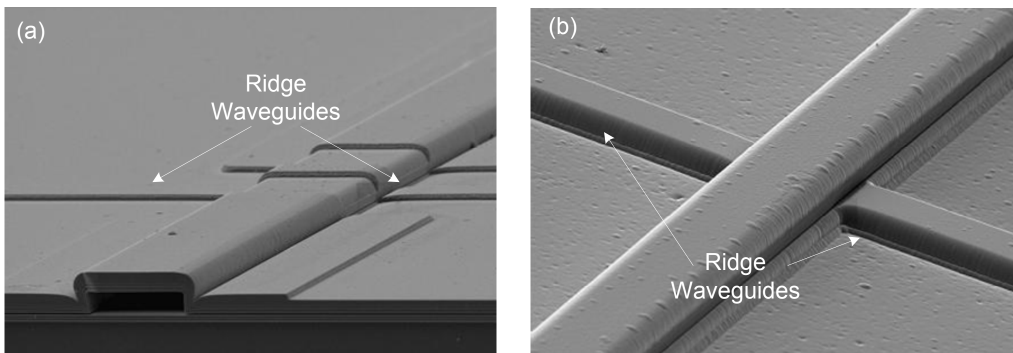


Figure 3-30: SEM pictures of ridge waveguides on ARROW chips

3.6.5 ICP RIE (Trion Minilock Phantom III)

Different from Anelva RIE, the Trion Minilock Phantom III ICP/RIE tool has two sources for plasma excitation. Figure 3-31 illustrates the structure for the Trion etcher. In addition to a Reactive Ion Etching (RIE) RF generator, the Trion uses an Inductively Coupled Plasma (ICP) RF generator to produce a high-density plasma with a magnetic field. These two sources can create high-density, low pressure, low-energy plasma by coupling ion-producing

electrons to the magnetic field arising from the RF voltage. The plasma is shielded from the electric field of the RF to avoid capacitive coupling, which tends to create high energy ions.

Figure 3-32 demonstrates how ICP is created. Solenoid coils connected to the ICP RF generator are around the outer walls of ceramic tube. According to the Ampère's Law, RF current (I_{rf}) in the coils generates a changing magnetic field ($B_z(t)$), which can penetrate through the ceramic walls. A time varying E-field ($E(t)$) is then produced inside the vacuum chamber, wrapping around the axis of the solenoid coils. Electrons, which gain the energy from this electric field, are capable of ionization (hot electrons). Collisions between hot electrons and neutrals create high-density ions (~100CCP), therefore maintaining the plasma. Since plasma has a relatively high electrical conductivity, it can be regarded as a conductor. It is known that AC current flows mainly at the "skin" of a conductor due to the opposing eddy currents within the conductor. Therefore the energy transferred from RF source to plasma is dissipated via Joule heating (Ohm's Law) within the skin depth (δ) as Figure 3-32(c) illustrates. At high frequencies, δ gets smaller due to the increasing eddy current. Once high-density ions are created, the RIE power serves to create a negative DC potential on the lower electrode, accelerating ions across the sheath region and bombard on the substrate surfaces. In comparison, ICP obtains energy from the varying electromagnetic fields, while CCP gains energy from the electric field across the sheath region. As a result, unlike CCP, ICP can produce high density ion flux, which is not limited by the Paschen's Law. In other words, ICP can be used for etching at low pressure (~mTorr). This is beneficial for anisotropic deep etching because high-density ion flux can be highly directional without many collisions.

The advantage of the ICP/RIE system is that two RF generators provide separate control over ion density and ion energy, providing flexible recipes for various etching requirements

(isotropic and anisotropic). Without ICP power, the ICP/RIE system (Trion) can also serve as a RIE system. Unlike the Anelva RIE etching, Trion etching does not require a high DC bias to reach high etching rates. This is beneficial for decreasing the damage on the etching surfaces and increasing the selectivity between the target and mask materials.

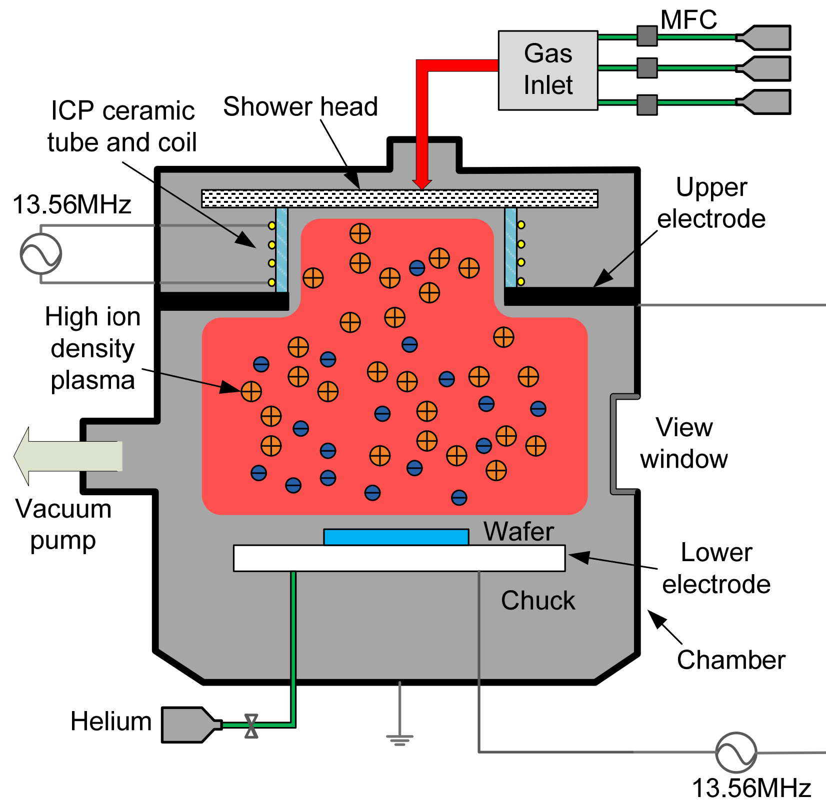


Figure 3-31: Diagram of Trion ICP RIE

The Trion ICP RIE is also used to etch ridge waveguides. The etching recipe and experimental results are shown in Table 3-6 and Figure 3-33. In comparison to an RIE only etch, the etching rate and the selectivity are increased using Trion. Figure 3-34 shows cross-sectional SEM images of ridge waveguides etched using Anelva RIE and Trion ICP/RIE. We can see from

the pictures that ridge waveguides fabricated by the Trion have more anisotropic etching profiles than those fabricated by the Anelva RIE system. Loss measurements prove that the loss numbers for the two different profiles are very close, indicating that the loss is dominated by the waveguide material rather than the etch profile. Compared with Anelva RIE, the Trion ICP/RIE is preferred to etching ridges because of its higher etch rates, more precise pattern transfer, and higher etching uniformity across a wafer.

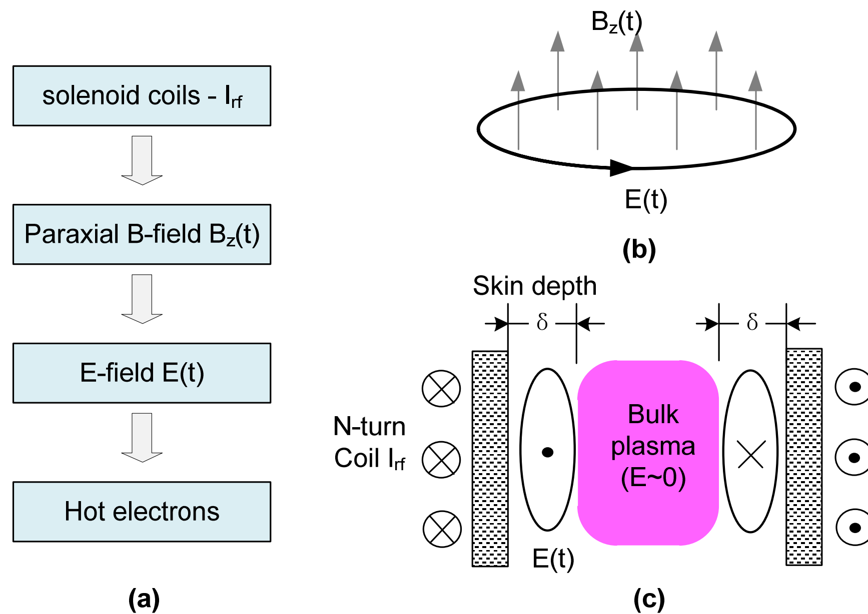


Figure 3-32: Demonstration for Inductively coupled plasma

Table 3-6: Etching Recipes for Ridge Waveguides Used with ARROW Devices

Pressure (mTorr)	*ICP Power (w)*	*RIE Power (w)*	*Gas (CF4) (sccm)*	*Etching Rate (nm/s)*	*Uniformity (%)*	*Selectivity (SU8 10:SiO2)*
12	550	75	50	5.1	~6%	1.2

In addition, Trion ICP RIE can be used for fabrication of self-aligned pedestal (SAP) ARROW waveguides. ARROWs on a wet-etched pedestal have been described in Figure

3-27(b). It was found that the alignment between the core and pedestal is critical for ARROWs fabrication. Any misalignment will lead to the optical loss for the waveguides. The Trion ICP RIE was investigated to dry etch a pedestal using the core as a mask which avoided the alignment step between the core and pedestal. The anisotropic etching for SAP structure will be discussed in Chapter 6 in detail.

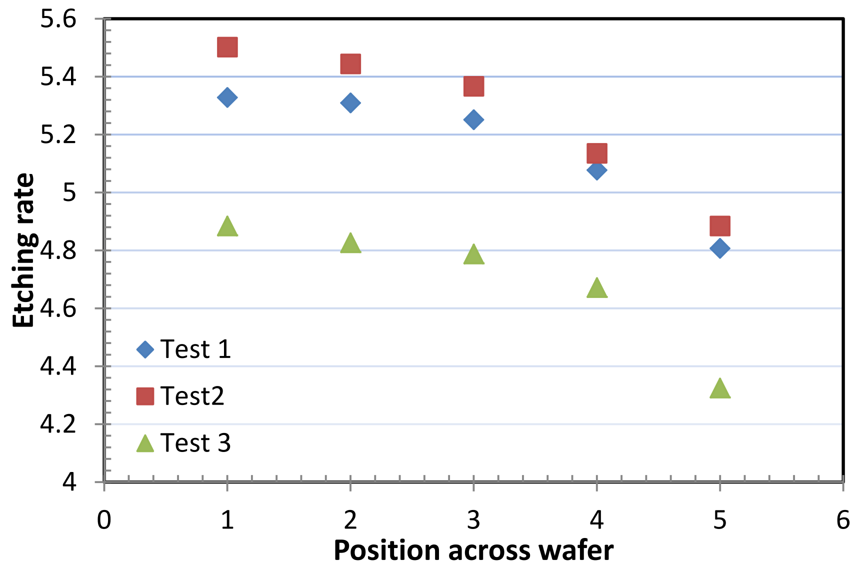


Figure 3-33: Measurement for etching rate of PECVD SiO_2 with Trion ridge etch recipe (see Table 3-6) at different locations

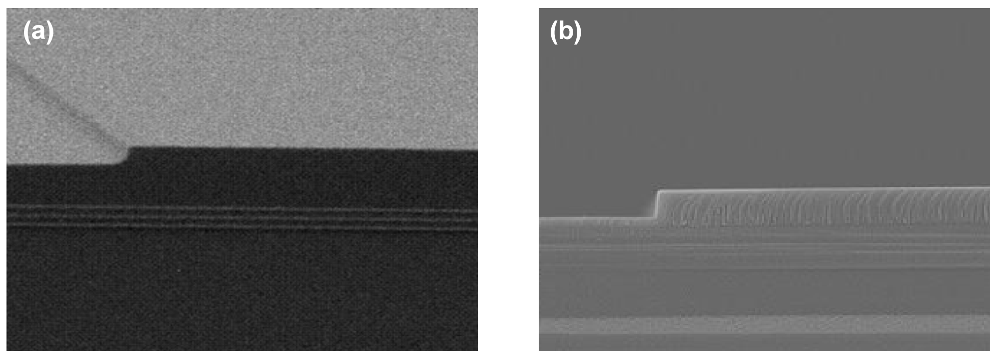


Figure 3-34: SEM pictures of cross section of ridge waveguide (a) Anelva RIE - more isotropic, (b) Trion ICP RIE - anisotropic

3.7 Materials for ARROWs Fabrication

The cladding materials have to meet several criteria for ARROW waveguides. Firstly, the claddings should have relative high refractive index compared with liquid inside the core. Secondly, the thin films can be deposited using inexpensive standard microfabrication process, such as CVD, sputtering, and sol-gel methods. In addition, the materials should have low absorption in a large range to ensure the low-loss propagation within the hollow core. The typical fabrication process has been demonstrated earlier. The antiresonant layers are required to build a robust structure and should be able to withstand the wet etching process in the acid or solvents. As discussed in Chapter 2, hollow ARROW waveguides are particularly useful for optofluidic sensor, including very sensitive fluorescence detection of biological particles in aqueous solutions [19, 81-83]. To improve the ARROW biosensor's sensitivity, the material noise has to be reduced.

3.7.1 Photoluminescence

Photoluminescence (PL) is a process in which a substance absorbs photons (electromagnetic radiation) and then re-radiates photons. Quantum mechanically, this can be described as an excitation to a higher energy state and then a return to a lower energy state accompanied by the emission of a photon. For the ARROW platform, the waveguide material can absorb photons from excitation beam and then generate PL in the same wavelength range as analyte fluorescence. The PL in this range cannot be filtered by emission filter and can be collected by the detector system, limiting to the limiting the signal-to-noise rato (SNR) of ARROW biosensor platforms.

To improve the ARROW platform's sensitivity, the background noise results from the materials has to be reduced. In this dissertation, SiN, SiO_2 and Ta_2O_5 have been investigated as

the claddings of ARROW waveguides. To characterize the PL of thin films, a HeNe laser (l=632.817 nm) was used for normal excitation of the samples, and an objective (50x, 0.5 NA) was used to couple light into a LabRAM HR spectrometer (Horiba Jobin Yvon) to collect the emitted spectral data. PL intensity was measured for a bare silicon wafer and 150 nm-thick SiN, SiO_2 and Ta_2O_5 layers on silicon substrates. After data collection, the PL contribution from the silicon was subtracted from the data for the SiN, Ta_2O_5, and SiO_2 layers. As Figure 3-35 shows, the PL of PECVD SiN is much higher than that of SiO_2 and Ta_2O_5 (Room temperature, 100˚C, 200˚C, 300˚C) in the measured wavelength span for layers of equal thicknesses. It has been reported that the PL of SiN film is dominated by confined exactions within Si quantum dots embedded in SiN films and defects in the amorphous silicon nitride films [84]. Since high index nitride films have more silicon than low index films [77], it is likely that the PL centers in the film are increased by greater relative numbers of silicon atoms. In previous researches, SiN and SiO2 were used to make ARROW waveguides and SiN film is the main source contributing to the background noise for ARROW platforms. Replacing SiN with Ta_2O_5 can potentially reduce the noise significantly.

Different from SiN films, the light emissions in this range originate from the oxygen-defect level of the TaO_x films [85]. Usually, as-deposited films consist of fully oxidized Ta_2O_5 and TaO_x ($x<2.5$) suboxides. The existence of TaO_x leads to the oxygen deficiency in the films [86-89]. Specifically, the first and second ionization energies of the O-vacancy double donor are 1.2 eV and 2.1–2.7 eV below the conduction band, respectively. For the ARROW waveguides application, the wavelength of pump light is usually 633nm (1.88eV>1.2eV) and therefore it likely causes the light emission during the oxygen ionization process. In our Denton sputtering system, Ar gas is introduced as working gas and a Ta_2O_5 target in 99.999% purity is applied.

This can form TaO films with relatively lower PL than that of SiN films. Strictly speaking, a small amount of TaO_x still exists in the film. The method for further suppressing the PL intensity of TaO films will be discussed in Chapter 6.

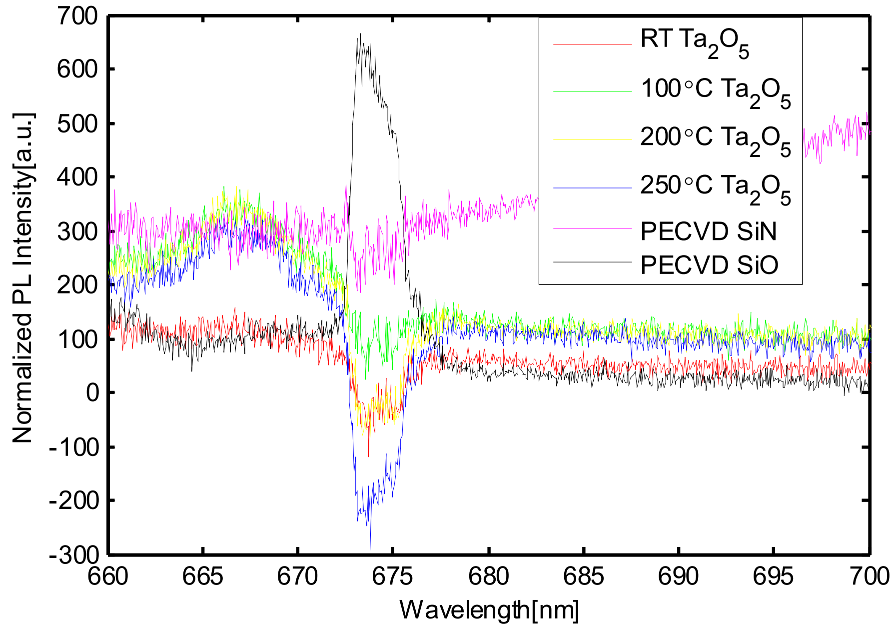


Figure 3-35: Photoluminescence of 150nm-thick SiO_2, SiN and Ta_2O_5 films on silicon substrates

The HGT hybrid glass has also been investigated to make the cladding layers for ARROW waveguides. In Figure 3-36, the photoluminescence of hybrid glass is very close to that of deposited SiO_2. This makes it a potential replacement for topmost thick SiO_2 of the ARROW structure. HGT is attractive because it can be deposited using spin-on method which is convenient and time-saving. The detailed fabrication method will be described in Chapter 5. However, HGT cannot stand etching in acid and the planarization of the film over the waveguide leads to higher loss.

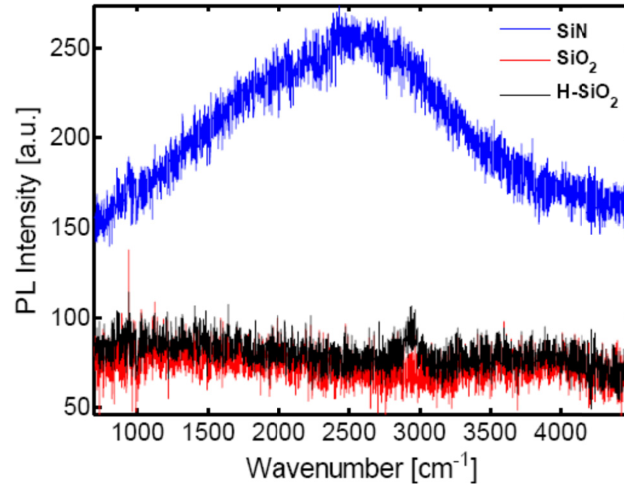


Figure 3-36: The photoluminescence of PECVD SiN and SiO, and hybrid glass

3.7.2 Stress

The stress of thin films consists of extrinsic stresses and intrinsic stresses. Extrinsic stress (σ_1) is caused by thermal expansion mismatch between the film and substrate while intrinsic stress (σ_2) is dependent on the film microstructure and the deposition process.

Extrinsic stresses can be estimated from thermal expansion coefficient differences:

$$\sigma_1 = E_f(\alpha_f - \alpha_s) \times \Delta T/(1 - \nu), \qquad (3\text{-}12)$$

where ΔT stands for the difference between deposition and measurement temperature. E_f and ν are Young's modulus and Poisson ratio, respectively. α_f and αs account for the thermal expansion coefficients for thin film and substrate (usually silicon), respectively. Intrinsic stresses are caused by a variety of mechanisms that are not fully understood.

Films deposited by sputtering or PECVD can be under tensile or compressive stress. Stress in thin films causes wafer curvature shown in Figure 3-37. The stress relies on many factors, such as RF power, reactant gases, working pressure, substrate temperature, etc. The stress of 150nm-thick films grown by sputtering and PECVD under different temperature is

measured using a Flexus 2320 Dual Wave Length Thin Film Stress System (KLA – Tencor Corporation). The results are listed in Table 3-7. The results indicate that higher deposition temperature leads to less compressive stress for sputtered films. Compared with the stress of SiN film grown by PECVD (~22.5Mpa, T=250°C), the stress of sputtered Ta_2O_5 or SiN film is approximately 6~15 times higher. This fact explains why sputtered ARROWs have a weaker structure than PECVD ARROWs. Even though the films deposited under room temperature show the lowest PL intensity (Figure 3-35), high temperature films are preferred from the fabrication standpoint for hollow ARROW waveguides since they can build a much more robust structure. This will be described in Chapter 5 and Chapter 6.

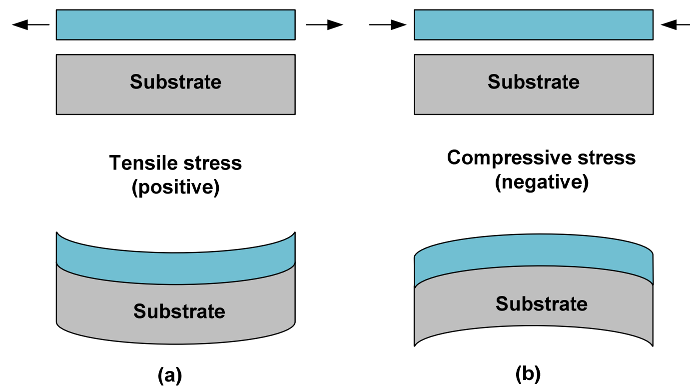


Figure 3-37: Thin-film stress (a) tensile stress (positive) and (b) compressive stress (negative)

Table 3-7: Film Stress of Sputtered and PECVD Films

	Name	*Deposition Temperature (˚C)*		
		25	*90*	*250*
Stress (MPa)	Sputtered Ta_2O_5	-317.23	-208.246	-128.714
	Sputtered SiN	-227.633		-124.553
	Sputtered SiO	-104.594		-124.984
	PECVD SiO			-188.41
	PECVD SiN			22.5341

4 OPTIMIZATION OF INTERFACE TRANSMISSION BETWEEN INTEGRATED SOLID CORE AND OPTOFLUIDIC WAVEGUIDES

4.1 Introduction

As discussed in Chapter 2, it is critical to maximize optical throughput from chip edge to chip edge on an ARROW platform (Figure 2-13) in order to achieve high-efficiency sensing and fluorescence analysis with sensitivities down to the single molecule level. For an ARROW chip, the main sources for on-chip optical loss include the propagation loss in the solid and hollow core waveguides, input and output coupling efficiencies, and interface transmission between solid and hollow core waveguides. In this chapter, the interface transmission loss of ARROW platform was studied. Simulations and experimental measurements were made, based on an established ARROW design and basic fabrication process.

4.2 Throughput of the ARROW Platform

The overall optical throughput T from edge to edge on an ARROW chip can be described by Figure 4-1 and Equation (4-1)

$$T = \kappa_{e1} \cdot e^{-\alpha_s l_s} \cdot \kappa_i^{\,2} \cdot e^{-\alpha_h l_h} \cdot \kappa_{e2} \quad . \tag{4-1}$$

The input coupling efficiency κ_{e1} and output efficiency κ_{e2} contribute to loss at the edges of the ARROW chip. Good-quality facets on the two ends of ARROW chips and optical fibers can help to enhance κ_{e1} and κ_{e2} ($\kappa_{e1} \times \kappa_{e2} \approx 0.55$). The propagation loss of solid and hollow core waveguides are accounted for using loss coefficients and propagation lengths (α_s, l_s, α_h, and l_h).

The loss in different sections of ARROW chips is primarily caused by material absorption and scattering. For a typical rectangular-core water-filled waveguide designed for 633nm, α_h is measured to be around 2-5 cm^{-1} [62] for a core cross section of 12μm × 5μm.

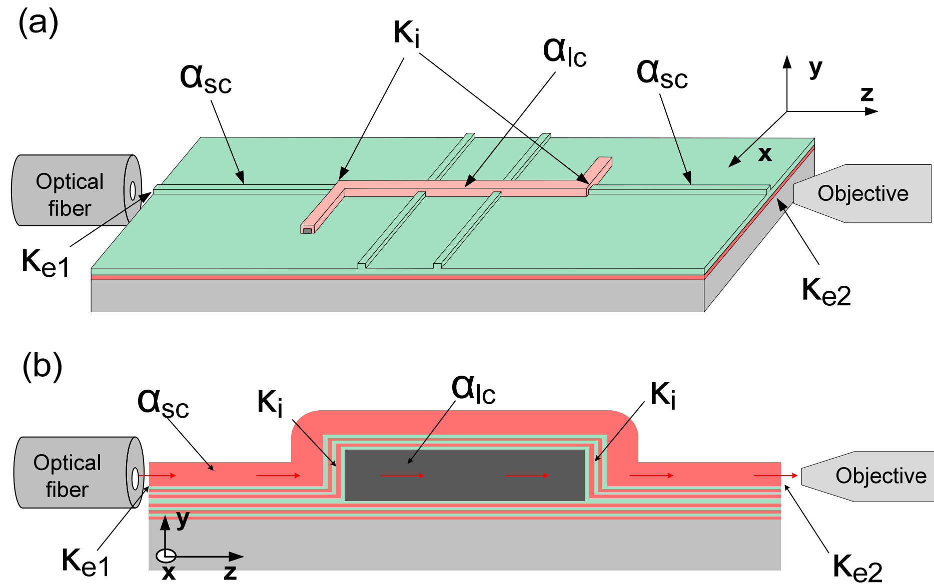


Figure 4-1: Sources of optical loss for liquid core ARROW platform (a) 3D view, (b) sideview

Interface coupling efficiency κ_i between solid and hollow core waveguides is also a significant source of optical loss. κ_i is influenced by the mode mismatch at the solid-to-liquid core interfaces. In the x direction, mode-matching is largely limited by the alignment tolerance of lithography (~1μm) used to form the ridge that defines the solid core waveguide. In the y direction, the mode center in the solid core cannot align perfectly with that in the hollow core because of two factors. First, as shown in Figure 4-1(b), the additional top ARROW layers under the solid core contribute to the mode mismatch by elevating the midpoint of the top solid core mode compared to the hollow core mode. SOC (single over coating) structures [90] were

previously employed to improve this vertical mismatch by not introducing additional ARROW layers in the solid core (Figure 4-2). But SOC structures showed higher loss (at least 3.4 cm^{-1}) because only one top layer was used to confine the light. A second important reason for vertical mode mismatch is the film profile that results during the deposition of the topmost cladding layer. Most thin-film deposition methods will be affected by feature shadowing and result in different coating rates on sidewalls versus horizontal surfaces. The ARROW chips are fabricated with plasma enhanced chemical vapor deposition (PECVD), and as shown in Figure 3-19, crevices are formed at the interface between solid and hollow waveguides. Although the conformality of films can be improved by adjusting the deposition conditions, crevices cannot be completely eliminated which will introduce more transmission loss at the interfaces.

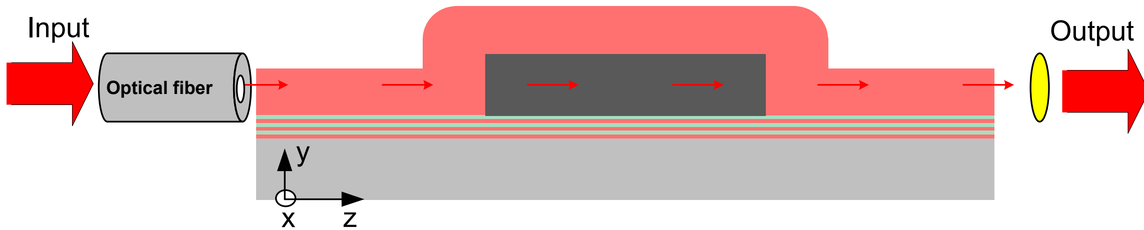


Figure 4-2: Side view of SOC ARROW platform

4.3 Fabrication

In order to look into the effects of interface crevices on κ_i, four ARROW devices were grown with different top cladding thicknesses, but with otherwise identical fabrication processes as illustrated in Figure 3-1. Three periods of alternating bottom cladding layers were first deposited on the silicon substrate by PECVD. SU-8, a negative photoresist, was then used to

form a sacrificial rectangular core. Another three pairs of alternating top layers were grown on top of the SU8 and a hollow core was finally formed by wet etching the SU8.

The hollow core dimensions for the four devices were 12×5μm^2. The cladding layers used were SiO_2 and SiN (silicon nitride) with the following order and thicknesses (hollow waveguide): SiO_2/SiN/SiO_2/ SiN/SiO_2/ SiN-core- SiN/SiO_2/ SiN/SiO_2/ SiN/SiO_2 (270/93/270/93/270/93-5000-127/285/142/300/123/d_{to}). The thicknesses of the top SiO_2 layer away from the surface and at the crevice are represented by d_{tO} and d_{cr} respectively. Using a Focused Ion Beam (FIB) system, waveguides were ion-milled precisely at the solid-to-hollow core interfaces. The SEM images of the samples were shown in Figure 4-3 and the parameters were then measured and listed in Table 4-1.

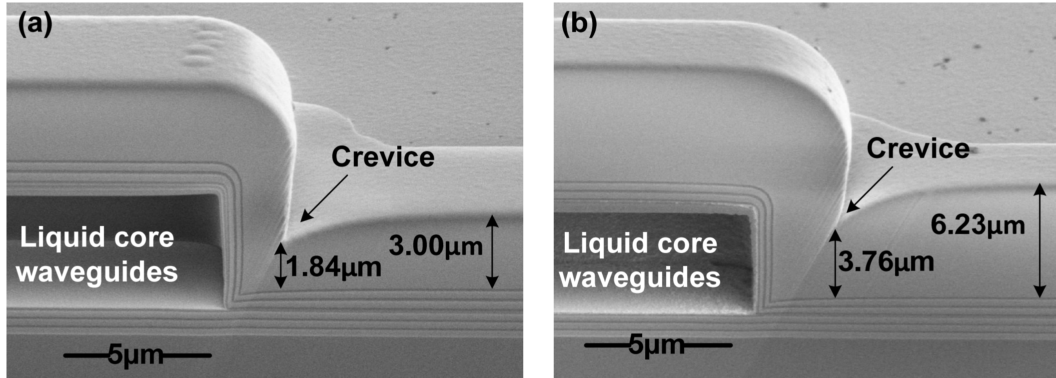


Figure 4-3 SEM image at interface between solid core and liquid core ARROW waveguides (a) 3.00μm thick top SiO_2, (b) 6.23μm thick top SiO_2

Table 4-1: The Measured Parameters of ARROW Samples

Sample #	*1*	*2*	*3*	*4*
d_{to} (μm)	3.00	4.27	5.03	6.23
d_{cr} (μm)	1.84	2.70	3.14	3.76

4.4 Simulation Results

A simulation was performed using FIMMPROP (Photon Design) and two simulation scenarios were explained in Figure 4-4. In the first, the top layer film was assumed to be perfectly conformal ($d_{to} = d_{cr}$; no crevice formation). In this case, high coupling efficiency over a wide d_{to} range with a maximum around d_{to}=4.5μm is predicted. The transmission efficiency begins to drop when the mode center in the solid cores is located significantly above that in the liquid cores. For the second set of simulations, the data in Table 4-1 was used to model a real shape for the interfaces. The optimum thickness shifted to d_{to}~7μm when actual crevices were taken into consideration. From the energy propagation simulations in Figure 4-5 (a-b), we can see that more scattering and loss take place at the interface when the top SiO_2 is thinner while there was better mode alignment at the interfaces in the vertical direction when the top SiO_2 is thicker.

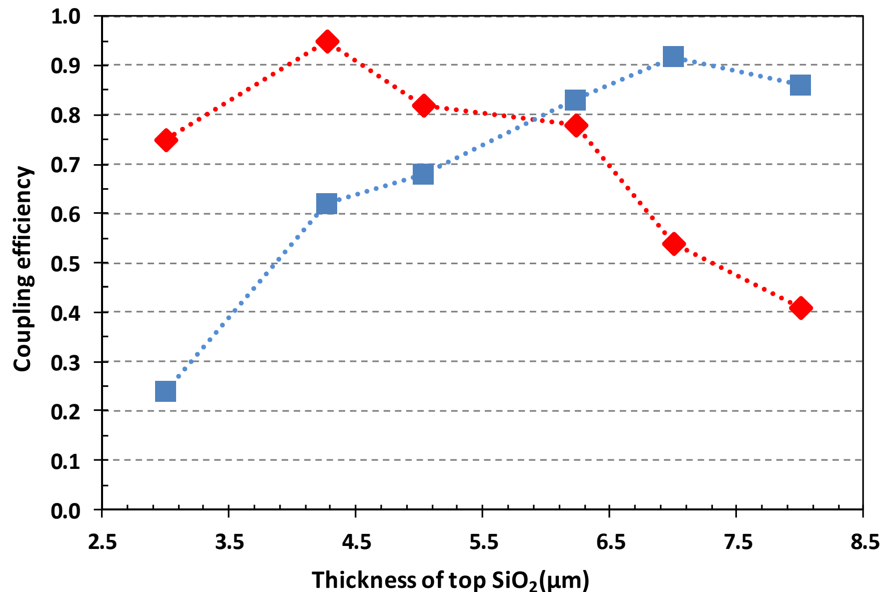


Figure 4-4: Simulation results under ideal conditions (diamonds), simulation results taking crevice into account (squares).

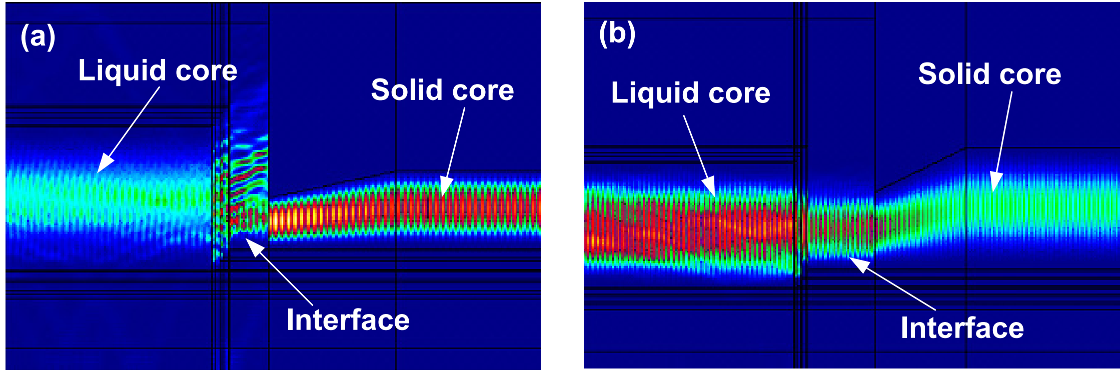


Figure 4-5: Energy propagation across interface simulated by FIMMPROP (a) 3.00µm thick top SiO_2, (b) 6.23µm thick top SiO_2

4.5 Optical Characterization

4.5.1 Scattering Imaging Method Summary

A non-destructive light scattering method was used to characterize the optical loss of ARROW waveguides [91]. As Figure 4-6 shows, a water-filled ARROW sample with good facets was stabilized on an xyz stage. An input laser beam of 650 nm was coupled into the ARROW chip through a single mode fiber. A video camera (FASTCAM SA3), operating in the linear response mode, was connected to a macro lens (105mm, F/2.8) and then used to image the light scattered from the top of the waveguides.

The scattering measurement is based on the assumption that the light power scattered out of waveguides is proportional to the power guided in them [92]. After a waveguide has been imaged, software tools such as the image processing toolbox in MATLAB can be used to extract information about scattered light intensities versus position and solve the loss coefficients of the waveguides. The detailed steps are described in the following.

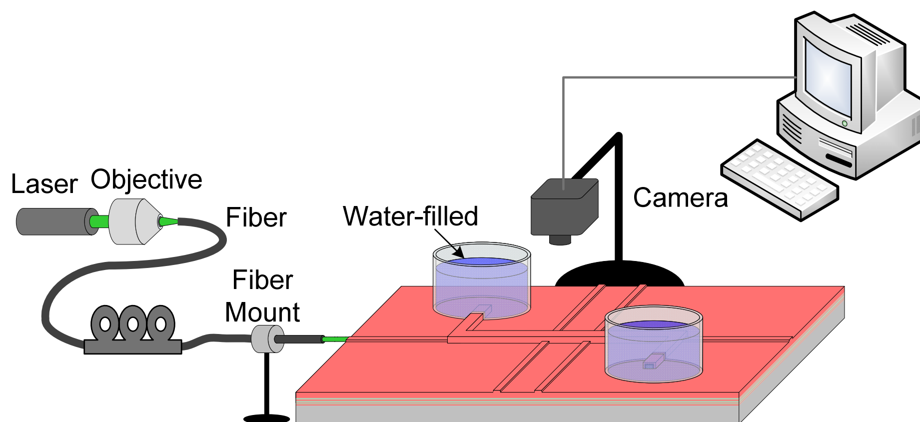


Figure 4-6: Experimental setup used in scattered light imaging method

4.5.2 Sample Preparation

Before the samples were measured, liquid core ARROW chips have to be filled with water without air bubbles to ensure the accuracy of the measurement. Light will scatter exactly where a bubble exists and end propagation. To ensure bubble free filling, first, the samples should be immersed in nanostrip (a commercially available acid - H_2SO_4:H_2SO_5:H_2O_2:H_2O=9:0.5:0.1:0.5 Cyantek) for at least 12 hours to remove any possible dirty things inside the channel. Then the samples must be rinsed thoroughly with DI water for 60s and blow dry with nitrigen. Before filling the channels, a drop of soap (Triton X) is mixed into a small dish of water. The soap helps to reduce surface tension in the water and allows the channels to fill more easily. The dish with water and Triton X should be loaded into a vacuum oven at room temperature. Vacuum should be applied for 10 minutes while the soapy water is being de-gassed, reducing the amount of gas in the water and discouraging bubbles.

After the soapy water has been de-gassed, samples should be carefully placed into the water. A syringe filled with the soapy water can be used to expel large bubbles that form in the reservoirs. After each sample has been placed in the dish and all reservoir bubbles are removed,

the dish should be again placed into a vacuum chamber for another 10 minutes. After that, all samples have to rest in the water in the cleanroom for approximately 5 hours before taking them out for measurement. According to careful observation, bubbles in the channels slowly migrate out to the reservoirs. Care must be taken no to leave the sample in water for longer than this, however, if they are left in for too long the marine epoxy on the reservoirs begins to disintegrate and like to form around the liquid core channel. This will have a negative effect on the device performance and the measurement reliability.

4.5.3 Experimental Measurement and Data Processing

The chips are put on the experimental stage, as Figure 4-6 shows, after the wafer is filled with water. The input light coming from the laser is aligned with the solid core waveguides on the chip by adjusting the position of the channels in three dimensions. To characterize the whole ARROW chip, more than one image has to be taken for the same sample using different exposure times. This is because the overall transmissions for ARROW chips are low and therefore pixels easily get saturated in either the first section or the second half of the device. Pictures taken at longer exposure times (1/60 or 1/250 seconds) accurately measure the second half of the device, likewise pictures at shorter exposure times (1/1000, 1/2000, or 1/3800 seconds) accurately measure the first half of the device. As shown in Figure 4-7(a-b), two images were taken at an ARROW chip using 1/60s and 1/2000s respectively. The light which propagates along the waveguide can be described by the Equation (4-2).

$$P(z) = P(0)exp(-\alpha z) , \tag{4-2}$$

where P(z) is the optical power at position z and P_0 is the power at the beginning of the chip. A vector of integrated intensity (power) versus position can be extracted from the images using MATLAB curving tool box and the natural logarithm is applied to solve the propagation loss α

as the slope of a line. Figure 4-8 shows the resulting intensities in a logarithm as a function of position with two different exposure times (1/60s: grey and 1/2000s: green). It can be seen that the optical power saturates (too large) in the first section of the solid core waveguide when the exposure time is 1/60s while it saturates (too week) in the second section of solid core waveguide when the exposure time is 1/2000s. As Figure 4-9 demonstrates, the propagation loss in the first section of waveguide can be solved using the data extracted from Figure 4-7(b) and the loss in the second section of waveguide can be solved with data from Figure 4-7(a). The loss coefficient in the liquid core waveguide can be found out using either data sheet.

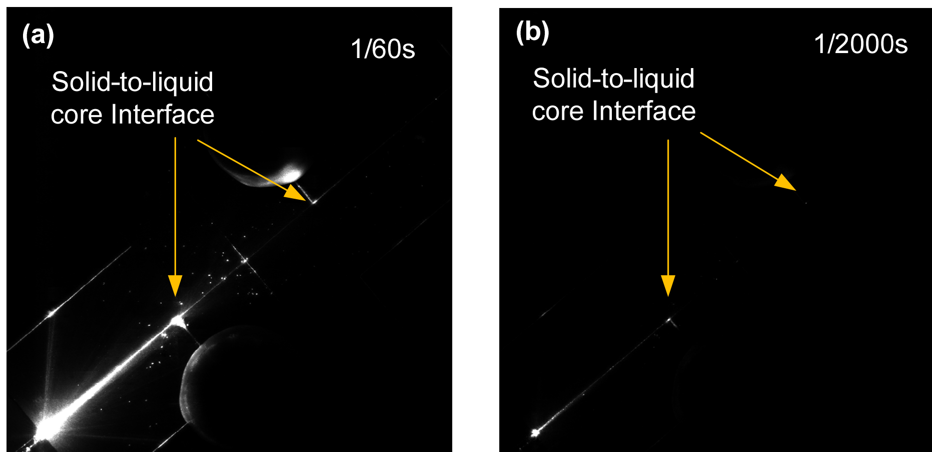


Figure 4-7: The scattering images taken from the same ARROW chip using two different exposure time (a) 1/60s, (b) 1/2000s

Once all propagation losses are known, the overall transmission T can be measured using Figure 4-8, where values at the beginning and end of the included data are placed in the exponent to invert the logarithm operation. κ_i is solved for analytically using Equation (4-3).

$$T = \frac{e^{line\ fit(i1(ending\ point))}}{e^{line\ fit(i1(beginning\ point))}}. \quad (4\text{-}3)$$

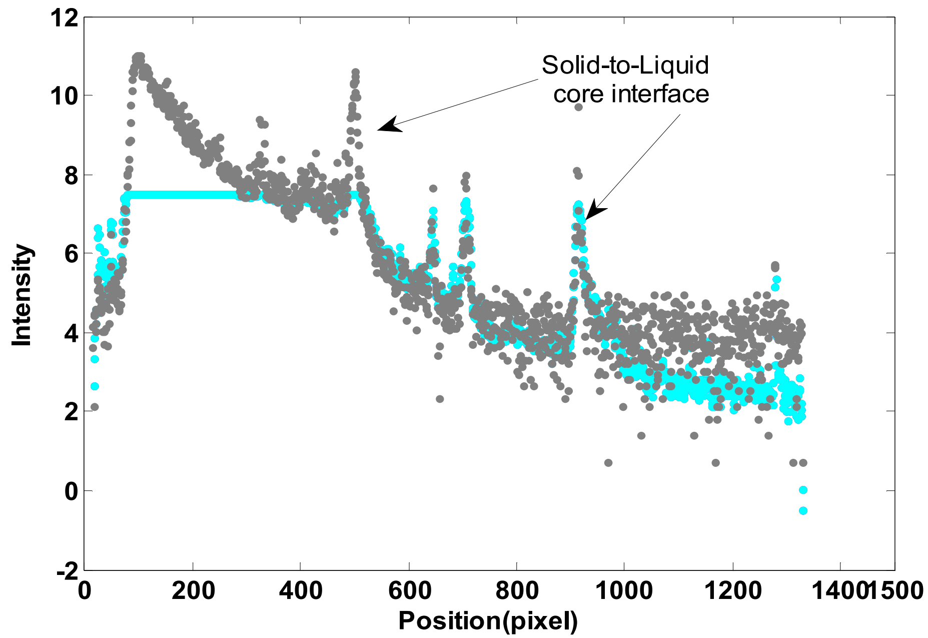


Figure 4-8: Intensities versus positions: grey (1/2000s exposure time) and blue (1/60s exposure time)

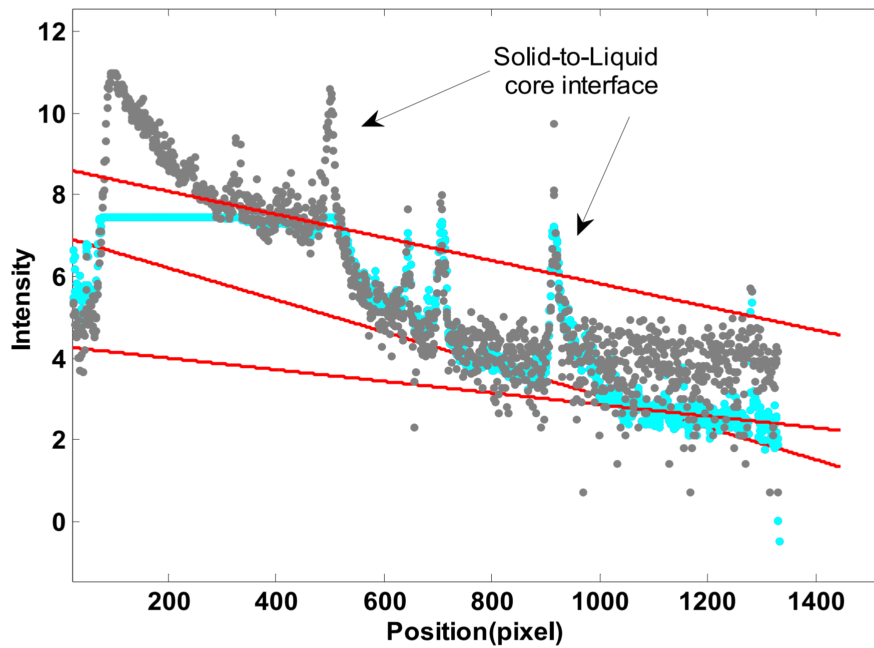


Figure 4-9: Intensities versus positions and fitting curves (red) for three sections of an ARROW chip

4.5.4 Results and Accuracy

In order to determine the experimental uncertainties of this measurement technique, a single device was aligned and imaged 10 times and the solid- and hollow-core waveguide losses measured. The results of this test are shown in Figure 4-10(a-b), where the experimental uncertainty was calculated to be a value encompassing 68.2% of the measured values. An uncertainty of 15.8% was found for the solid-core measurements and an uncertainly of 12.6% was found for the hollow-core measurements.

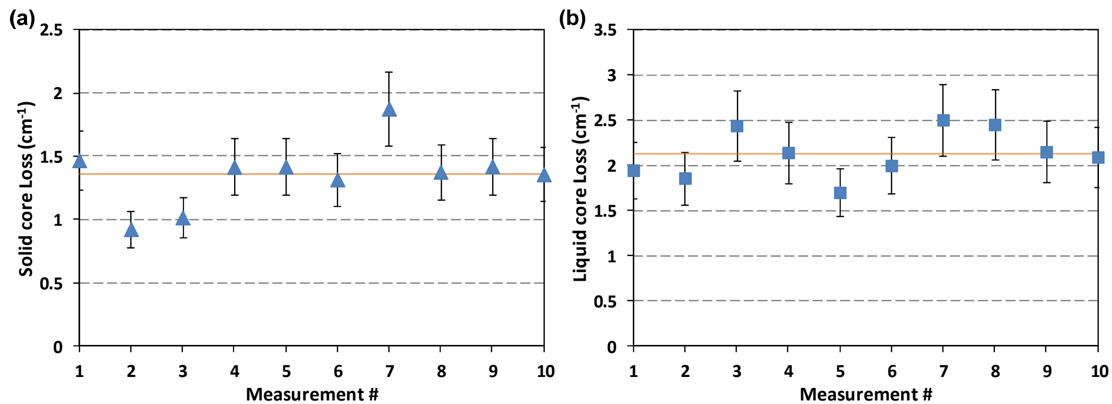


Figure 4-10: Loss measurements made on the same optofluidic platform multiple times. A mean value for these measurements is shown by the solid lines and experimental uncertainty is indicated by the error bars. (a) solid core, (b) liquid core

With the measurement uncertainty determined, the scattered light imaging method described above was applied to twenty-eight ARROW devices with the different topmost SiO_2 thickness as explained in Table 4-1[93]. The average loss coefficient for solid-core waveguides was 1.63cm^{-1} with a standard deviation of 0.36cm^{-1}. The average hollow-core loss was 2.19cm^{-1} with a standard deviation of 0.42cm^{-1}. The average coupling efficiency κ_i was calculated for each sample and plotted versus the thickness of top SiO_2 in Figure 4-11. The measured data shows an

ascending trend from 18% to 67% for interface transmission when the thickness of top SiO_2 increases from 3μm to 6μm. Comparing with the simulation results, the trend of the experimental results matches the simulation results taking the crevice into account, but they appear lower than the simulation results. The reflections from upper layers on the sidewalls of the hollow cores, core roughness and imperfections, and variations on the thickness of layers are the likely causes for this discrepancy. As a practical consideration, we are reluctant to grow the SiO_2 thicker than 6.5μm in a PECVD process because of the rapid incorporation of additional scattering defects into the film at these thicknesses and the accumulated stress that leads to film delamination.

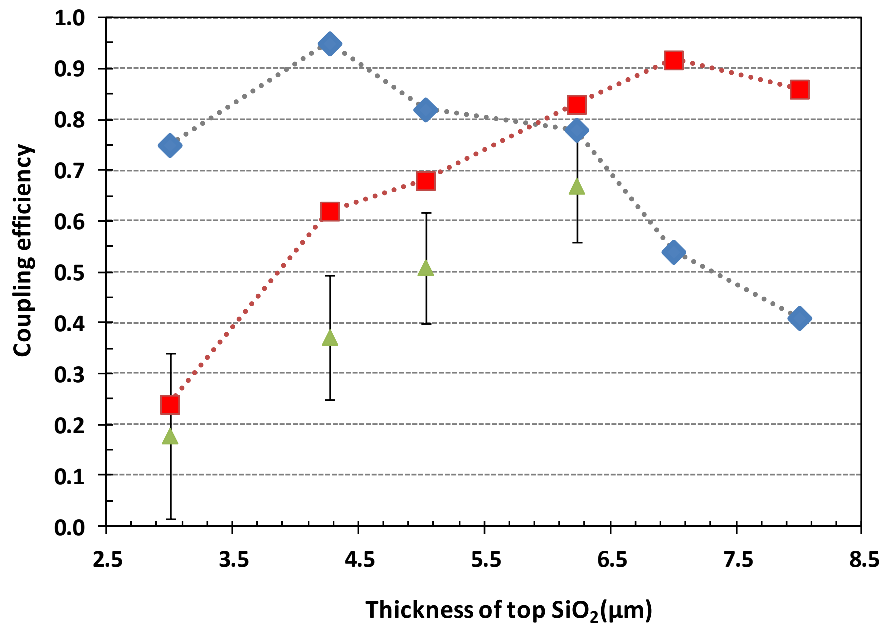


Figure 4-11: Simulation results under ideal conditions (diamonds), simulation results taking crevice into account (squares), and experimental results (triangle) with standard deviation for interface transmission on ARROW chips

It is important to note that before this systematic study of cladding height, we had attributed the bulk of interface losses to imperfections in ARROW layer thicknesses surrounding

these interfaces. A structure was reported in [94] that selectively removed all but the topmost SiO_2 layer at the interface and κ_i was improved up to 73%. However, the devices in [94] were coated with 5μm-thick top SiO_2 instead of a previously used 3μm-thick layer, and the influence of SiO_2 thickness on κ_i was not examined separately until the study described here. By comparison, as shown in Figure 4-11, κ_i was improved to around 50% by only increasing the thickness of top SiO_2 to 5μm. Given the 73% transmission measured for the 5μm SiO_2-only interfaces, we conclude that mode mismatching and layer thickness imperfections contribute significantly to interface loss. Based on our results, we can predict that a SiO_2-only interface with a 6-6.5 μm thickness would have even greater than 73% transmission.

In conclusion, the interface transmission between solid and liquid core waveguides is one of the most dominant factors impacting the throughput in an optofluidic chip. The interface transmission relies on the mode-matching at the interface and is also limited by fabrication non-idealities. Simulations and experiments were performed to improve the interface transmission by enhancing the mode matching in the vertical direction. By increasing the thickness of top SiO_2 to around 6~6.5μm thick, the effect of crevices forming at the interface was compensated. The coupling efficiency was improved by a factor of 3.7 and the overall throughput was enhanced by a factor of 17.1. Simulations taking into account real film profiles match experimental trends and illustrate the need for mode alignment at waveguide interfaces.

5 ALL-SPUTTERED HOLLOW WAVEGUIDES

5.1 Introduction

As described earlier, surface micromachined ARROWs created previous to this research were typically fabricated by surrounding the sacrificial core with alternating dielectric layers formed using PECVD. Silicon nitride (SiN) and silicon dioxide (SiO_2) have been the dielectrics of choice and are deposited at temperatures of at least 250˚C to grow conformal films. Cores typically have either arched shaped or rectangular cross sections [15, 95]. The arched shaped ARROWs [96] are made by reflowing photoresist while rectangular shaped ARROWs are made with SU-8 or aluminum [16] as a sacrificial material.

The process based on PECVD thin film deposition has some downsides that can potentially be addressed using sputter deposition: 1) SU8 or photoresist sacrificial lines are used that carbonize at these temperatures and so strong acids must be applied to remove the core. This is a diffusion driven process and can take a relative long time for small geometry cores (around 1 week in a heated Piranha [97] bath to produce a 1.5 cm long waveguide). Because sputtering can be done near room temperatures, coated polymer sacrificial layers can be removed with solvents. This potentially cuts the fabrication time significantly for arch shaped hollow waveguides. 2) The deposition of PECVD layers over large areas with precise thicknesses and refractive indexes can also be challenging because of the complicated chemical reactions during a CVD process, especially for Si_3N_4 and Ta_2O_5. 3) Additionally, the native photoluminescence of

silicon nitride films deposited by PECVD are relatively high as stated in Chapter 3, which can decrease the sensitivity of optical sensing, especially fluorescence sensing.

In this chapter, sputtered deposition [98-101] is investigated as a means of growing dielectric layers for making hollow core ARROWs, with hopes of overcoming some of the material downsides and processing challenges associated with PECVD deposition. ARROWs produced only with sputtered layers will be discussed, including their limits imposed by the sputtering process. Optical measurements and results will be presented, including ARROWs with hollow and solid cores.

5.2 Fabrication Process for Arched Core ARROWs

Arched core sputtered ARROWs were constructed by using either a combination of Si_3N_4 and SiO_2 or Ta_2O_5 and SiO_2 for dielectric cladding layers. The waveguides were optimized to guide 633-nm light through a water core (n=1.33) by satisfying the antiresonant condition given by Equation (2-4). The thin film designs for two different cladding material combinations are detailed in Appendix C.

Figure 5-1 shows the fabrication process used for arched shaped, hollow core ARROWs based on sputtering. The first step was the deposition of three pairs of alternating dielectric layers on a silicon wafer using a Denton Explorer 14 system with a three-cathode chamber (Figure 5-1(a)). The growth rates of Si_3N_4, SiO_2 and Ta_2O_5 films were controlled to be around 5~6 nm/min by using the recipe listed in Table 3-2.

5.2.1 Photoresist Reflow

After the deposition of bottom layers, the wafer was prepared with a dehydration bake in an oven at 150°C for 15 minutes. Then SPR220 (Shipley) photoresist was applied on the wafer

and spun at 3650rpm for 60s (Figure 5-1(b)). A soft bake at 115°C on the hotplate for 90s then follows. The wafer is then exposed for 25 seconds in the MA-150 aligner with a mask. The exposed portion of resist is dissolved in 3 minutes in the AZ300K developer. The cross sections of sacrificial cores are now rectangular. The widths of the cross sections varied from 35µm to 9µm and the heights of the cores are about 6µm.

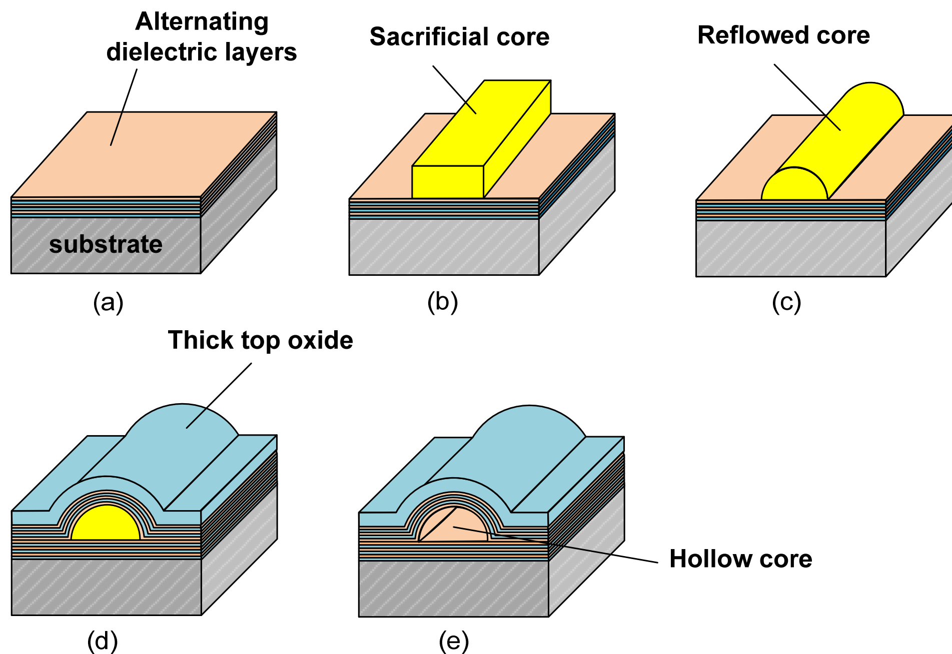


Figure 5-1: Process steps used to fabricate sputtered arch-shaped ARROWs on silicon substrates.

The lines of SPR220 photoresist were then reflowed into arch-shaped cross-sections with smooth surfaces when heated above a liquefaction temperature (around 125ºC) (Figure 5-1(c)). During the reflow process, the widths of the cores are maintained while the total volume of the resist reduces to only 80% of the original due to the evaporation of the solvent. The reflowed shape of photoresist was found to be dependent on its initial width. The dimensions of the

photoresist cores were determined by taking SEMs to measure the widths and heights and shown in Figure 5-2.

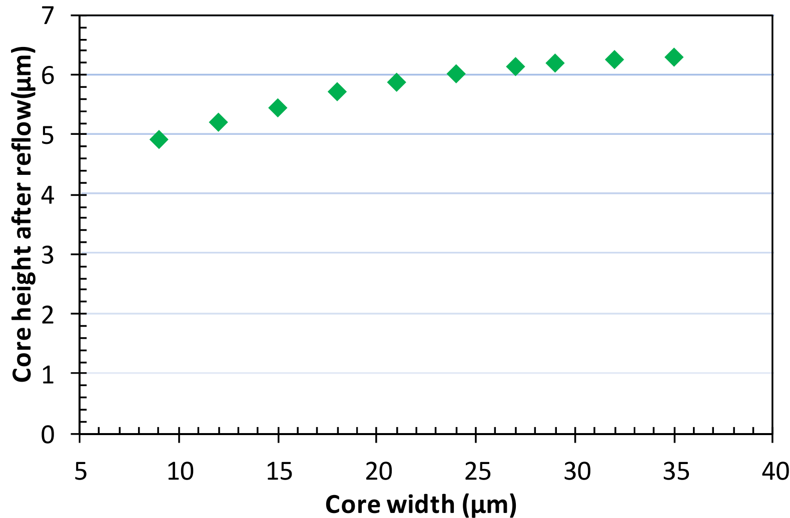


Figure 5-2: Height of reflowed photoresist versus core width

5.2.2 Low Temperature Sputtered Top layers

After the cores were pattered and reflowed, six alternating dielectric layers were deposited over the reflowed photoresist, including a thick top oxide layer which is grown over the other top layers to ensure mechanical strength (Figure 5-1(d)). The sputtering deposition of top layers kept the substrate temperatures below 140˚C, so the photoresist could be removed by an organic solvent instead of acid.

Initially, the top layers were grown while keeping the substrate near room temperature, but the sputtering films cracked and peeled off during the subsequent chemical removal step that etched away the photoresist as Figure 5-3(a-b) shows. As stated in Chapter 3, low temperature films tend to have poor adhesion and mechanical strength. The deposition temperature of all the

top layers was increased to around 120°C, however “knots” appeared in the film near the photoresist lines due to the stress between photoresist and multiple cladding layers as illustrated in Figure 5-3(c). The waveguides would again crack and break during the chemical removal process.

To minimize the stress between layers and enhance the adhesion between top layers and bottom layers, the top layer closest to the photoresist was coated at substrate temperatures of 120˚C and the other five remaining top layers were grown near room temperature. Using this method, the “knots” or bubbles disappeared during the process of growing top layers as shown in Figure 5-3(d).

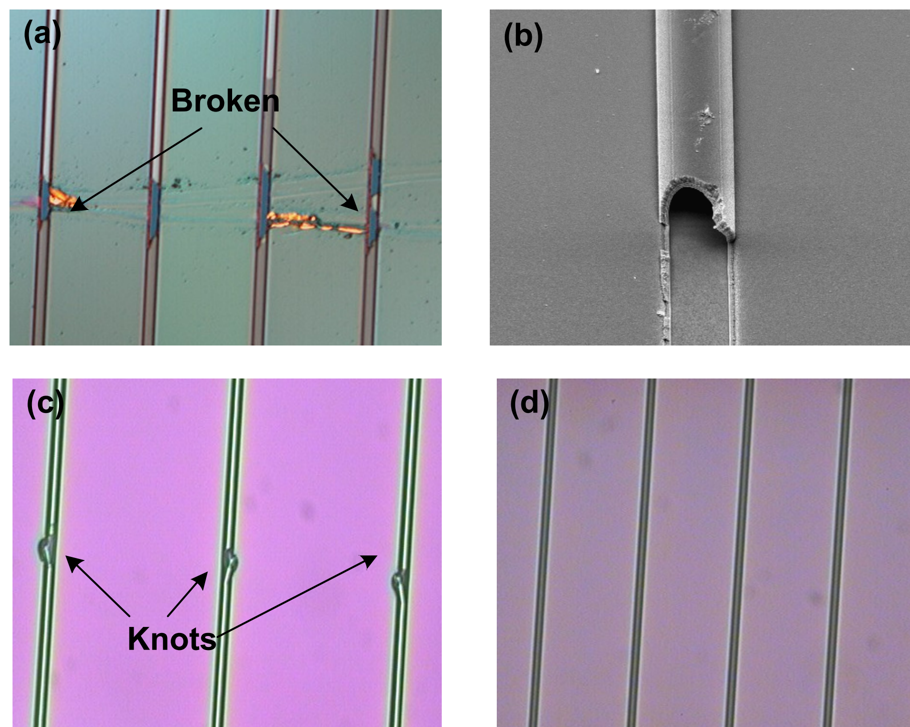


Figure 5-3: Arch-shaped ARROWs with sputtered layers (a-b) deposited at room temperature (broken channels during etching process), (c) deposited at 120°C, (d) one top layer deposited at 120°C and other five layers deposited at room temperature

5.2.3 Solvent Etching

Three solvents were investigated for the removal of photoresist core, acetone, SU8-developer and N-methyl pyrrolidone (NMP). The amount of core etched varied as the square-root of time (this is a diffusion driven process), and can be express by the following equation:

$$l(t) = \sqrt{2k_n DC_0 t} \quad , \qquad (5\text{-}1)$$

where l(t) is the length of the sacrificial core that is etched vs. time t, k_n is a geometric constant, D is the diffusion coefficient of the etchant, and C_0 denotes the concentration of agent in the solution.

Acetone removed the core aggressively and unevenly, leaving residue along the core's length. As Figure 5-4 (a-b) shows, the channels cracked when exposed to acetone. SU8-developer is another option which is much gentler for etching. However, the etching rate in SU8-developer is quite slow. It takes about 4~5 days to finish etching a 1-cm long ARROW waveguide. Another disadvantage of SU8-developer is that it does not dissolve in water. The wafer must be rinsed thoroughly with IPA then with water. In contrast, NMP is a more attractive solvent choice for removing photoresist because it leaves the interior of the waveguide cleaner (Figure 5-4 (c)) and etches with less breaking of the top layers. As Figure 5-5 shows, the narrower channels were etched faster than the wider ones. In 24 hours, the etched lengths for channels of 18μm, 24μm and 35μm were about 11.85mm, 11.44mm and 10.70mm respectively.

Hollow channels were formed after photoresist was completely removed (Figure 5-1 (e)). After NMP etching was complete, the whole wafer had to be rinsed with water, followed by a cleaning cycle of water-nanostrip-water at room temperature for at least 12 hours for each rinse step to make sure no solvent residue remained. The SEM images of the resulting arched shaped hollow ARROW waveguides with sputtered layers are shown in Figure 5-6. For both Si_3N_4/SiO_2

and Ta_2O_5/SiO_2 ARROWs, channels with widths varying between 18μm and 35μm were made successfully while channels with widths below 18μm broke apart during the removal process. This can probably be explained by the crevice problem which has been discussed in Chapter 4. Compared with wide channels, narrow channels form deeper crevices (Figure 5-6 (b)) during the deposition process.

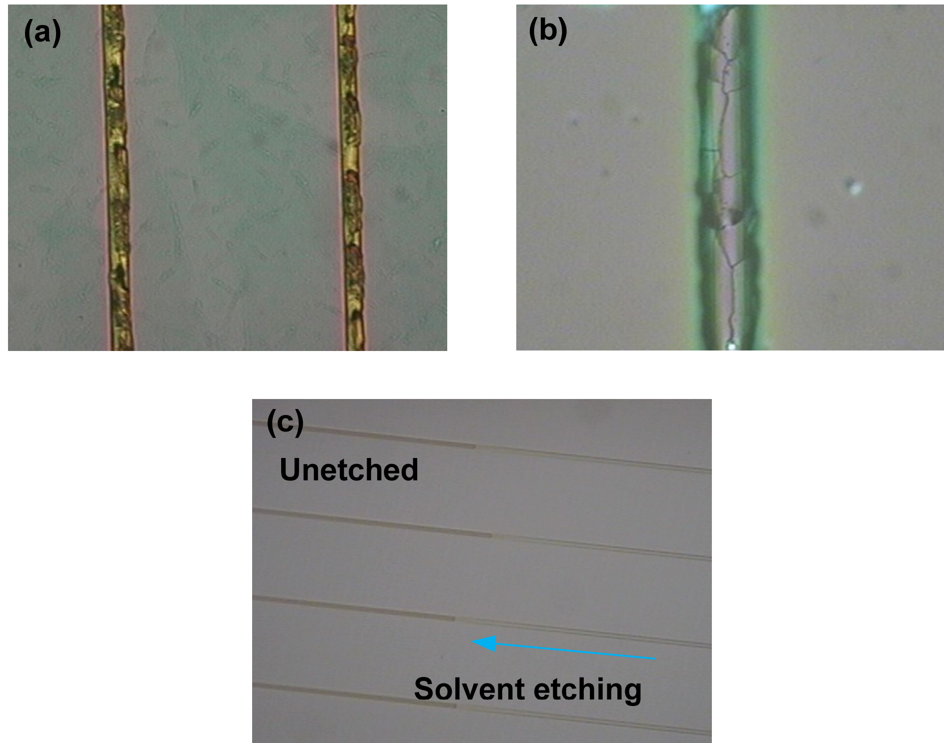


Figure 5-4: Etching in a solvent: (a-b) acetone, (c) NMP

Sputtered layers were also used for making hollow waveguides with a rectangular cross-section. The detailed fabrication process is very similar with that of previous described devices made with PECVD films (Figure 3-1). However, the sputtered layers cannot stand the wet

etching process in the acid, and as a result, hollow channels with a rectangular cross section were not made successfully.

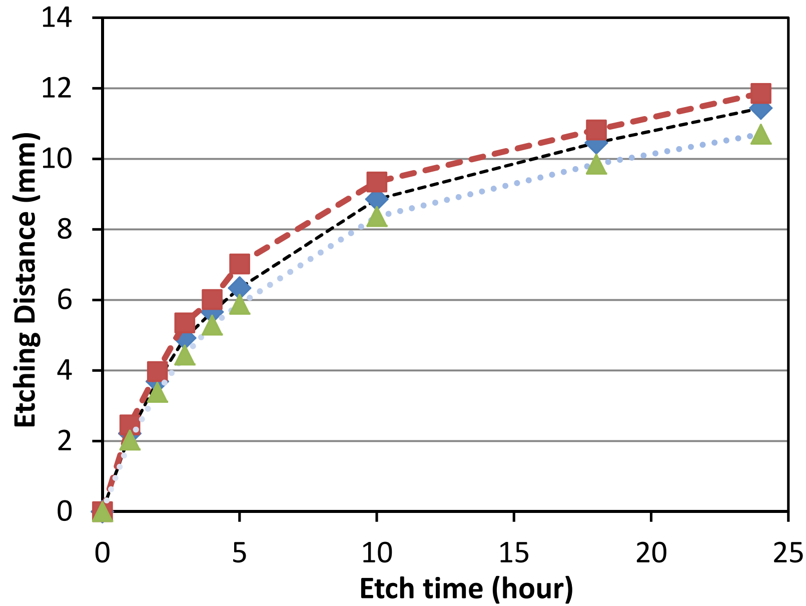


Figure 5-5: The Etching distance versus etching time in NMP at 80°C for an arch-shaped ARROW waveguide with a width of 18µm(square), 24µm(diamond), and 35µm(triangle).

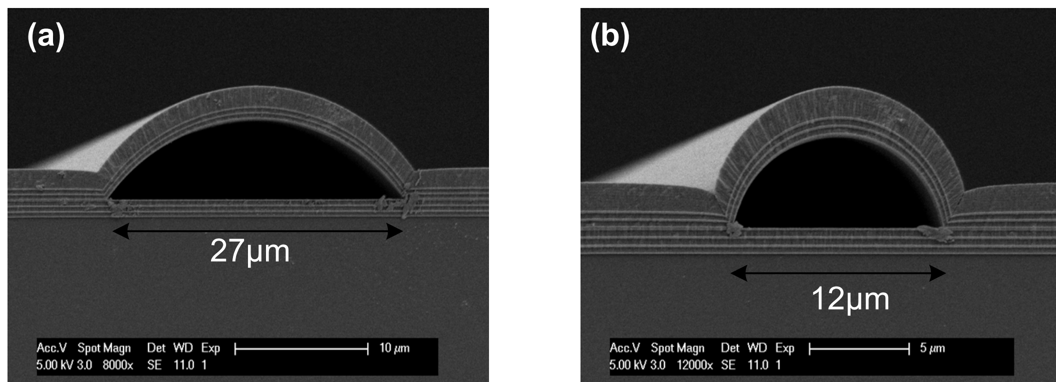


Figure 5-6: SEM images of a resulting hollow ARROW waveguide made with Ta_2O_5/SiO_2 (a) 27µm wide, (b) 12µm wide

5.2.4 Hybrid Glass Coating

In order to further improve the mechanical strength of top layers, hybrid glass (HGT produced by Hybrid Glass Technologies, n~1.465) was studied to protect the whole structure. After the top layers were sputtered over the core, a layer of hybrid glass (HG) was spun and coated over the entire wafer as illustrated in Figure 5-7.

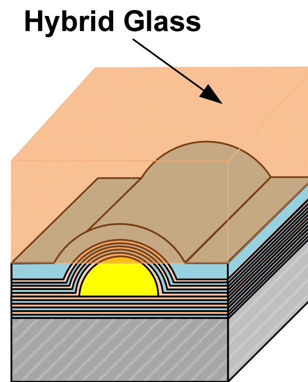


Figure 5-7: Illustration of hybrid glass coating on an ARROW waveguide

HG has to be cured well so that it can survive during the subsequent wet etching process. Since the whole process has to be maintained below 150°C, HG was cured at 140°C in an oven for an hour for a fully curing. Bubbles appeared on all the channels (Figure 5-8(a)) when the HG was baked in this way. These bubbles cause the channel to break even before the devices were immersed in the solvent for etching. This is likely caused by the large differences in the thermal expansion coefficients of HG and ARROW waveguides, which leads to the stress that deforms the channels. After a great deal of experimentation, an optimum fabrication recipe was found: cure the HG on an ARROW chip in a vacuum oven, ramp up the temperature from 50°C to 140°C at a rate of 1°C per minute, and then cool down the wafer to room temperature in the

vacuum environment. With this adjusted recipe, no bubbles were produced during the curing process (Figure 5-8(b)). The SEM images of cross sections of arched ARROW waveguides with HG were shown in Figure 5-8(c-d)).

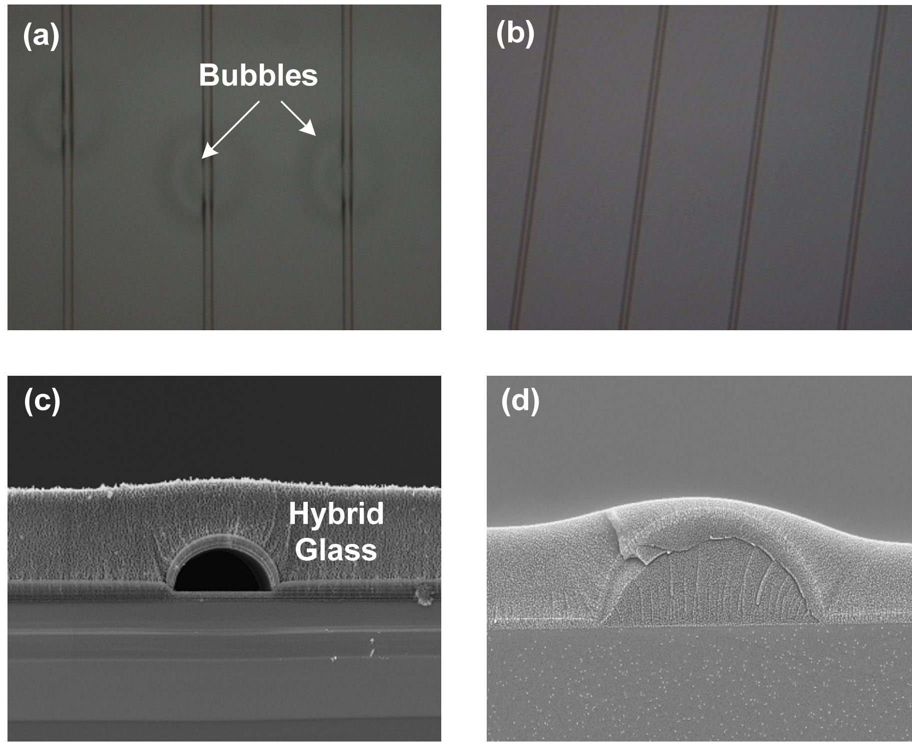


Figure 5-8: Hybrid glass overcoat on ARROW waveguides (a) with bubbles, (b)without bubbles, (c) thick layer coating, (d) thin layer coating

With HG as a protection layer, the channels with varying width from 9µm to 35µm can survive the etching process in NMP as long as the etching can be done in 48 hours. Experiments prove that HG is removed if it is left in the solvents larger than 48 hours. Since NMP etches channel quite fast as described earlier, HG can potentially be used as an overcoat. However, the HG tends to planarize over the core and this will lead to more optical loss for the hollow waveguides.

5.3 Optical Characterization

Optical loss in sputtered hollow and solid core ARROWs was characterized using the cutback method. Figure 5-9 shows the experimental setup used for the cutback loss measurement. An ARROW sample was cleaved with clean edges and stabilized on a XYZ positioner. Hollow core waveguides were filled with water, and 633 nm light from a laser diode was coupled directly into all tested waveguides through a single mode fiber. After propagation through the waveguide, the laser light was collected by a lens system and measured with a power meter. Waveguides were cleaved shorter after each measurement and the throughput power (dB) was plotted versus distance as Figure 5-10 shows. Then the loss coefficient α and coupling coefficient κ can be calculated by an exponential fit of data according to the Equation:

$$P(L) = P(0)\exp(-\alpha L)\kappa \quad (5\text{-}2)$$

where P (L) is the transmitted power after propagation, P(0) is the power from the source, L is the length of the waveguide.

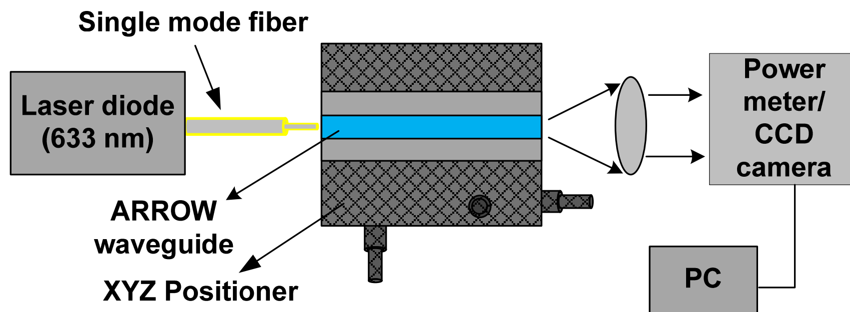


Figure 5-9: Cut-back measurement method for arched core ARROW waveguides

The loss for all hollow (water filled) sputtered, arched core ARROWs tested using the cut back method are illustrated in Figure 5-11. Ta_2O_5/SiO_2 based hollow ARROWs showed an

average propagation loss lower than Si_3N_4/SiO_2 based hollow ARROWs. Simulation results for the two different ARROWs predict similar optical losses despite their refractive index differences. Scattering due to surface roughness or material absorption are likely causes for loss disparity. Surface roughness for these films was measured with an atomic force microscope and all were less than 1.5nm rms (root mean square) roughness. This leads us to conclude that material absorption is the dominant loss factor for these waveguides.

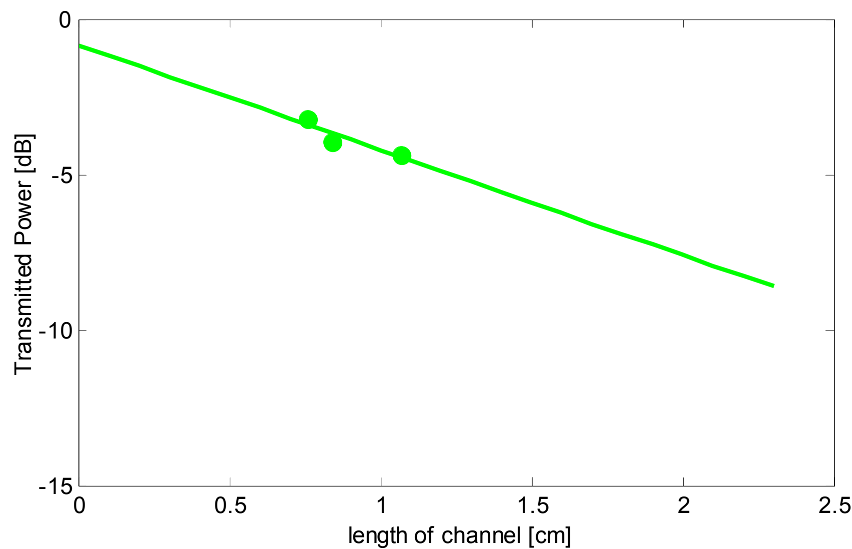


Figure 5-10: Loss measurement for a 32µm wide arched-core ARROW waveguide - measured values (circles) and linear fit to the data

To compare the ARROW waveguides made with PECVD and sputtered films, solid core waveguides were fabricated with a width of 14µm and a ridge height of 1µm. The structures are shown in (Figure 2-13(c)). The propagation loss coefficients achieved by the cut back method are listed in Table 5-1. Given that all solid core waveguides were fabricated with the same geometries and etching procedures, and that the surface roughness for all films was very similar (<1.5nm rms), two primary sources contribute to the high loss of sputtered solid core

waveguides. The first is the absorption in the low temperature sputtered films. The second reason lies in the fact that the topmost SiO_2 layer has to be sputtered for 3~4 times to reach a thickness of 4μm since the growth rate is low and the machine cannot run continually for too long time. This creates a boundary between films which increases the propagation loss of the waveguide.

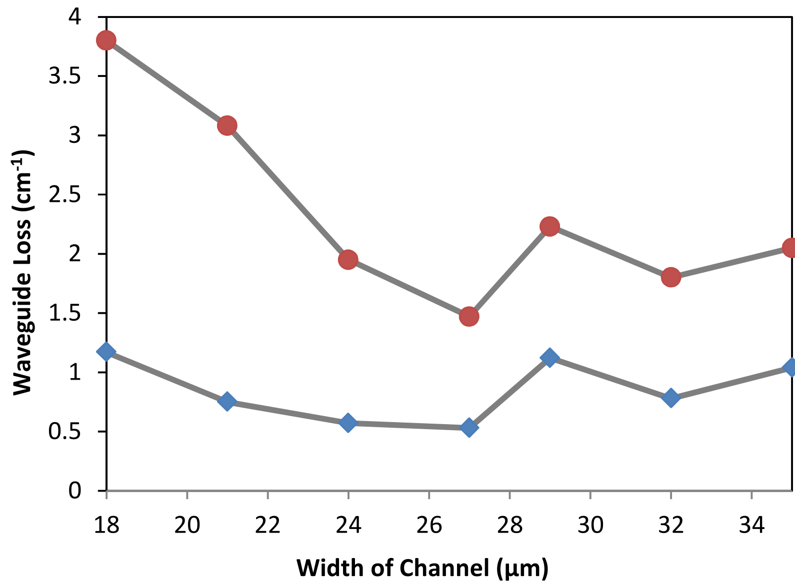


Figure 5-11: Measured loss for hollow waveguides with varying widths fabricated with cladding layers - Si_3N_4/SiO_2 (circles) and Ta_2O_5/SiO_2 (squares)

Table 5-1: Measured Loss Comparison for Solid Core Waveguides

Type	*Cladding materials*	*Loss (cm^{-1})*
Sputter	Ta_2O_5/SiO_2	> 10
	Si_3N_4/SiO_2	> 10
PECVD	Si_3N_4/SiO_2	0.58

5.4 Conclusion

In conclusion, sputtered films are inferior to PECVD films for ARROW fabrication due to their poor adhesion, mechanical strength and film quality. Hollow waveguides with arched cross sections, which are wide from 18μm to 35μm, can be fabricated successfully. However, optical measurements show that ARROW waveguides made with sputtered films have much higher loss than those fabricated with PECVD films. This is most likely due to material absorption. In addition, integrating arch-shaped hollow waveguides and solid core waveguides would be hard due to the non-idealities at the interface. More light will be scattered away from the interface, leading to higher loss. The arched core structure is abandoned in the further study. For rectangular core waveguides made with SU8 sacrificial cores, they cannot survive because the sputtered films crack and peel during the core removal process.

Sputtered Ta_2O_5 film is very desirable from a fluorescence sensing standpoint, however, due to its low photoluminescence background. In order to combine low PL background with high structural integrity, hybrid layers of PECVD SiO_2 and sputtered Ta_2O_5 were constructed. The details of ARROW waveguides made with hybrid layers will be discussed in Chapter 6.

6 HOLLOW WAVEGUIDES MADE WITH HYBRID LAYERS

6.1 ARROW Waveguides on a Planar Substrate

As stated in previous chapters, the sputtered films, especially grown under low temperature, show poor adhesion and mechanical strength than PECVD films. On the other hand, sputtered Ta_2O_5 film is still very attractive for ARROW fabrication since it has much lower photoluminescence than PECVD Si_3N_4 films which has been discussed in Chapter3. Over the past decades, a large number of deposition methods for tantalum pentoxide thin films have been proposed and applied, including anodic or thermal oxidation of tantalum layers [102-104], sputtering [105-108], vacuum evaporation [109, 110], atomic layer deposition [111, 112], and CVD [113-115]. CVD actually is most widely for Ta_2O_5 deposition. However, the typical precursors, such as Ta $(OC_2H_5)_5)$, Ta $(OCH_3)_5$, $TaCL_5$, etc., likely cause high levels of hydrocarbon contaminants [116] (H_2O, CO_2, CO, C_2H_4, CH_4, C_2H_5OH, etc.) which result in high photoluminescence intensity of the film. In addition, CVD process is much more complicate than sputtering because various chemical reactions are involved. As a result, RF sputtering with a pure Ta_2O_5 target is preferred to make Ta_2O_5 films in our IML. From the observations demonstrated in Figure 3-35, the Ta_2O_5 film deposited under 250˚C maintains a low PL intensity comparing with SiN films. This is beneficial from the fabrication point because higher temperature films favor a more robust structure for ARROW fabrication. At the same time, PECVD is employed to produce the SiO_2 film because it has better quality and adhesion.

Moreover, the thick topmost SiO_2 layer (at least 4μm) can be deposited continually without boundaries which decrease the loss introduced by the multiple deposition of the topmost SiO_2.

The specific fabrication process is similar to that of previous SiN/SiO devices which has been illustrated in Chapter 4. The only difference that is the PECVD SiN film was replaced with a sputtered Ta_2O_5 film deposited at 250˚C.

A 12μm-wide and 5μm-high rectangular hollow core hybrid ARROW was fabricated successfully and its SEM image is shown in Figure 6-1. By using the scattering imaging method explained in Chater 4, the loss of the hollw waveguide was measured to be 3.1±0.2 cm^{-1}, which is slightly higher than that of SiN/SiO devices (2.7cm^{-1}). So replacing SiN with Ta_2O_5 film does not increase optical loss dramatically.

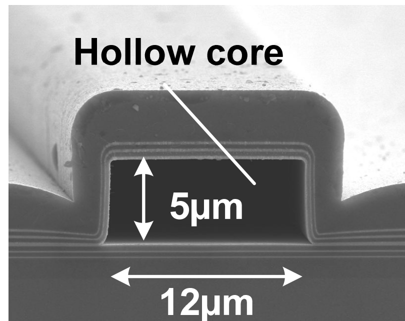


Figure 6-1: SEM picture of a resulting rectangular core ARROW waveguide with PECVD SiO_2 (T=250˚C) and sputtered Ta_2O_5 (T=250˚C)

6.2 SAP SOC structure

6.2.1 Comparison between Planar ARROWs and SAP SOC ARROWs

In order to enhance the optical throughput of the ARROW chip and the yields of devices, a SAP (self-aligned pedestal) SOC structure was proposed. Compared with planar ARROWs (Figure 6-2), the SAP SOC ARROWs (Figure 6-3) can maintain low loss in the liquid core.

Although there is only one top SiO_2 layer to confine the light within the core for the SAP SOC structure, the pedestal beneath the core helps to decrease the loss because air boundaries are formed on the two sides of the core (Chapter 2). At the interface, the transmission loss caused by the reflections on the sidewall of the liquid core was minimized because the five antiresonant layers over the core were removed.

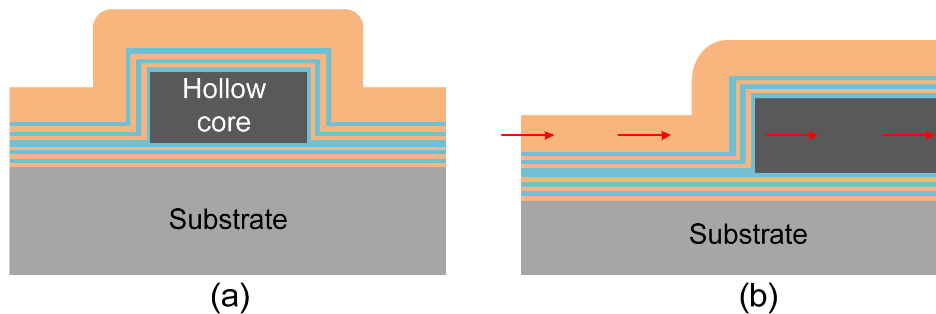


Figure 6-2: ARROW waveguides built on a planar substrate (a) cross-section, (b) interface

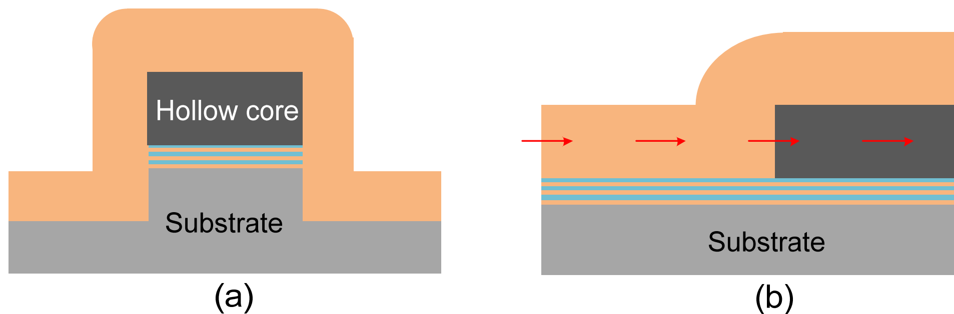


Figure 6-3: SAP SOC ARROW waveguides (a) cross section, (b) interface

6.2.2 Fabrication Process of SAP SOC ARROWs

The fabrication process for SAP SOC ARROW is illustrated in Figure 6-4 [31, 117]. To begin with, three pairs of alternating SiO_2 and Ta_2O_5 layers are deposited on a silicon substrate

and a rectangular core is patterned using SU8 photoresist (Figure 6-4(a)). To accomplish the following steps, an etching mask has to be developed to form pedestals under the hollow core and solid core waveguides. A layer of photoresist (AZ P4620) is spun coated over the whole wafer (Figure 6-4 (b)). After soft bake and exposure, the photoresist over the core is gradually developed before the photoresist on other parts of the wafer because the thickness of the PR over the core is much thinner than in other places (Figure 6-4(c)). A thin nickel film (75~80nm) is then deposited using e-beam evaporation (Figure 6-4(d)). After lift-off, the nickel film is left at desired locations to protect the core and solid core waveguides during the following dry etching process (Figure 6-4(e)).

To create an intact SU8 core and form an anisotropic etching profile, an inhibitor-driven anisotropic etching process had to be developed to create pedestals beneath the hollow and solid core waveguides. The desired height of a pedestal is 5~6μm which has to be taller than the height of the core (5μm). The first step is to etch through 6 bottom ARROW layers (SiO_2/Ta_2O_5), which are about 1~1.2μm thick. Fluorine-based etch chemistries are usually used for SiO_2 and Ta_2O_5 etching, and two common source gases are CF_4 [118, 119]and CHF_3. The typical reactions for SiO_2 etching are explained in Equation (3-8) (3-9) (3-10) (3-11) . In comparison, CHF_3 displays a smaller F/C ratio than CF_4. The addition of hydrogen to fluorocarbon gases helps promote CF_x film growth (such as CF_2, C_2F_4) because hydrogen combines with F radicals. CF_x actually is the main radical which etches the SiO_2 film. The ion bombardment can be very directional in an ICP RIE process with high-density plasma, especially at a low working pressure. Simultaneously, CF_x works as an inhibitor film which can protect the SU8 core from etching. In such plasma, the selectivity of SiO_2/Si can also be enhanced because silicon etching relies on the concentration of fluorine neutrals rather than CF_x radicals [120]. The F concentration is decreased by hydrogen

and the CF_x film protects silicon from etching. The etching recipe is shown in Table 6-1. The etching principles for Ta_2O_5 are very similar with those for SiO_2. Figure 6-5(a) shows an example etch profile that was created using this recipe for SiO_2 and Ta_2O_5 etching.

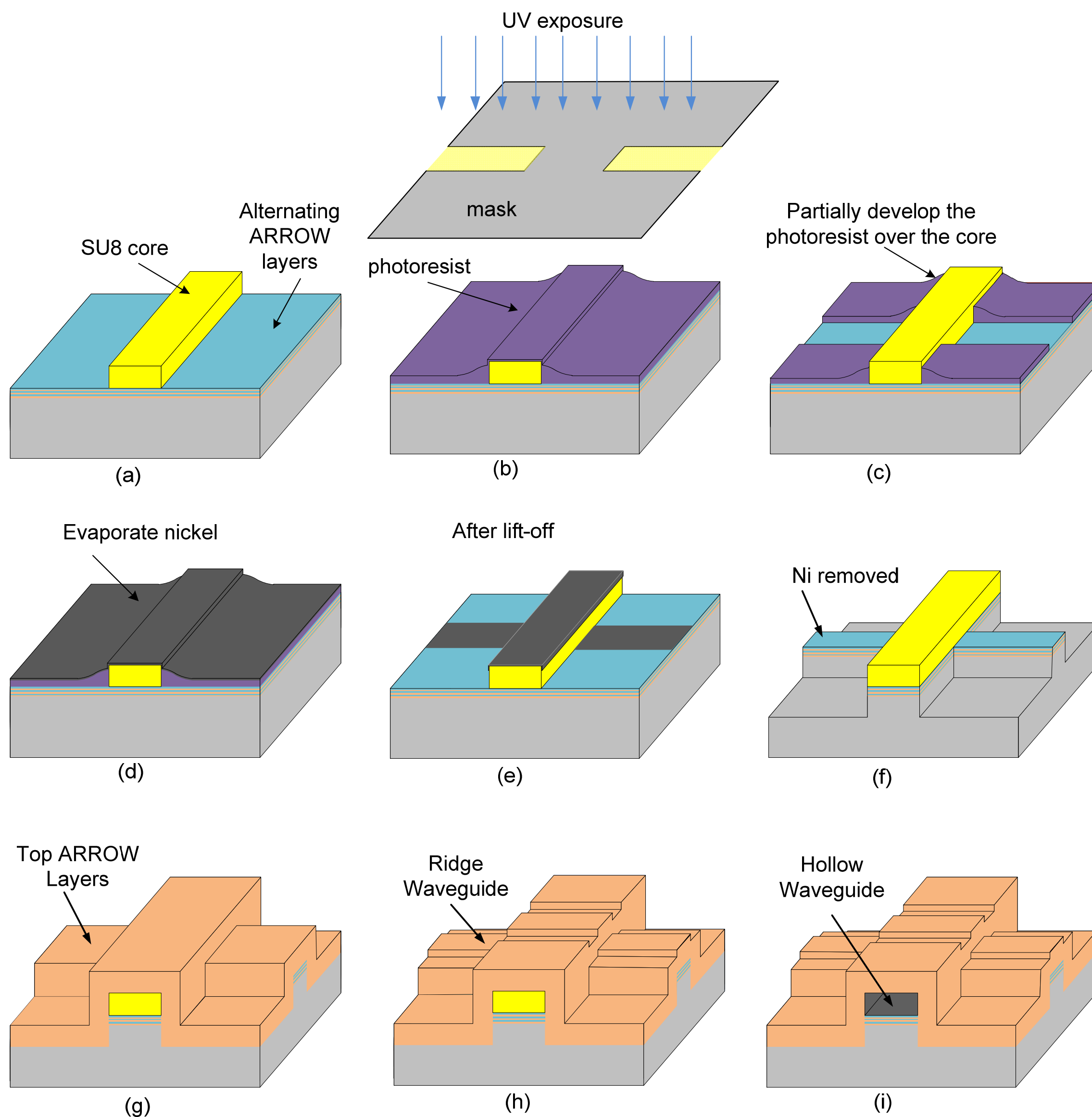


Figure 6-4: The fabrication process of SAP SOC ARROW waveguides

Most dry etching of silicon is accomplished using fluorine [121-123] (SF_6, NF_3, CF_4, etc.), chlorine [124-126] (Cl_2, BCL_3, etc.), and bromine (HBr) based gases [127]. Limited by our Trion system, fluorine based gases were only considered for the etching. Other researchers have used the black silicon method [128]. Here, $SF_6/O_2/CHF_3$ is often employed to control the etching profile of silicon since SiO_xF_y can be formed to serve as an inhibitor film. However, this method is not suitable in this case because a large amount of O_2 must be added which reacts with SU8 rapidly. The Bosch process [129, 130] is another deep silicon etching method which has become popular used for many applications in microelectronics, MEMS, and photonics [131]. The Bosch process involves alternating passivation and etch steps and allows for high aspect-ratio etching with a great deal of control over the etch profile. During the passivation step, a fluorocarbon polymer inhibitor film is deposited isotropically on the substrate, usually using C_4F_8 as the source gas. The etch step employs the ion-enhanced energetic etch mechanism, often using SF_6/O_2. The overall etch profile can be anisotropic as long as the deposition and etching steps are carefully adjusted. The etch process developed for SAP silicon pedestal etching uses the same principles as the Bosch process. But C_4F_8 is not available for the Trion ICP/RIE system, the lower-cost gas CHF_3 was investigated as a replacement gas for polymer formation. For the etching step, a mixture of SF_6/CHF_3 gases is used to replace SF_6/O_2 for inhibitor driven etching because O_2 will deteriorate the SU8 profile. The recipe for etching silicon pedestals was shown in Table 6-1.The etching rules for silicon can be demonstrated in Equation (6-1) and (6-2). Although the CHF_3 produces fluorine, which is the reactive species that etches the silicon, the high process pressure and lack of ion bombardment during the deposition step causes polymerization to be favored over etching [94]. For each cycle of one 20 second passivation and one 11 second etching step, about 200 nm of silicon is removed. For SAP etching, about 25

cycles are used to etch 5 μm-tall silicon pedestals, with an example silicon pedestal shown in Figure 6-5(b).

$$SF_6 \xrightarrow{yields} SF_5 + F \; or \; SF_4 + 2F \; etc. \quad (6\text{-}1)$$

$$Si + F \xrightarrow{yields} SiF_4 \uparrow . \quad (6\text{-}2)$$

Table 6-1: Plasma Etching Recipes for SAP ARROWs Using the Trion ICP/RIE

Recipe		ICP (w)	RIE (w)	Pressure (mTorr)	Gas Flow (sccm) SF_6	Gas Flow (sccm) CHF_3	Etching Rate (nm/s)
SiO_2(PECVD) Ta_2O_5(sputter)		350	70	18		125	1.5 0.47
Si	Passivation (20s)	550	0	120		75	
Si	Etch (11s)	550	60	35	20	30	
Isotropic Si etch		0	200	150	50		varies

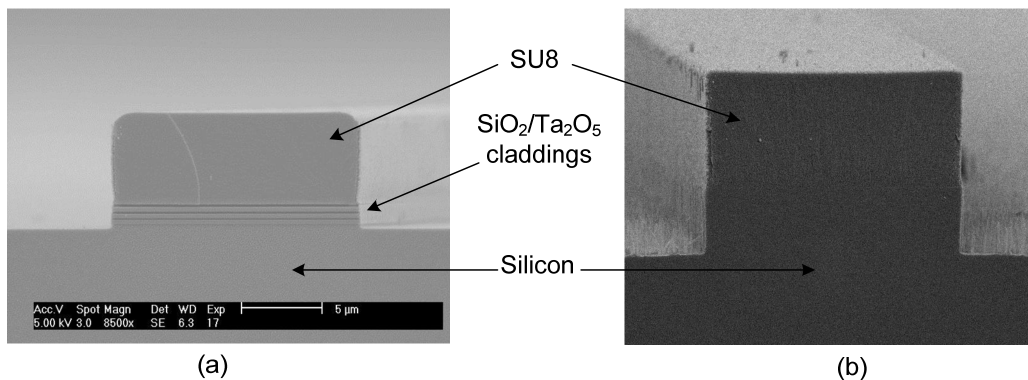


Figure 6-5: The etching profile of SAP structure (a) SiO_2/Ta_2O_5 cladding layers etching, (b) silicon etching

Etch grass (silicon spikes) [132, 133] is always formed after the described etching processes, as shown in Figure 6-6(a-b). This is because small clusters, which remain on the substrate, act as micromasks [128, 134] on the wafer surfaces. The clusters consist of debris from

the redeposition of mask materials, defects formed on the etching surfaces before the etching, and the fluorocarbon-containing residue coming from the excessive passivation process. The grass height can reach up to ~1µm after the etching of 5µm-high pedestals.

The formation of the grass would not necessarily be a problem with SAP ARROW etching, as most of the grass is far from the waveguide pedestal. However, the upper PECVD cladding layers that are subsequently deposited will be much rough over the grass, which will lead to higher loss, especially when these layers are very close to the edges of the pedestals.

In the SAP etching process, the imperfections can also come from PECVD or sputtered layers or any previous process steps which cannot be eliminated entirely. To reduce these defects, the PECVD and sputter chamber has to be cleaned. Between each layer deposition, an O2 plasma cleaning (100w, 60s) step has to be applied to remove any organic contaminates during the PECVD or sputtering process. It has been reported that another possible reason behind silicon grass production is the localised concentration of incoming fluoride ions when SF6 flow is very high [135]. In the etching recipe shown in Table 6-1, SF6 gas is limited to a low flow rate to discourage the grass.

The methods described above can help to reduce grass, but some grass inevitably survives. A post-treatment by isotropic plasma etching of SF_6 [136] had been reported to effectively improve the smoothness of silicon surfaces. So after the pedestal has been etched, an isotropic silicon plasma etch process is performed (see Table 6-1Table 4-1). This isotropic etching attacks the silicon base of the etch grass and undercuts it to the point where the grass collapses. For overlong overetch times, the pedestal sidewall can be severely undercut. Due to this disadvantage, a post-treatment of the patterns by isotropic etching using SF_6 is only applied for 60s at high pressure. This short post-treatment creates only a slight tilt angle for pedestals,

which usually is not an issue for the SAP structure. Figure 6-6(c) shows a SEM image of the SAP ARROW structure after the etch grass has been removed by this isotropic plasma etching and water rinsing. The roughness of the silicon grass can be reduced to about 200nm after this step.

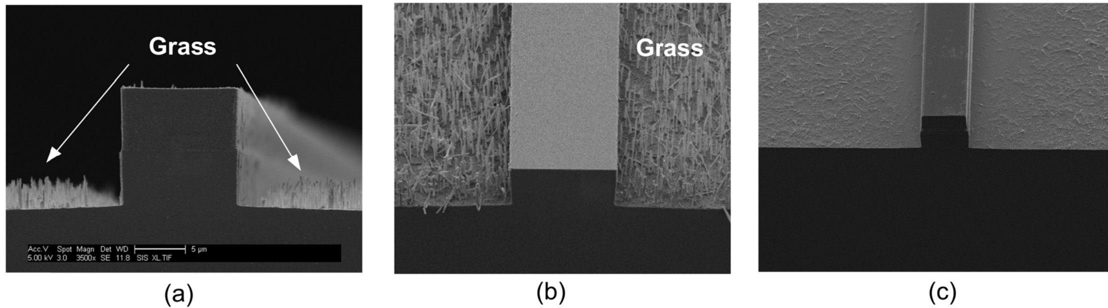


Figure 6-6: SEM pictures of (a) (b) etch grass after SAP etching and (c) after grass removal

As stated above, the rough surfaces of silicon can also arise from the post-etch residue which is mainly make up of fluorocarbon-containing films formed during the inhibitor driven etching process (including SiO_2/Ta_2O_5 stacks and silicon etching steps). In the SAP etching process, fluorocarbon residue not only remains on the surfaces of silicon leading to the micromasks but also on the SU8 core, especially on the sidewalls. The post treatment using isotropic etch can only partially remove the CF_x residue from the SU8 core (Figure 6-7(a)). In order to avoid defects and device failure, extra post-etch cleaning steps had to be developed that were compatible with other ARROW fabrication processes.

For most microelectronic devices, etch residue can be removed by ‘‘ashing’’ in an isotropic plasma of O_2, thereby converting the fluorocarbon film residue to volatile products such as CO, CO_2, COF_2, H_2O, HF, CF_4, etc. However, for the SAP ARROWs, the oxygen-based

plasma would also strip off the SU-8 material which contains organic groups. Reducing chemistries such as H_2 or H_2/N_2 plasmas [137] are possible alternatives. The shortcoming of these plasmas is they often do not remove the fluorocarbon residue completely and require an additional liquid step based on n-methyl pyrrolidone (NMP) which tends to displace the SU8 core from the substrate.

Due to certain limitations of plasma cleaning, liquid-based methods continue to be widely prevalent in IC fabrication. The most common silicon surface clean in the IC industry for the last 30 years is the RCA clean procedure. This process consists of SC-1(standard clean-1), dHF (Diluted Hydrofluoric Acid) and SC-2 cleaning steps. The SC-1 step is an aqueous mixture of ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) heated to 60 °C. The dHF is a 50:1 mixture of deionized water (DIW) and hydrofluoric acid (HF). The SC-2 step is an aqueous mixture of hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) heated to 60 °C. The SC-1 strongly oxidative and removes organic contamination from the surface by oxidation. On silicon, this step also causes the growth a thin oxide that captures metallic contamination on the surface. Dilute HF etches a thin layer of silicon dioxide from the surface. The SC-2 step removes metallic and other ionic contamination from the wafer. The RCA clean is effective for removing both polymeric and metallic contamination from silicon or silicon dioxide. SC-1 solution was tried as a residue remover on ARROW samples after pedestal etching. It proved to be effective for removing fluorocarbon residue but too aggressive for the SU8 material. Commercial formulations based on hydroxylamine solvents are another option. But these amines probably cause poisoning [138] of the chemically amplified resist in residues that remaining after the cleaning step which is not suitable in our IML.

Some researchers suggest that the replacement of NH_4OH with tetramethylammonium hydroxide (TMAH) in the SC-1 clean can be equally effective at contamination removal [139]. To investigate the possibility, H_2O_2 and RS-6 (the photoresist remover, contains ~8% TMAH in H_2O: Cyantek Corp., Fremont, CA) were mixed 1:10 by volume for the cleaning solution which is called TPM [139]. Wafer containing SAP ARROWs were placed in this solution at 40˚C for 10 minutes to remove the etch residue after the SiO_2/Ta_2O_5 etch step and again after the silicon etch step. After each cleaning step, the wafer is soaked in water for 5 minutes to thoroughly clean off the solution.

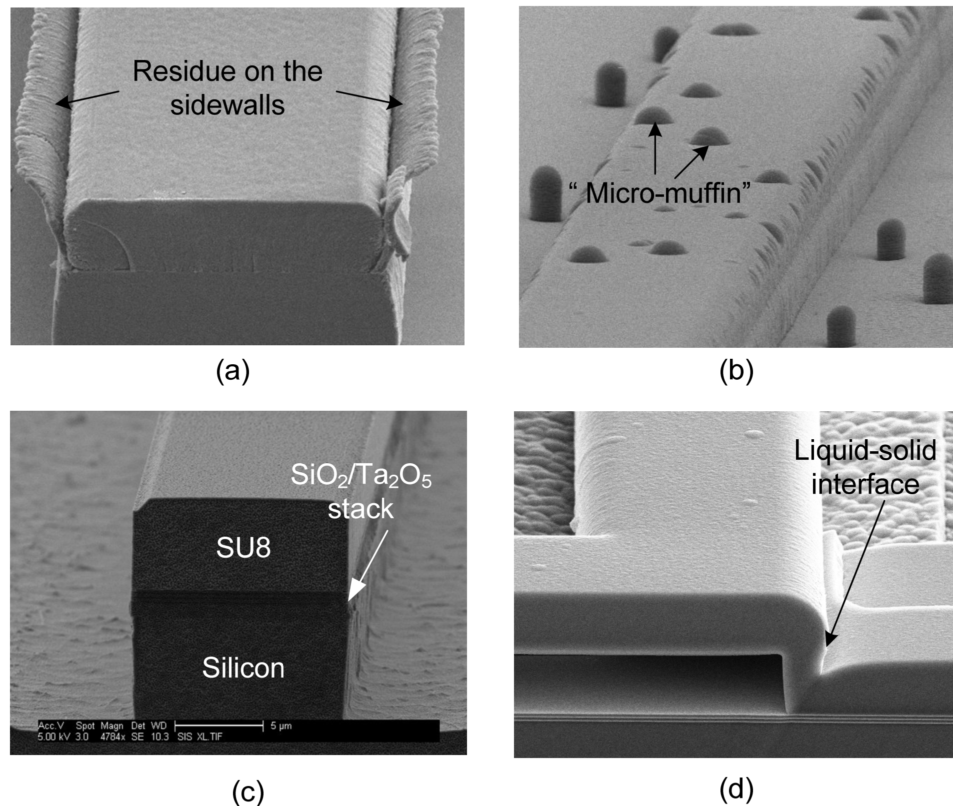


Figure 6-7: (a) Fluorocarbon film residue on the sidewalls of SU8 core, (b) after TPM cleaning but without O_2 plasma cleaning and dehydration, (c) SAP structure after all the cleaning procedures, (d) clean SAP SOC ARROW structure after thick top SiO_2 was deposited

Bases on the results described above, a standard cleaning procedure combining dry/wet etching process after SAP etching was established: isotropic SF_6 plasma etching, TPM cleaning, water soak, O_2 isotropic plasma etching (50w, 30s), dehydration bake (150˚C, 10min). Any skipped step in the cleaning procedure will result in dirty surfaces for ARROW structures as Figure 6-6 (a-b) and Figure 6-7 (a-b) show.

After the pedestal is formed, the Ni masking layer is taken off by nickel etchant as Figure 6-4(f) demonstrates. The steps that follow in Figure 6-4 (g-i) are very similar to the fabrication process for planar ARROW waveguides which were described in Chapter 3.

Figure 6-8 shows a SEM image of a completed SAP SOC ARROWs fabricated with SiO_2 and Ta_2O_5 with a core dimension of 12μm×5μm.

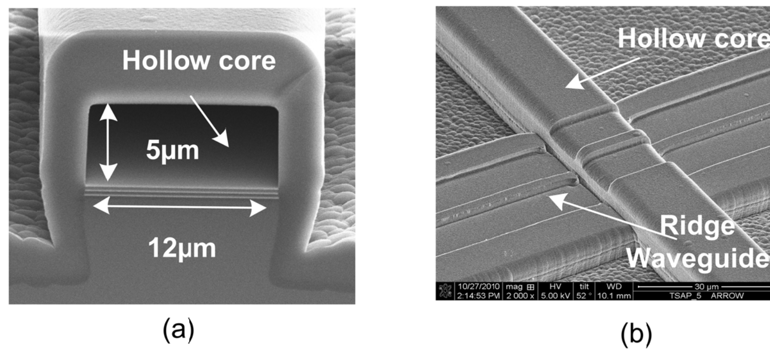


Figure 6-8: The SEM images of SAP SOC ARROWs (a) cross section, (b) top view

6.3 Optical Characterization and Fluorescence Testing

As stated in Chapter 3, sputtered Ta_2O_5 shows lower PL than Si_3N_4. In order to explore and compare the detection sensitivity between SiN/SiO_2 ARROW chips and Ta_2O_5/SiO_2 ARROW chips, the photoluminescence background was also measured on complete multi-layer, solid-core ARROW waveguides using the previous described spectrometer [27]. As shown in

Figure 6-9 (a), a 3mm-long solid core waveguide sample was placed vertically on the instrument's measurement stage and the excitation light was coupled into the solid core waveguide. The PL signal was guided and collected by a detector through an objective lens. It must be noted that the PL spectra shown in Figure 6-9 (b) is generated by the whole solid core waveguide rather than only a single film as in Figure 3-35, and compares the normalized PL signal from solid core Ta_2O_5/SiO_2 and SiN/SiO_2 ARROWs. Because of the long length of the waveguides, the differences in PL shown by the films in Figure 6-9 (b) are magnified dramatically. Photoluminescence measurements show ARROW waveguides fabricated with Ta_2O_5/SiO_2 reduce the PL background between 660nm and 690nm significantly compared to SiN/SiO_2 devices. This improved material system potentially allows for much better signal-to-noise ratios when doing fluorescence based sensing.

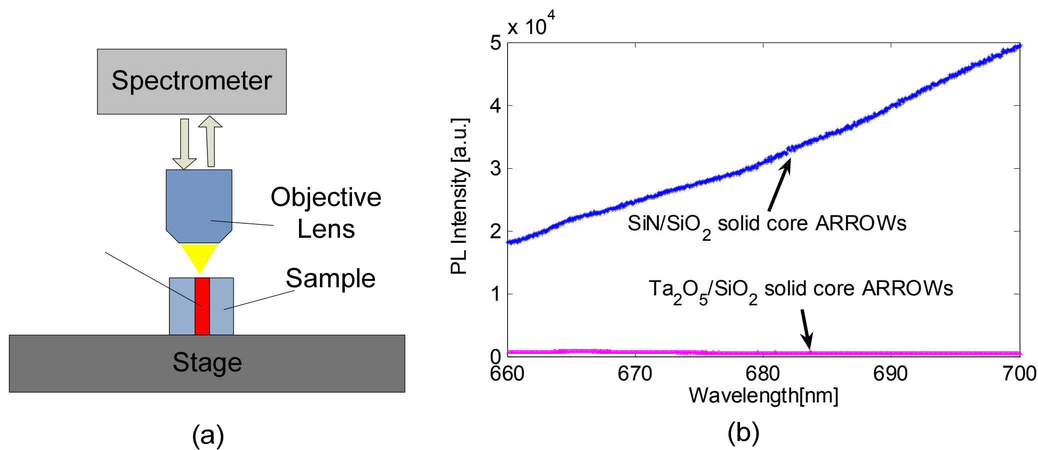


Figure 6-9: (a) Optical fluorescence setup and (b) the fluorescence comparison between SiO_2/SiN and SiO_2/Ta_2O_5 solid core waveguides

Next, SAP SOC ARROW chips with integrated hollow and solid core waveguides were tested with real fluorescing analytes in fluids. As Figure 6-10 illustrates, a 633 nm pump light of

3.3 mW emitted from a HeNe laser was coupled into the solid-core waveguides on an ARROW platform (Figure 2-13). The fluorescence signals generated at the excitation volume were collected via an objective lens (Olympus, NA=0.85). Spurious excitation photons were removed by collecting the fluorescence perpendicularly to the excitation direction and by optical filters (Semrock, 640nm long pass and 670±17nm bandpass) before coupling into an avalanche photodiode detector (APD, Perkin Elmer, SPCM-AQR-14-FC). The data were finally analyzed by using a time-correlated single photon counting card and software (Picoquant, Timeharp 200).

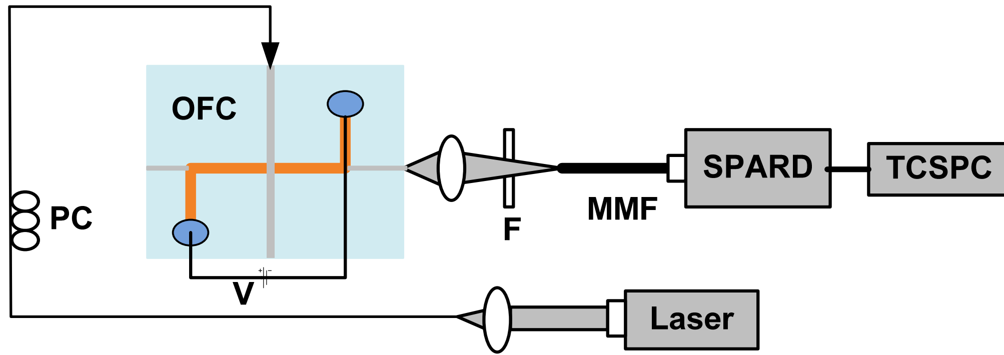


Figure 6-10: Optical fluorescence setup. OFC: optofluidic chip; F: filter; PC: polarization controller; MMF: multimode fiber; SPAPD: single-photon avalanche photodiode; TCSPC: time-correlated single-photon counting card; V: applied voltage between fluid reservoirs.

The PL intensity as a function of time from water filled (18MΩ-cm) SiN/SiO_2 and Ta_2O_5/SiO_2 ARROW chips are measured and compared in Figure 6-11. The liquid core channels were filled with water and the detector signal was recorded with laser off (t<10s) and laser on (10s<t<40s). The experimental results show that the background noise baseline above the detector dark counts of liquid core ARROWs is reduced by a factor of 10 when SiN films are replaced by Ta_2O_5 films. Note that the total optical throughput from chip edge to edge (through

both hollow and solid core waveguides) was approximately 10% for both types of ARROW chips.

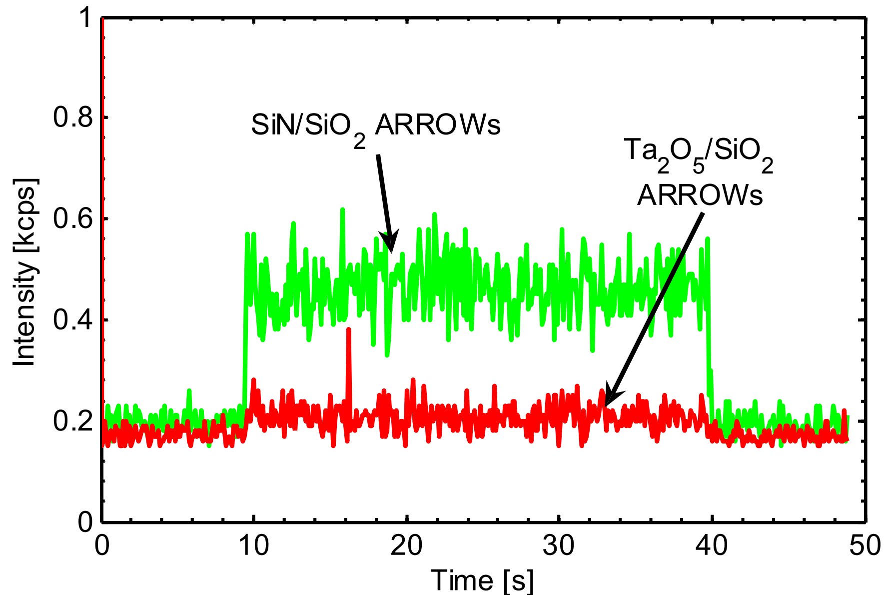


Figure 6-11: Comparison of fluorescence background signals between SiN/SiO_2 samples and Ta_2O_5/SiO_2 samples.

To characterize the SNR (detected signal divided by the standard deviation of the noise) of the devices, fluorescent nanoparticles (100nm diameter, Tetraspeck, Invitrogen) were introduced into the chip via the reservoir (Figure 6-10, 10μL). The particle concentration (1.8×10^{10} particles/mL) was chosen such that only one particle was detected in the device excitation volume (~85fL using $1/e^2$ beam diameters). The particles traveled down the channel using pressure driven flow and were optically excited at the orthogonal hollow core/solid core interface. The particle fluorescence was then collected by the APD. The detected signals for SiN/SiO_2 and Ta_2O_5/SiO_2 devices are shown on Figure 6-12 (a) and (b) (over a 5 second span) respectively, where each spike corresponded to a detected nanoparticle. The device baseline and noise was clearly higher in Figure 6-12(b) than in Figure 6-12(c). Over a 40 second timeframe,

the number of detected particles for the Ta_2O_5/SiO_2 sample was 948, with an average SNR of 126.7. The number of detected particles for the SiN/SiO_2 ARROW sample was 53, with an average SNR of 10.3. In other words, the number of detected particles increased by a factor of 18 and the SNR improved by a factor of 12 by replacing SiN with Ta_2O_5 films. This improved material system allows for more sensitive measurements, including pushing detection limits down to the level of single fluorophores.

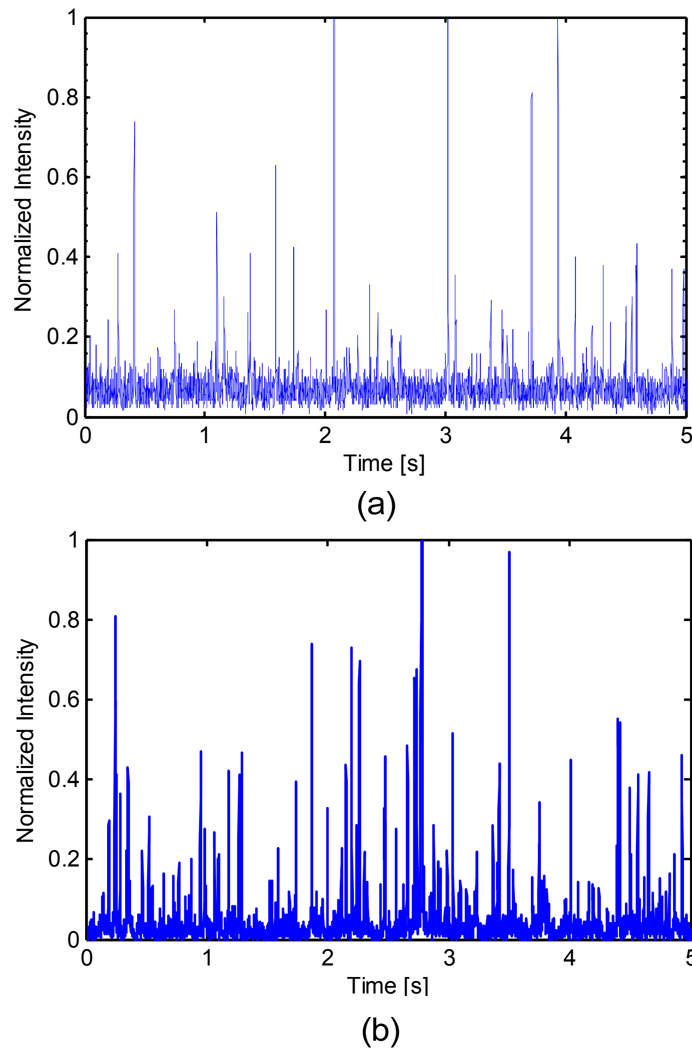


Figure 6-12: Fluorescence signals from excited Tetraspeck nanoparticles in the excitation volume on (a) SiN/SiO_2 ARROWs , (b) Ta_2O_5/SiO_2 ARROWs.

6.4 Post-deposition Annealed Films

As stated in Chaper 3, the PL intensity of TaO films in the red light wavelength regime mainly arises from the oxygen vacancies in TaO_x suboxides. As a result, the percentage of TaO_x is critical in determining the PL of TaO films. A great deal of research has been devoted to reducing TaO_x by after-deposition annealing [140-144].

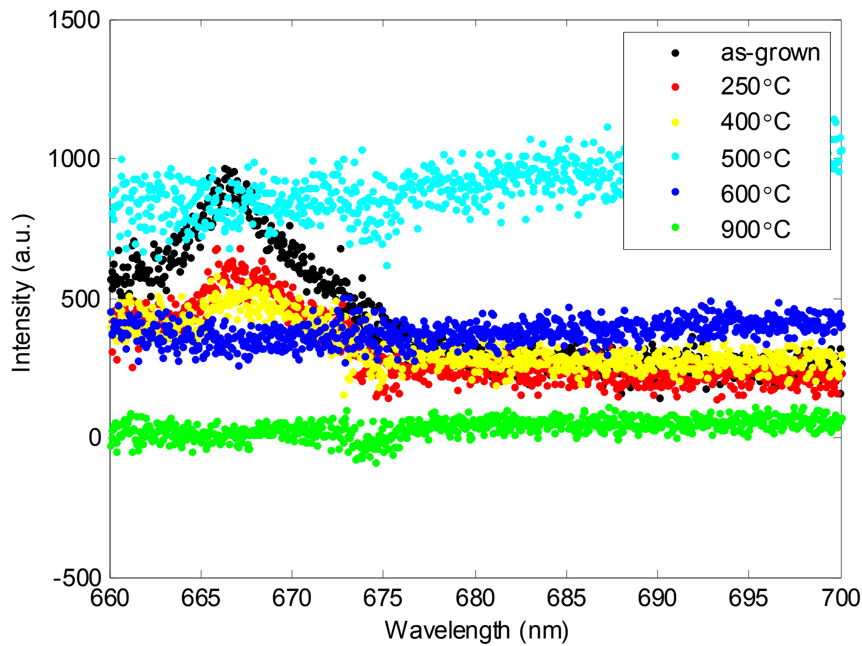


Figure 6-13: PL spectra of Ta_2O_5 samples annealed in N_2 at different temperatures

Considering the availability of equipment in our IML, annealing with N_2 in a furnace (Bruce Furnace) was the most easily conducted experiment in TaO PL reduction. Seven pieces from an as-deposited sample (sputtered TaO film ~150nm) were annealed in a N_2 environment at 250, 400, 500, 600, 700, 800, and 900˚C for 30 min using a furnace. Figure 6-13 compares the PL spectra of as grown and annealed Ta_2O_5 films at a wavelength range of 660nm to 700nm. It

shows that the as-grown amorphous TaO thin films exhibit visible-light emission having intensity peaks in the red-wavelength range (~667nm). This matches results previously reported before [85]. This peak gets smaller when the films were annealed, eventually disappearing when the annealing temperature is above 600˚C. It has reported that the peak actually shifts to a shorter wavelength range [145] and this makes Ta_2O_5/SiO_2 multilayered photonic crystals possible for active devices that efficiently emit blue light utilizing their photonic bandgaps and dispersion properties if annealed under proper conditions.

To clarify the effect of annealing on PL of Ta_2O_5 films, the PL intensity is shown in Figure 6-14 as the integral of the intensity in the range of 660~700nm for all the samples. The graph reveals that N_2 annealing helps to slightly decrease the PL intensity if the temperature is below 500˚C. The maximum intensity was obtained from the piece annealed at 500˚C. When the annealing temperature is above 700˚C, the PL intensity drops dramatically. The results demonstrated that the proper annealing temperature to obtain low PL intensity at 600nm~70nm is probably above 650˚C. The film probably changes from amorphous to the crystalline form [144, 146] at 500~600˚C.

Ta_2O_5 films annealed at temperature above 700˚C are very attractive based on the discussion above since they have very low PL intensity compared with as-deposited films. However, high temperature processes likely create stress problems due to the different thermal expansion coefficients of the thin film and the silicon substrate. Figure 6-15 illustrates the SEM images of annealed films in a N_2 environment. The film annealed under 700˚C looks very smooth, while 800˚C and 900˚C films have 'star-like' defects on the surfaces which make them unusable as cladding layers for ARROW waveguides. The roughness of the 700˚C film was measured to be ~1.08nm which is slightly high than as-deposited films (0.73nm). In conclusion,

the sputtered Ta_2O_5 film annealed under 700˚C can potentially be used to make ARROW waveguides with very low background noise while maintaining a low loss.

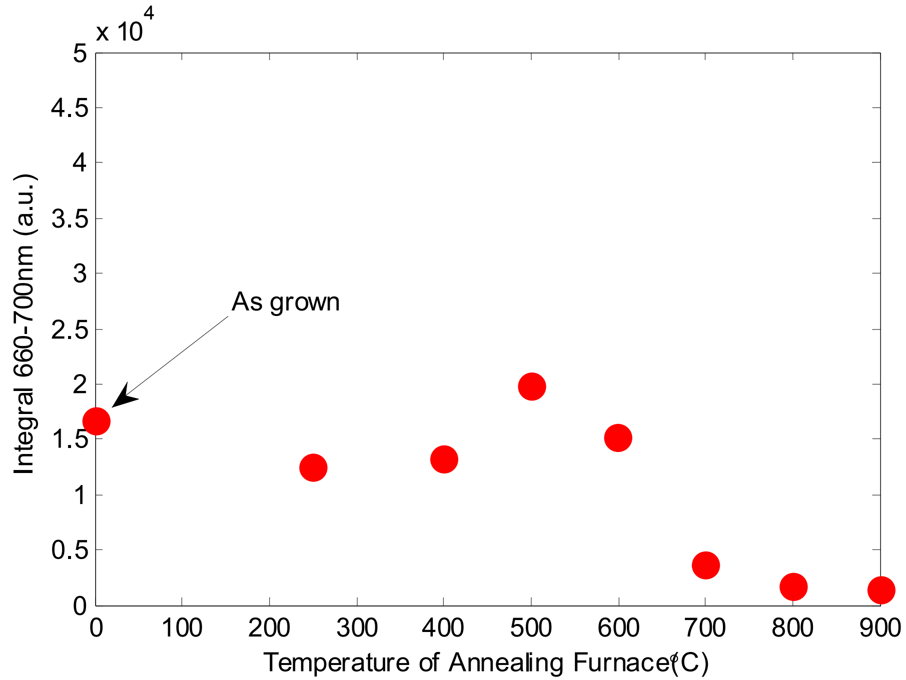


Figure 6-14: Integral PL Intensity of sputtered Ta_2O_5 films (T=250˚C) - as-grown and annealed at different temperatures

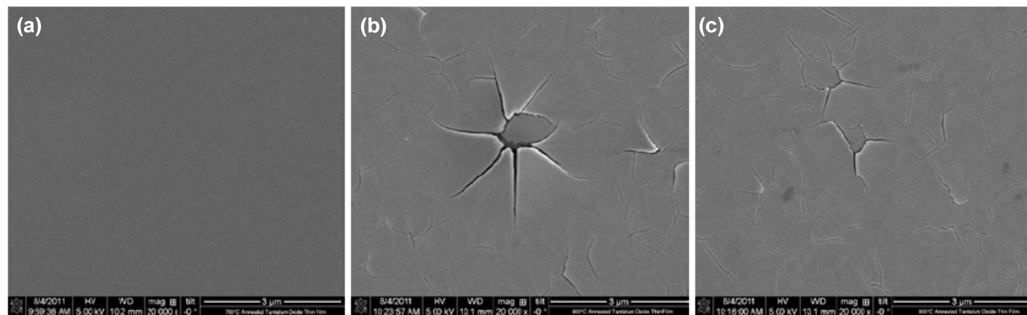


Figure 6-15: The SEM images of annealed films with N_2 under (a) 700˚C, (b) 800˚C, (c) 900˚C

6.5 Applications

Optofluidic devices can be applied to detect nucleic acid molecules towards the point of need or point-of-care (POC) as a method of infectious disease diagnosis [1]. The preferred method for nucleic acid testing (NAT) has been polymerase chain reaction (PCR) [147]. In PCR, pathogen-specific nucleic acid targets are amplified to a level that can be detected using fluorescence. However, PCR typically requires trained personnel, delicate reagents, reverse transcriptase for RNA detection, and precise temperature controls, thereby inhibiting POC NAT. More recently, efforts have been made to automate and miniaturize PCR and other nucleic acid amplification methods towards POC use [148]. But ultimately, the amplification step has been the time limiting factor which typically takes 1-4 hours. Recently, amplification-free pathogen optofluidic detection approaches have been investigated [1]. One approach to creating an ultrasensitive chip utilizes liquid-core antiresonant reflecting optical waveguides (ARROWs) [149].

One type of molecular probe that has shown both sensitive and specific detection of nucleic acids is a molecular beacon [150]. The specificity can be used to differentiate between single nucleotide mismatches (SNP) [151]. Molecular beacons consist of a nucleic acid strand specific to a complementary target strand (such as a particular infectious disease) with self-complementary regions at the end to form a hairpin structure (Figure 6-16(c), top). At the ends of the strand a fluorescent dye, D, and quencher, Q, is attached so that when unbound, D remains close to Q so that non-radiative energy exchange is dominant and no fluorescence is seen when excited (Figure 6-16(c), top). However, when bound to the target strand, D is far away from Q so that fluorescence is not quenched and the structure is bright when excited (Figure 6-16(c), bottom).

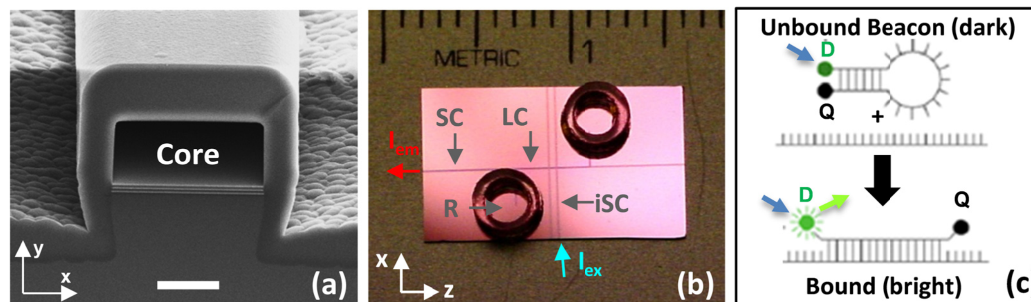


Figure 6-16: (a) Scanning electron microscope image of a hollow-core ARROW cross-section (scale-bar 5µm), (b) photo of an optofluidic chip showing the liquid-core ARROW (LC), solid-core ARROW (SC), intersecting solid-core ARROW (iSC), liquid reservoir (R), excitation light (I_{ex}) and emission light (I_{em}), (c) function of a molecular beacon when unbound (top) and bound (bottom) to a target nucleic acid strand with a dye, D, and quencher, Q on the ends.

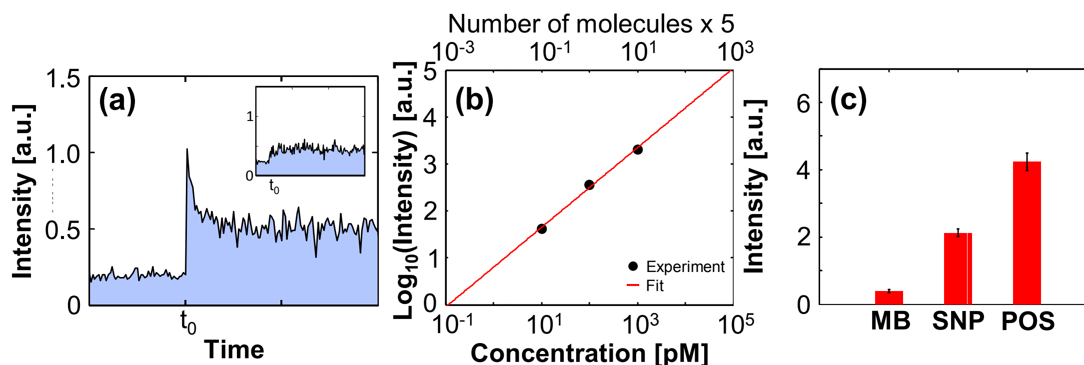


Figure 6-17: (a) Fluorescence signal from hybridized molecular beacons and target HPV-18 strand at 10pM (inset: TE buffer background), (b) concentration series of target HPV-18 strand hybridized to molecular beacons (10-1000pM), (c) signal level for molecular beacons only (MB), target with a single mismatched sequence (SNP) and an exact matching sequence (POS) at 10nM.

After fabricating a platform with optimized fabrication and materials (see cross section in Figure 6-16(a)), the limit of detection of the device was determined by introducing molecular beacons hybridized to target strands into the liquid core via the reservoir. The beacons were specifically designed to detect HPV-18, one major cause of cervical and head/neck cancers, in the L1 protein region (responsible for viron capsid formation and indicative of a late phase

infection). The beacons were hybridized to the complementary strand at 70 °C in a thermal cycler prior to chip introduction.

The signal at the lowest concentration (10pM) is shown on Figure 6-17(a) and the corresponding TE buffer background is shown on the inset. The laser is initially off and is turned on at t_0 where the optical signal is detected and eventually decays to the background due to photobleaching. As can be seen, a SNR~2 is achieved even at the lowest concentration and the signal linearly increases to 1nM (Figure 6-17(b)). The corresponding average number of molecules is shown at the top scale of figure 2b which shows the signal from an average of 50 molecules to the single-molecule detection level (an average of ~0.5 molecules in the excitation volume of ~80fL).

In order to assess the specificity of the HPV-18 molecular beacon assay, the observed signal was measured when only molecular beacons were present (Figure 6-17(c), MB), when the exact positive target strand was present (Figure 6-17(c), POS) and when a target strand with a single nucleotide mismatch was present (Figure 6-17(c), SNP). As can be seen, the POS signal can be differentiated from the SNP signal.

In conclusion, we have demonstrated, for the first time, highly specific nucleic acid detection at the single molecule level on a planar, optofluidic chip. This was achieved without nucleic acid amplification, reverse transcription and antibodies exemplifying a promising platform for infectious disease detection.

7 CONCLUSION

7.1 Conclusions

In conclusion, this dissertation describes research on the microfabrication and optimization of a type of optofluidic sensing chip based on intersecting hollow core and solid core ARROW waveguides. The overall objective of the research was to develop a low cost, high sensitivity, and high yield fabrication process for ARROW based sensor platforms.

Hollow waveguides used in this work have been made with PECVD or sputtered films. Initial experiments replaced PECVD with sputtering as a deposition method to produce antiresonant coatings for hollow channels. Several aspects of the fabrication processes were explored, including sputtering process and etching characteristics of the sacrificial core materials. Purely sputtered layers were found not to be suited for hollow core waveguides with small dimensions because the layers had poor adhesion and mechanical strength (discussed in Chapter 5).

To improve the throughput of ARROW sensing platforms, the reasons behind the low transmission at solid-to-liquid core interfaces were explored. Simulations were optimized to include actual profiles during the fabrication processes and ARROW devices were created that had more than 2× improvement in interface transmissions with optimized design (discussed in Chapter 4).

The PL intensities for SiO_2, Si_3N_4 and Ta_2O_5 were investigated in order to find out ideal material systems for ARROW sensing platforms with low background noise. Sputtered Ta_2O_5 was targeted as an ideal replacement for Si_3N_4 because of its very low PL intensity at interesting wavelength range. To utilize films with low background noise and build a robust structure, hybrid layers including sputtered Ta_2O_5 and PECVD SiO_2 were used to form claddings for ARROW waveguides, resulting in successful integrated ARROW chips with intersecting hollow and solid core waveguides. An optimized structure was also studied, which used ARROW waveguides with a self-aligned pedestal beneath the cores and only one top thick oxide over the cores. This structure proved to have lower loss, higher fabrication yield, and higher interface coupling efficiency than planar ARROWs described in Chapter 3. By applying this SAP SOC structure and hybrid layers as claddings, we produced an ARROW sensing chip was produced with 10% throughput and over 90% yield. The background noise was reduced by 10× and the signal-to-noise ratio for fluorescent nanobead detection was improved by a factor of 12 (discussed in Chapter 6).

7.2 Future Work

Given the work described in this dissertation, there are many possible paths that could improve the performance of the integrated ARROW platforms. First, the fabrication processes described in this dissertation have potential for improvement. Not only sputtered films but also PECVD films have technical issues including stress, roughness, and comformality that lead to device failure or suboptimal performance. Future work could be done to optimize those properties by design of experiments and recipe adjustments. There are also some common issues that need to be improved during the dry etching process, such as contamination in the chamber,

burning of the etch mask (photoresist), grass and residue problems, etc. Wet etching is also a possible alternative to dry etching method to produce a self-aligned pedestal in the future work.

Second, more work could be done to decrease the noise that decreases the overall signal-to-noise ratio of the ARROW detection platform during single particle fluorescence detection. One possible approach is to achieve proper annealing conditions for sputtered Ta_2O_5 film to further suppress the PL intensity at 660~700nm. Other related methods which can be accomplished in the future include smaller excitation volumes, shorter ARROW waveguides, and smaller distances between the excitation volume and avalanche photodetectors.

It is also very important to improve the optical throughput of ARROW sensing chips in the future. This is especially true when measuring particles with small dimensions, for example nucleic acids. A new design with 6 instead of 3 pairs of antiresonant layers has been shown in simulation to decrease TM loss within the hollow core. Recently, we have realized that the optimal polarization to detect single molecules on our ARROW sensing platforms is not x-polarization but y-polarization. This is due to the fact that we are detecting at an orthogonal geometry instead of a parallel one and the direction of the excited dipole is in the direction of the excitation. We expect that adding more claddings and increasing the core height can decrease the TM loss and more single nucleic acids can be detected. The fabrication of ARROW waveguides with this new design has initiated and the effects of this modification will be verified in the future.

In addition, further integration of additional optical elements such as light sources, filters, and detectors is possible, yielding biomedical sensors that are compact, portable and fast, and possess single molecule sensitivity at moderate cost. One possible layout for ARROW based chips for chemical analysis and DNA sequencing is shown in Figure 7-1.

Last, the fabrication process developed in this work is not limited to ARROW waveguides. It can potentially be used for making other types of micro-channels or nano-

channels, which have a large variety of applications such as heat transfer, cooling system, chemical test platforms, etc.

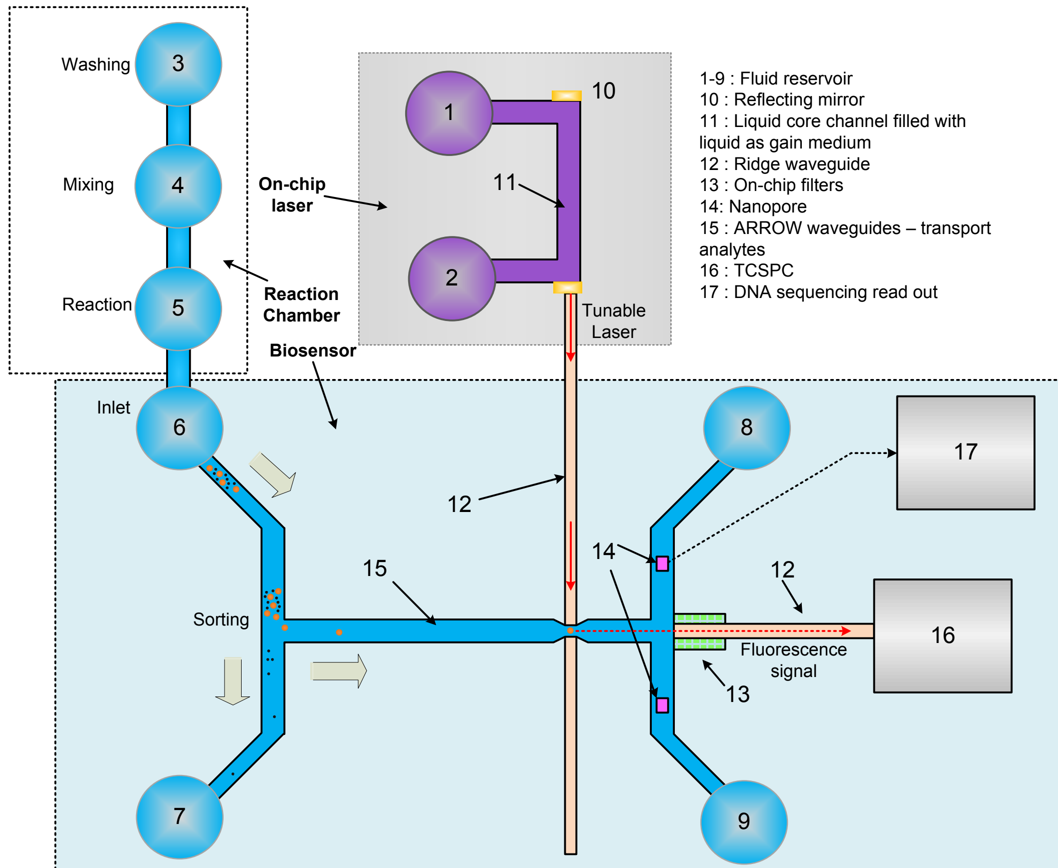


Figure 7-1: An example design of an ARROW-based platform with integrated laser source, filter, and biosensor.

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APPENDIX A. LIST OF PUBLICATIONS

A.1 Referreed Journal Publications

[1] **Y. Zhao**, B. S. Philips, D. Ozcelik, P. Measor, J. Parks, D. Gulbransen, H. Schmidt, and A. R. Hawkins, "Tailoring the spectral response of liquid waveguide diagnostic Platforms," *Journal of Biophotonics*, In process, 2012.

[2] **Y. Zhao**, K. D. Leake, P. Measor, M. H. Jenkins, J. Keeley, H. Schmidt, and A. R. Hawkins, "Optimization of Interface Transmission between Integrated Solid Core and Optofluidic Waveguides," *Photonics Technology Letters, IEEE,* vol. 24, pp. 46-8, 1 Jan 2012.

[3] **Y. Zhao**, M. Jenkins, P. Measor, K. Leake, S. Liu, H. Schmidt, and A. R. Hawkins, "Hollow waveguides with low intrinsic photoluminescence fabricated with Ta_2O_5 and SiO_2 films," *Appl Phys Lett,* vol. 98, p. 91104, Feb 28 2011.

[4] M. H. Jenkins, B. S. Phillips, **Y. Zhao**, M. R. Holmes, H. Schmidt, and A. R. Hawkins, "Optical Characterization of Optofluidic Waveguides Using Scattered Light Imaging," *Opt Commun,* vol. 284, pp. 3980-3982, Aug 1 2011.

[5] B. S. Philips, P. Measor, **Y. Zhao**, H. Schmidt, and A. R. Hawkins, "Optofluidic notch filter integration by lift-off thin films," *OPTICS EXPRESS,* vol. 18, pp. 4790-5, 1 March 2010.

A.2 Book Chapter

[1] Y. Zhao, "Chapter 2: Microfabrication," in *Handbook of Optofluidics*, A. R. Hawkins and H. Schmidt, Eds., ed Boca Raton, FL: CRC Press, 2010, pp. 2:1-39.

A.3 Conference Papers and Presentations

[1] P. Measor, **Y. Zhao**, A. R. Hawkins, and H. Schmidt, "An Ultrasensitive Optofluidic Nucleic Acid Biosensor," presented at the CLEO, San Jose, CA, 2012.

[2] **Y. Zhao**, M. Jenkins, K. Leake, S. Liu, P. Measor, H. Schmidt, and A. R. Hawkins, "Optofluidic Waveguides with Ta_2O_5 Cladding Layers and Low Photoluminescence," presented at the CLEO:Science and Innovations, Baltimore, MD, 2011.

[3] P. Measor, B. S. Philips, **Y. Zhao**, A. R. Hawkins, and H. Schmidt, "Selectively Patterened Notch Filter Waveguides for Optofluidic Biosensors," presented at the Integrated Photonics and Nanophotonics Research and Applications (IPNRA), Honolulu, Hawaii, 2009.

[4] B. S. Philips, **Y. Zhao**, P. Measor, H. Schmidt, and A. R. Hawkins, "Selective Deposition of Thin Films for Integrated Notch Filters in Optofluidic Sensors," presented at the OSA 93rd Annual Meeting, San Jose, CA, 2009.

[5] **Y. Zhao**, E. Lunt, D. Yin, H. Schmidt, and A. R. Hawkins, "Integrated hollow-core waveguides made by sputter deposition," presented at the Integrated Photonics and Nanophotonics Research and Applications (IPNRA), Salt lake city, UT, 2007.

APPENDIX B. PROCESS RECIPES

B.1 Introduction

This Appendix lists the process recipes used in the fabrication of ARROW waveguides described in this dissertation. This included recipes for photolithography, PECVD/sputter film deposition, dry etching (Trion and Anelva) and wet etching process for ARROW based structure.

B.2 Photolithography

B.2.1 SPR220 Sacrificial Core

1. O_2 plasma descum, 100w, 90s
2. Dehydration bake - in clean oven, 15 min, 150 ˚C
3. Vapor coat HMDS, 5 min in closed plastic box
4. Apply SPR220
   (a) Pour big puddle (cover half of the wafer)
   (b) Spin: 3650 rpm @ 3000/s, 60s
5. Soft bake - hotplate bake, 115˚C, 1 min;
6. Expose - 27 s (south aligner - constant intensity, hard contact), 10 mW/cm2
7. Develop
   (a) Immerse in MF-24A developer and agitate, 2 min
   (b) Rinse with DI water, nitrogen dry
8. Descum - PE2, 60 s, 50 W, 100 sccm O_2

9. Hard bake - ramp on hotplate from RT to 130˚C, bake 20 min, cool down to RT

B.2.2 SU-8 10 Sacrificial Core

1. O_2 descum, 100w, 90s
2. Dehydration bake - in clean oven, 15 min, 150 ˚C
3. Apply SU-8 10
   (a) Pour small puddle (about quarter size)
   (b) Spin: 500 rpm @ 100/s, 6 s; See see Table A.1 @ 1200/s, 60 s; 6000 rpm @ 6000/s, 2 s
4. Soft bake
   (a) Hotplate bake - 65˚C, 10 min
   (b) Ramp to 95˚C, bake 10 min
   (c) Cool to 65˚C on hotplate, cool to RT
5. Expose – see Table A.1 (south aligner - hard contact), 7.3 mW/cm2
6. Post exposure bake (PEB)
   (a) Hotplate bake - 65˚C, 5 min
   (b) Ramp to 95˚C, bake 5 min
   (c) Cool to 65˚C on hotplate, slowly cool to RT
7. Develop
   (a) Immerse in SU-8 developer and agitate 1-2 min
   (b) Rinse with IPA, nitrogen dry
8. Hard bake
   (a) Ramp on hotplate from RT to 200˚C, 10 min
   (b) Ramp down to 65˚C

9. Descum - PE2, 90 s, 40 W, 100 sccm O_2
10. Hard Bake
    (a) Ramp on hotplate from RT to 250˚C, bake at 250˚C, 5 min
    (b) Ramp down to 65˚C

Table A.1 SU8 Recipes for ARROWs with Different Targeted Heights

	Target Height (μm)	*Spin Speed (RPM)*	*Exposure (s)*	*Lamp Intensity (mw/cm^2)*
Sacrificial core	5	4350	20.5	7.3
	6	3600	26.5	7.3

B.2.3 SU-8 10 Ridge Etch Mask

1. O_2 descum, 100w, 90s
2. Dehydration bake - in clean oven, 15 min, 150 ˚C
3. Apply Omnicoat
    (a) Spin: 5000 rpm @3000/s, 60s
    (b) Hot plate, 200˚C, bake 60s
4. Apply SU-8 10
    (a) Pour small puddle (about quarter size)
    (b) Spin: 500 rpm @ 100/s, 6 s; 600 rpm @ 1200/s, 60 s; 6000 rpm @ 6000/s, 2 s
5. Soft bake
    (a) Hotplate bake - 65˚C, 10 min
    (b) Ramp to 95˚C, bake 10 min
    (c) Cool to 65˚C on hotplate, cool to RT
6. Expose – 23s (south aligner - hard contact), 7.3 mW/cm^2

7. Post exposure bake (PEB)
    (a) Hotplate bake - 65˚C, 5 min
    (b) Ramp to 95˚C, bake 5 min
    (c) Cool to 65˚C on hotplate, slowly cool to RT
8. Develop
    (a) Immerse in SU-8 developer and agitate 1-2 min
    (b) Rinse with IPA, nitrogen dry
9. Hard bake
    (a) Ramp on hotplate from RT to 180˚C, 15 min
    (b) Ramp down to 65˚C
10. Descum - PE2, 90 s, 50 W, 100 sccm O_2

B.2.4 AZP4620 for Ni liftoff- SAP

1. Dehydration bake - in clean oven, 15 min, 150 ˚C
2. Apply AZP4620
    (a) Pour big puddle (about silver-dollar size)
    (b) Spin: 2800 rpm @ 1100/s, 30s; 6000 rpm @ 6000/s, 2s
3. Soft bake - hotplate, 70˚C, 1 min; 100˚C, 1 min; 120˚C, 25s (separate hotplates)
4. Relax - sit at room temperature, 5 min
5. Exposure-55 s (south aligner - constant intensity), 7.3 mW/cm^2
6. Flood expose - 5 s (south aligner - constant intensity), 7.3 mW/cm2
7. Develop
    (a) Immerse in 400K 1:4 developer and agitate, 2-3 min
    (b) Rinse with DI water, nitrogen dry

8. Descum - PE2, 30 s, 50 W, 100 sccm O_2 (Best height: 2.8~3.5μm)
9. E-beam deposition – planetary position, 74~85 nm Ni at 1.5 A /s
10. Remove photoresist and liftoff Ni
    (a) Acetone soak, 10 min
    (b) IPA rinse, nitrogen dry
11. Descum - PE2, 30 s, 50 W, 100 sccm O_2

B.2.5 AZP4620 Etching Mask for Core Expose

1. Dehydration bake - in clean oven, 15 min, 150 ˚C
2. Apply AZP4620
    (a) Pour big puddle (about silver-dollar size)
    (b) Spin: 700 rpm @ 1100/s, 30s; 4000 rpm @ 6000/s, 2s
3. Soft bake - hotplate, 70˚C, 1 min; 100˚C, 1 min; 120˚C, 25s (separate hotplates)
4. Relax - sit at room temperature, 5 min
5. Exposure-55 s (south aligner - constant intensity), 7.3 mW/cm^2
6. Develop
    (a) Immerse in 400K 1:4 developer and agitate, 4-6 min
    (b) Rinse with DI water, nitrogen dry
7. Descum - PE2, 30 s, 50 W, 100 sccm O_2
8. Hard Bake
    (a) Hard bake - Ramp on hotplate from RT to 125˚C, 15 min
    (b) Ramp down to 50˚C
9. Apply the steps from 1-10

B.3 PECVD Deposition

Table A-2. PECVD SiO_2 Deposition Recipes for ARROW Waveguides.

	Pressure (mTorr)	*Power (w)*	*Gas (sccm)*			*Conformality Ratio*	*Variation*	*Growth Rate (nm/min)*
			SiH_4/He	*N_2O*	*CF_4/O_2*			
SiO_2	600	19.5	119	34		1.7	2%	45
	1100	23	132	9		1.4	7%	35
Clean	600	91			100			

Table A-3. PECVD SiN Deposition Recipes for ARROW Waveguides.

	Pressure (mTorr)	*Power (w)*	*Gas Flow(sccm)*		*Growth Rate (nm/min)*
			SiH_4/He	*NH_3*	
SiN	1000	100	104	6	8~9

B.4 Sputter

Table A-4 Recipes for Sputter SiO_2, Si_3N_4 and Ta_2O_5

	Argon Pressure (mTorr)	*Gas Flow (sccm)*	*Temperature (°C)*	*RF Power (w)*	*Deposition Rate (nm/min)*
SiO_2/Si_3N_4	5	88.5	RT~250	300	5~6
Ta_2O_5	5	88.5	RT~250	120	5~6

B.5 Dry Etch

Table A-5: Plasma Etching Recipes for SAP ARROWs Using the Trion ICP

Recipe		*ICP (w)*	*RIE (w)*	*Pressure (mTorr)*	*Gas Flow (sccm)*		*Etching Rate (nm/s)*
					SF_6	CHF_3	
	SiO_2(PECVD)	350	70	18	0	125	1.5
	Ta_2O_5(sputter)						0.47
Si	Passivation (20s)	550	0	120		75	
	Etch (11s)	550	60	35	20	30	
	Isotropic Si etch	0	200	150	50		varies

Table A-6: Plasma Etching Recipes for Ridge Etch and Core Exposure Step Using the Trion ICP

Recipe	*ICP (w)*	*RIE (w)*	*Pressure (mTorr)*	*Gas Flow (sccm)* CF_4	*Etching Rate (nm/s)* O_2
SiO_2(PECVD) Ta_2O_5(sputter)	550	75	12	50	5.5 1.7

APPENDIX C. ARROW WAVEGUIDE DESIGNS

C.1 Rectangular Core Ta_2O_5/SiO_2 (RT1) ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	1.385	0.095	0.277	0.095	0.277	0.095
n	3.85	1.467	2.245	1.245	2.245	1.467	2.245

ARROW Top Layer Design

Layer	Hc	T4	O4	T5	O5	T6	TO	d_r
t [μm]	5.0	0.190	0.277	0.190	0.277	0.190	H-2.248	TO/2
n	1.33	2.245	1.467	2.245	1.467	2.245	1.467	-

C.2 Rectangular Core Ta_2O_5/SiO_2 (RT2) ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	1.230	0.082	0.277	0.082	0.277	0.082
n	3.85	1.467	2.485	1.467	2.485	1.467	2.485

ARROW Top Layer Design

Layer	Hc	T4	O4	T5	O5	T6	TO	d_r
t [μm]	5.0	0.133	0.277	0.133	0.277	0.133	H-1.906	TO/2
n	1.33	2.485	1.467	2.485	1.467	2.485	1.467	-

C.3 Rectangular Core Ta_2O_5/SiO_2 (RT2V2) ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	1.385	0.106	0.277	0.106	0.277	0.106
n	3.85	1.467	2.10	1.467	2.10	1.467	2.10

ARROW Top Layer Design

Layer	Hc	T4	O4	T5	O5	T6	TO	d_r
t [μm]	5.0	0.212	0.277	0.212	0.277	0.212	H-2.380	TO/2
n	1.33	2.10	1.467	2.10	1.467	2.10	1.467	-

C.4 Rectangular Core Ta_2O_5/SiO_2 (RT3) ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	1.385	0.093	0.281	0.093	0.281	0.093
n	3.85	1.467	2.3	1.467	2.3	1.467	2.3

ARROW Top Layer Design

Layer	Hc	T4	O4	T5	O5	T6	TO	d_r
t [μm]	5.0	0.158	0.277	0.158	0.277	0.158	H-2.072	TO/2
n	1.33	2.3	1.467	2.3	1.467	2.3	1.467	-

C.5 Rectangular Core Ta_2O_5/SiO_2 (TSAP1p) SAP SOC ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	0.227	0.077	0.227	0.077	0.227	0.077
n	3.85	1.461	2.3	1.461	2.3	1.461	2.3

ARROW Top Layer Design

Layer	Hc	TO	d_r
t [μm]	5.0	5.5	TO/2
n	1.33	1.461	-

C.6 Rectangular Core Ta_2O_5/SiO_2 (TSAP2p) SAP SOC ARROW Design

12 Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	0.265	0.102	0.265	0.102	0.265	0.102
n	3.85	1.47	2.107	1.47	2.107	1.47	2.107

Layer	O4	T4	O5	T5	O6	T6
t (μm)	0.265	0.102	0.265	0.102	0.265	0.102
n	1.47	2.107	1.47	2.107	1.47	2.107

C.7 Arch Core Sputtered Si_3N_4/SiO_2 ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	0.336	0.112	0.336	0.112	0.336	0.112
n	3.85	1.41	1.94	1.41	1.94	1.41	1.94

ARROW Top Layer Design

Layer	Hc	T4	O4	T5	O5	T6	TO	d_r
t [μm]	6.0	0.112	0.336	0.112	0.336	0.112	4.0	TO/2
n	1.33	1.94	1.41	1.94	1.41	1.94	1.41	-

C.8 Arch Core Sputtered Ta_2O_5/SiO_2 ARROW Design

Bottom ARROW Layers

Layer	Si	O1	T1	O2	T2	O3	T3
t (μm)	500	0.301	0.084	0.301	0.084	0.301	0.084
n	3.85	1.426	2.3	1.426	2.3	1.426	2.3

ARROW Top Layer Design

Layer	Hc	T4	O4	T5	O5	T6	TO	d_r
t [μm]	6.0	0.084	0.301	0.084	0.301	0.084	4.0	TO/2
n	1.33	1.426	2.3	1.426	2.3	1.426	1.426	-