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A Design Basis for Composite Cascode Stages Operating in the Subthreshold/Weak Inversion Regions

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ABSTRACT

A Design Basis for Composite Cascode Stages Operating
in the Subthreshold/Weak Inversion Regions

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Composite cascode stages have been used in operational amplifier designs to achieve ultra-high gain at very low power. The flexibility and simplicity of the stage makes it an appealing choice for low power op-amp designs. Op-amp design using the composite cascode stage is often made more difficult through the lack of a design process. A design process to aid in the selection of the MOSFET dimensions is provided in this thesis. This process includes a table-based method for selection of the widths and lengths of the MOSFETs used in the composite cascode stage. Equations are also derived for the gain, bandwidth, and noise of the composite cascode stage with each of the devices operating in the various regions of inversion.

Keywords: composite cascode, weak, moderate, strong, subthreshold, inversion level, low power operation, high gain, low frequency, low noise

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NOMENCLATURE

$\alpha_{[n]}$	Constant used in the calculation of $g_{DS[n]}$ for the MOSFET n.
ε_0	Permittivity of free space $(8.854 * 10^{-14} \frac{F}{cm})$
ε_S	Epsilon coefficient for SiO_2 (3.9 for C5X)
ε_{SiO2}	The permittivity of the SiO_2 layer $(\varepsilon_S * \varepsilon_0)$
γ	The body effect constant
ϕ_f	The flatband voltage of a MOSFET.
μ	The electron (n) or hole (p) mobility of an N-Type or P-Type MOSFET respectively.
A_{MB}	The midband gain of the system, $\frac{V_{OUT}}{V_{IN}}$.
C_{OX}	The capacitance of the oxide layer given by $\frac{\varepsilon_{SiO_2}}{t_{OX}}$.
$g_{DS[n]}$	Channel conductance of the MOSFET n.
$g_{M[n]}$	Transconductance of the MOSFET n.
$g_{MB[n]}$	Body effect of the MOSFET n.
gnd	Ground.
H_n	The height of the MOSFET n.
$I_{0[n]}$	The technology current of MOSFET n.
$IC_{[n]}$	The inversion coefficient of MOSFET n.
$I_{D[n]}$	Drain current through the nth column in the system.
k	Boltzmann's constant $(1.381 * 10^{-23} \frac{J}{K})$.
$k(L)_{[n]}$	Coefficient used in calculating $g_{DS[n]}$ for the MOSFET n.
$L_{[n]}$	The length of MOSFET n.
L_{OV}	The length of the overlap between the gate and the source.
m	A multiplier used in composite cascode load design.
n	The substrate factor used to account for deviations in I_0 due to substrate effect.
q	Charge of an electron $(1.6022 * 10^{-19} C)$
T	Temperature in kelvin (300 K for room temperature)
t_{OX}	The thickness of the oxide layer.
U_T	Thermal voltage given by the equation $\frac{kT}{q}$.
$V_{A[n]}$	Early voltage on the MOSFET n.
$V_{BIAS[n]}$	Bias voltages numbered 1 - n.
$V_{D[n]}$	Drain voltage on the MOSFET n.
V_{DD}	Positive supply rail.
$V_{DS[n]}$	Drain to source voltage on the MOSFET n.
$V_{E[n]}$	Early voltage factor for MOSFET n $(\frac{V_A}{L})$
V_{EE}	Negative supply rail.
$V_{G[n]}$	Gate voltage on the MOSFET n.
$V_{GS[n]}$	Gate to source voltage on the MOSFET n.
V_{IN}	Input AC voltage to the system.
$V_{S[n]}$	Source voltage on the MOSFET n.
$V_{SB[n]}$	Source to body voltage on MOSFET n.
$V_{T[n]}$	Threshold voltage of the MOSFET n.
V_{T0}	Threshold voltage at $V_{SB} = 0$
$W_{[n]}$	The width of MOSFET n.

CHAPTER 1. INTRODUCTION

1.1 Purpose

Recent research in low-power biomedical instrumentation amplifiers has generated interest in gain stages that produce exceptional gain with very low current draw [1, 2]. Several operational amplifier designs have been successfully fabricated using the composite cascode stage as the main gain stage [3–7]. Although these systems produce very high gain with very little current draw, the design methods used tend to be vague and/or dependent on the Complementary Metal Oxide Semiconductor (CMOS) process used by the designer. In order to make the composite cascode stage more accessible to circuit designers, a design methodology is needed.

This thesis provides a straightforward design methodology that can be extended to many CMOS technologies available for fabrication. Compatibility across CMOS technologies is enhanced through the use of the *Inversion Coefficient* (*IC*). The desired operation of the stage can be established using the value of *IC* for each device in the composite cascode stage, then extended to the given technology with the desired current draw and process parameters. The methods presented here provide circuit designers with an engineering approach to the design of CMOS composite cascode gain stages.

1.2 Contributions

The two main contributions of this thesis are: a design methodology in which the value of *IC* can be used to establish the desired operation of the composite cascode stage and equations that have been derived to explain the operation of the composite cascode gain, bandwidth, and noise. These tools are to be used by a circuit designer in the beginning stages of ultra-low-power operational amplifier design in order to select the dimensions of the MOSFETs in the composite cascode stage. The gain, bandwidth, and noise of the composite cascode stage have been plotted

against the values of the inversion coefficient of the two devices in the stage. The equations for gain, bandwidth, and noise are also used in the design of composite cascode stages to accurately predict the overall behavior of the stage.

The design methods developed in this thesis are to be used in the design of ultra-low-power, high gain, low bandwidth operational amplifiers. Such applications may include biomedical instrumentation amplifiers, where high frequency signals are not a concern and high gain is needed to amplify the inherently low signal levels present in biomedical applications. The design methods presented in this thesis allow for a designer of low-power, high-gain systems to quickly and accurately establish the desired operation of the composite cascode stage.

1.3 Outline

This thesis is broken up into several chapters that build on one another to arrive at the final results. In Chapter 2 the background information is presented. This chapter explores the various equations and models used in the analysis of a typical MOSFET. The equations, theory, and models shown in this chapter are used in the remainder of the thesis. In Chapter 3, the composite cascode stage is introduced and discussed.

Chapter 4 discusses the gain of the composite cascode stage and how certain device parameters can be used to achieve the desired gain in the final circuit. Chapter 5 considers the bandwidth of the composite cascode stage. Chapter 6 presents a discussion on the major noise sources in the composite cascode stage. Several suggestions are also given for lowering the overall noise.

Finally, Chapter 7 wraps up each of the previous sections, discusses the operation of the composite cascode stage at higher or lower drain current, and presents an example design of a differential stage utilizing the design methodology.

CHAPTER 2. BACKGROUND

Low power biomedical instrumentation and sensing has become one of the fastest growing fields of research [8]. Bio-sensing applications provide medical personnel with a great deal of information useful in improving the lives of those they treat. However, many of these systems produce very low power signals which must be amplified to higher levels before they can be effectively used [1, 3, 4]. Since many of these systems are battery operated, low power amplification is a very important aspect of the overall amplifier design.

As a result of the interest in this field, much work has been done in ultra-low power operational amplifier design. This chapter discusses a small portion of the recent work that has been performed and where this thesis fits into the recent research. In addition to the background information, this chapter lists some of the equations that are used in later chapters.

2.1 Recent Research in Low Power Biomedical Amplifiers

In the last few years, several groups have presented their work in developing high-gain, low-power amplifiers, many of which are intended for biomedical or other low power applications [1, 3, 4, 9–15]. Many different techniques have been used to achieve the goals of high-gain ($> 80dB$) and low-power ($< 1mW$) amplifying systems. A few of the many design configurations available have been chosen and are briefly discussed here. These systems have used gain boosting designs or bulk driven MOSFETs to make these amplifying systems smaller, faster, and more power efficient.

When short channel devices are used in amplifying designs, the gain of the system is often reduced due to short channel effects. In order to overcome these effects, many of the recent designs have employed a gain boosting technique to improve the gain of the short channel devices. In [16], the active cascode is shown to be an effective method for boosting the gain from a MOSFET cascode configuration. The active cascode configuration is shown in Figure 2.1

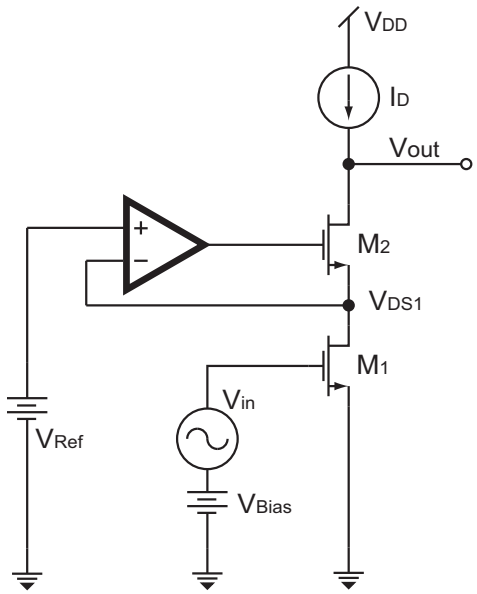

Figure 2.1: Active cascode configuration used to increase the cascode gain. Adapted from [16].

By applying negative feedback to the MOSFET M_2 through the differential amplifier, the voltage on the gate of M_2 can be held constant at V_{Ref}. This increases the impedance of M_2 which results in an increase in gain. Through the use of the gain boosted technique, low gain due to short channels can be overcome [9, 12, 16].

Operational amplifiers designed using the gain boosted technique suffer from several key limitations. First, the amplifiers used to drive the gate of M_2 must have a higher corner frequency than the overall bandwidth of the operational amplifier. If the f_{-3dB} corner of the driving amplifiers falls within the bandwidth of the overall amplifier, the gain is reduced. Also, instability may occur if the gain of the driving amplifier falls by too much [16]

In addition to general stability issues, other problems may arise when using the gain boosted cascode stage. The first problem is power consumption. Each gain stage in the amplifier requires a biasing operational amplifier or differential stage with a reference voltage. These amplifier and reference stages continuously draw current from the supplies resulting in excess power usage. In addition to lost power, the amplifier and reference stages can require a good amount of chip real estate. Higher power usage and chip real estate requirements may prevent the effective use of these amplifiers in low power biomedical applications.

Another method of improving the gain from MOSFET designs is by using a bulk driven technique. In these systems, the MOSFET is DC biased using the gate, with the signal being fed into the system through the bulk. An example cascode stage that utilizes this technique to improve the overall gain of the stage is shown in Figure 2.2.

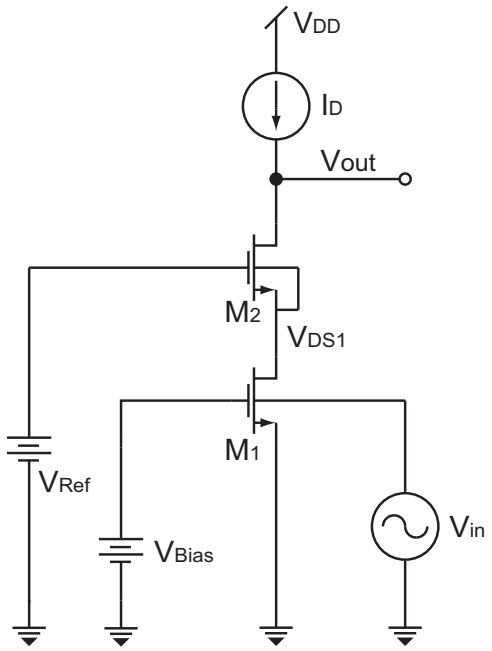

Figure 2.2: Bulk driven cascode configuration used to increase the cascode gain. Adapted from [15].

Many designs were compared in [15] with many of the bulk driven configurations achieving high gains at very low power due to lower headroom requirements. Power was also reduced due to the reduction of current through the biasing voltages into the gate of the MOSFET. However, the transconductance of a bulk driven MOSFET is typically much smaller than the transconductance of a gate driven device. This causes designs utilizing bulk driven devices to suffer from lowered gain and bandwidth. The gain and bandwidth of the operational amplifier shown in [15] compared to the overall gain and bandwidth shown in [9] and [12] is much smaller. Also, bulk driven devices require additional processing steps, as a well around the device must be formed in order to reduce leakage into the remainder of the bulk.

Finally, the composite cascode stages presented in [17–19] aim to combine the best features of both the bulk driven and gain boosted architectures. The composite cascode stage is shown in

Figure 3.2 and explained more fully in Chapter 3. Composite cascode gain stages are used in [4] and [19] to achieve open loop gains of $110dB$ and $120dB$ respectively. Although the unity gain bandwidth of these stages is very low, at $320kHz$ and $1.2MHz$ respectively, the power dissipation is very good. The operational amplifier proposed in [4] has a power dissipation of $27.6\mu W$.

By reducing the number of voltage references needed, the overall size of the composite cascode operational amplifier can be reduced. Also, since the gate of the device M_2 is tied to the bias voltage of M_1, similar effects to those seen in the gain boosting stages are seen in the composite cascode stage. The difficulty in using composite cascode stages is due to the process of selecting the widths and lengths of the MOSFETs in the gain stages. The width and the length of the devices set the overall behavior of the gain stages by simulating the drain to source behavior obtained in other configurations. In [4] and [19], the dimensions of the devices were chosen through a trial and error methodology until the desired gain was achieved. This thesis proposes a design methodology to enhance the use of composite cascode stages.

2.2 MOSFET Equations Used in this Thesis

Many textbooks and articles have discussed the modeling of MOSFETs across the various regions of inversion [20–23]. The complexity of these equations varies greatly as some provide general trends while others provide accurate modeling of the device behavior. In order to provide a solid foundation for the rest of this thesis, a short description of the equations used are given in this section.

2.2.1 Inversion Coefficient

In [20], D. M. Binkley presents a coefficient that can be used as an "at-a-glance" method for determining the inversion level of a MOSFET. The inversion coefficient (IC) of a device can be found by using

$$IC = \frac{I_D}{I_0 \frac{W}{L}}, \tag{2.1}$$

where I_D is the drain current through the device, W is the width of the device, L is the length of the channel, and I_0 is the technology current. The technology current is the intrinsic current through a MOSFET with a W/L ratio of 1, operating with an $IC = 1$. I_0 can be found by using parameters

that are dependent on the fabrication process. The equation used to solve for I_0 is

$$I_0 = 2\mu n C_{OX} U_T^2, \tag{2.2}$$

where μ is the carrier mobility of the MOSFET, n is a substrate factor, C_{OX} is the capacitance per unit area due to the oxide layer, and U_T is the thermal voltage of the silicon ($\approx 25.9mV$ at room temperature).

The relationship of IC to level of inversion can be seen in Figure 2.3. As the inversion coefficient increases, so does the level of inversion. At a value of $IC > 10$, the device is operating in the strong inversion region. An IC between 0.1 and 10 puts the device into the moderate inversion region, with 1 being the center of moderate inversion region. An $IC < 0.1$ is in the weak inversion region. If the value of IC falls even lower, the device may enter the subthreshold region, a subset of the weak inversion region where the channel has barely left the depletion region. If the value of IC is approximately 0.01 or less, the MOSFET has a good chance of operating in the subthreshold region.

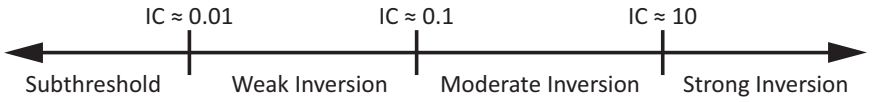

Figure 2.3: A plot showing the relationship of inversion level and inversion coefficient. Adapted from [20].

If the MOSFET fabrication parameters are known, as well as the desired drain current and operating region, the dimensions of the MOSFET can be found by rewriting equation (2.1) to solve for W/L. The resulting equation is

$$\frac{W}{L} = \frac{I_D}{I_0 IC}. \tag{2.3}$$

This function provides a quick method of device dimension selection. An important trend to observe is that as the inversion level increases, the width to length ratio of the MOSFET decreases. This means that longer lengths and shorter widths are common with higher values of IC. For low values of I_D, stronger inversion levels may even require channel lengths longer than channel widths to be fully biased into the strong inversion region. This behavior can be seen in Figure 2.4.

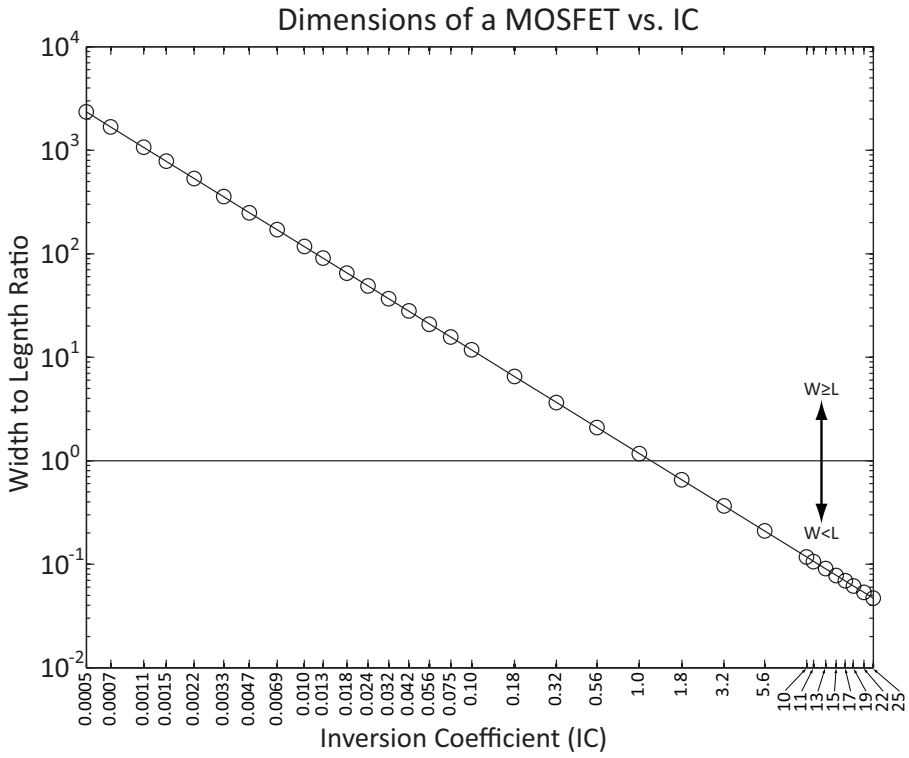

Figure 2.4: A plot showing the relationship of MOSFET dimension to the value of IC. The horizontal line shows where the ratio of width to length is unity for the ON Semiconductor C5X models operating at 200nA.

Subthreshold and Weak Inversion

The subthreshold and weak inversion region have become an important aspect of low power circuit design [18, 21, 23–26]. High voltage gain and low current draw are some of the most important features of the MOSFET operating in the subthreshold to weak inversion regions. A list of a few of the advantages and disadvantages for subthreshold to weak inversion operation found in some of the literature [21, 25] is given in Table 2.1.

An interesting behavior of MOSFETs operating in the subthreshold to weak inversion region is that they act very similarly to Bipolar Junction Transistors (BJTs) [18, 27]. The current carrying mechanisms in the subthreshold to weak inversion region are very similar to the mechanisms present in a BJT. This behavior can be used to obtain very high gain from the device at the cost of speed.

Table 2.1: Advantages and disadvantages resulting from operation in subthreshold to weak inversion region. Adapted from [21, 25].

Subthreshold and Weak Inversion Behavior		
	Short Channel	Long Channel
Advantages	Relatively High DC Voltage Gain Lowest Power Dissipation Low Harmonic Distortion Low Threshold Voltages Minimum $V_{GS} - V_T$ Minimum V_{DSAT} Small Thermal Noise	Highest DC Voltage Gain Low Power Dissipation Low Harmonic Distortion Simple Model Minimum Flicker Noise
Disadvantages	Relatively Slow Short Channel Effects	Slowest Higher Values of V_T Smaller Usable Weak Inversion Region

Strong Inversion

The strong inversion region is typically used in applications where speed is more important than power consumption or voltage gain [21, 25]. A list of a few of the advantages and disadvantages for operation in the strong inversion region is given in Table 2.2.

Table 2.2: Advantages and disadvantages resulting from operation in strong inversion. Adapted from [21, 25].

Strong Inversion Behavior		
	Short Channel	Long Channel
Advantages	Best Bandwidth (Fastest) Lower Threshold Voltage Minimum Capacitance Small Layout Area	Relatively Fast Relatively High Voltage Gain Lowest g_M Distortion Simple Model Small Thermal Noise
Disadvantages	Lowest Voltage Gain Short Channel Effects Higher Harmonic Distortion Mobility Degradation	Small Voltage Gain Highest Power Dissipation Highest Harmonic Distortion High Threshold Voltage

The MOSFET is often described as a square law device. This is due to the fact that the input value of V_{GS} is related to the output drain current by a power of α. For devices where the long channel approximation holds, $\alpha = 2$, relating the output of the device to the square of the input. As MOSFET fabrication techniques have improved, the length of the MOSFET channel has dropped. This has introduced many issues known as the short channel effects. The undesired effects of short channels are discussed later in this chapter.

Moderate Inversion

An increasing area of interest in low power MOSFET design is the moderate inversion region [21, 24, 25, 28–30]. Moderate inversion tends to combine some of the best features from the weak and strong inversion regions at the cost of simple and accurate design equations. However, as simulation software becomes better, and more accurate models are created, MOSFETs operating in the moderate inversion region are becoming standard in low power designs. A summary of a few of the advantages and disadvantages for operation in the moderate inversion region is given in Table 2.3.

Table 2.3: Advantages and disadvantages resulting from operation in moderate inversion. Adapted from [21, 25].

Moderate Inversion Behavior		
	Short Channel	Long Channel
Advantages	Good Voltage Gain Lower Threshold Voltage Relatively Low Power Smaller Layout Area	Better Voltage Gain Low Threshold Voltage Relatively Low Power Small Layout Area
Disadvantages	Low Bandwidth Short Channel Effects Complex Design Models	Lower Bandwidth Complex Design Models

A MOSFET operating in the moderate inversion region is in transition from weak to strong inversion. Added complexity is a major disadvantage to designs utilizing MOSFETs operating in

the moderate inversion region. However if higher performance is needed, the MOSFET operating in the moderate inversion region may be worth the added complexity.

2.2.2 Drain Current

Two equations are used to calculate the drain current of the MOSFET, one for the active (or saturation) region and one for the triode (or linear) region. The use of these equations is dependent on the "pinchoff condition" or the point where $V_{DS} \approx V_{GS} - V_T$. At this point the channel has formed and a small depletion region has separated the conducting channel from the drain. At $V_{DS} \ll V_{GS} - V_T$, the device is in the triode region. The drain current in the triode region is given in many texts as [17, 23, 31, 32]

$$I_D = \frac{\mu C_{OX} W}{nL} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]. \tag{2.4}$$

For the case when $V_{DS} \approx V_{GS} - V_T$ and $V_{DS} > V_{GS} - V_T$, the device is in the active region. A major challenge that arises in the design of systems with MOS devices in the active region, is the lack of a continuous and accurate drain current equation for all regions of inversion. A typical solution to this problem is to use the equation for the particular inversion region the device is operating in. However, since there is no simple equation for drain current in the moderate inversion region this solution is somewhat limited [20, 23]. An equation derived in [23] attempts to provide a function that holds throughout each of the regions of MOSFET inversion. This function is

$$I_D(WI - SI) = I_0 \frac{W}{L} \left\{ \left[ln\left(1 + e^{\frac{V_{GS} - V_T}{2nU_T}}\right) \right]^{\alpha} - \left[ln\left(1 + e^{\frac{V_{GS} - V_T - nV_{DS}}{2nU_T}}\right) \right]^{\alpha} \right\}. \tag{2.5}$$

2.2.3 Short Channel Effects

The active region drain current equation given in Equation (2.5), is very accurate for long channel approximations (channel length $\geq 2\mu m$). As fabrication techniques have improved, channel length has continued to shrink, allowing for more devices to be placed in a smaller area. However, smaller devices are prone to several short channel effects including drain induced barrier

lowering (DIBL), velocity saturation from the horizontal field, carrier mobility degradation, and threshold voltage rolloff [16, 27, 31, 32].

Many attempts have been made to accurately model the effects of short channel operation in MOSFETs. Some authors have created a table of MOSFET scaling rules that can be used to find out what the effects of scaling are [31,32]. Others have modified the equations for drain current and threshold voltage to account for the short channel effects [16,32]. Another method that can be used is to modify the power of the drain current equation (α) to be less than 2 for short channels [33]. Deviations in the active region can be easily accounted for if the value of α is lowered. In the case where the channel length is $1\mu m$, an $\alpha = 1.85$ can be used instead of $\alpha = 2$. The calculated current matches up with the simulated and measured current more accurately. As the channel continues to shrink, so does the value of α. For the $0.5\mu m$ process, α drops to about 1.5 and for the $0.18\mu m$ process α is closer to 1.08.

For simplicity in this thesis, the change in exponent is used. When shorter channels are used, the value of α is given. For longer channel devices, the long channel approximation holds, allowing the $\alpha = 2$ term to be used.

2.2.4 Active Region Small Signal Model

The small signal model of the MOSFET operating in the active region is given in Figure 2.5. There are four terminals to take into account on a typical MOSFET including the gate, drain, source, and body. Voltage potential between these four terminals change various internal parameters such as transconductance (g_M), body effect (g_{MB}), or channel conductance (g_{DS}).

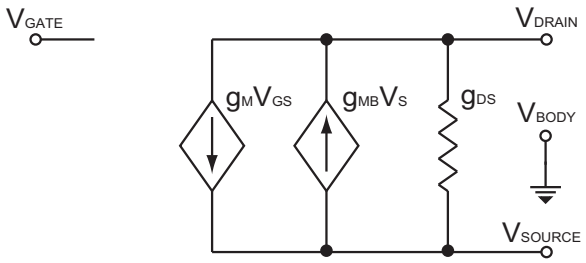

Figure 2.5: The MOSFET small signal equivalent circuit for the active region of operation.

The Active Region Transconductance

An important parameter when solving for the gain or impedance of an MOS device is transconductance. The transconductance specifies the capability of the MOSFET to convert gate to source voltage into drain current. The basic definition of the transconductance is the change in drain current with respect to the change in gate to source voltage with constant drain to source voltage or $g_M = \frac{\partial I_D}{\partial V_{GS}}$ [17, 31, 32]. In the active region the transconductance is

$$g_M = \frac{I_0 W \sqrt{IC}}{n U_T L} \frac{e^{\frac{V_{GS}-V_T}{2nU_T}}}{1+e^{\frac{V_{GS}-V_T}{2nU_T}}}. \tag{2.6}$$

The transconductance of the MOSFET is related to the $\sqrt{IC}$. As the value of IC increases, the ratio of width to length decreases. Since IC changes g_M as $\sqrt{IC}$ and width to length changes g_M as $\frac{W}{L}$, the value of g_M falls slowly with increasing inversion coefficient. If most of the parameters in Equation (2.6) are assumed to remain constant, this equation can be rewritten as

$$g_M = K \frac{W}{L} \sqrt{IC}, \tag{2.7}$$

to help visualize the value of g_M in terms of width, length, and IC. The behavior of g_M with changing IC is seen in Figure 2.6.

The Active Region Body Effect Parameter

If the source of a MOSFET is not tied to the same potential as the body, a small current flows into the body introducing the body effect. The body effect of an MOS device is the change in current due to the change in voltage potential from the source to body or $g_{MB} = \frac{\partial I_D}{\partial V_{SB}}$. In [27], the active region body effect parameter is

$$g_{MB} = \frac{\gamma g_M}{2\sqrt{V_{SB} + |2\phi_F|}}. \tag{2.8}$$

As can be seen in equation (2.8), the body effect of the MOSFET is very closely related to the transconductance of the MOSFET. Similar trends exist in the body effect as those that exist in the

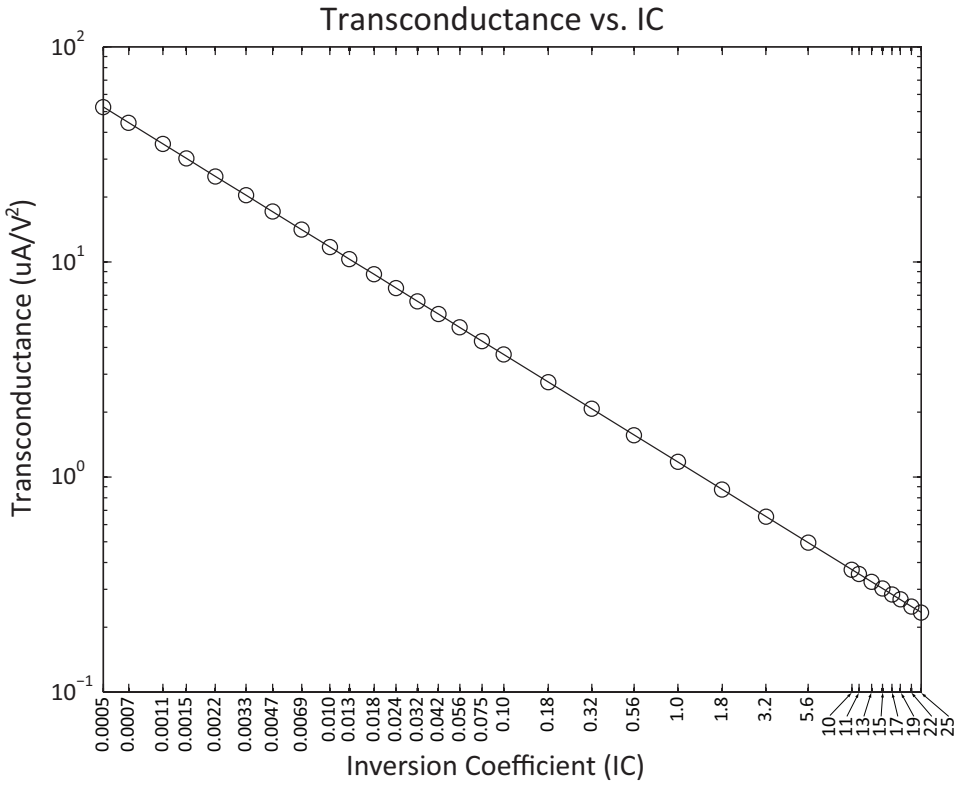

Figure 2.6: The change in transconductance with respect to the value of the inversion coefficient. As the value of IC increases, the transconductance drops. This figure was created with a typical average value of K=1E-6 ($\frac{A}{V}$).

transconductance. However, when the source and the body of the MOSFET are tied to the same voltage potential, the value of g_{MB} is zero.

The Active Region Channel Conductance

When the MOSFET is in the active region the channel conductance is very close to zero (or equal to zero in an ideal MOSFET). In the active region the current in an ideal MOSFET should not change with respect to drain to source voltage as the pinchoff condition should prevent any changes to current with changing drain to source voltage. However, in a practical MOSFET, changes in drain current with respect to the drain to source voltage is not negligible. The resulting change is normally described as $g_{DS} = \frac{\partial I_D}{\partial V_{DS}}$.

The first reaction is to simply take equation (2.5) and take the derivative with respect to the drain to source voltage. However, this method is shown to provide inaccurate results [23]. The

MOSFET drain current may be accurate, but if the slope of the drain current changes even slightly, the value of g_{DS} is very inaccurate. Parameters such as effective channel length and carrier mobility change too much with drain to source voltage to allow for a simple yet accurate solution.

The value of the Early voltage (V_A) is sometimes used to describe the channel conductance [20]. The Early voltage is used in BJT design to predict the impedance of the transistor. To find the Early voltage, the tangent of the I_D vs. V_{DS} line is drawn until it crosses the V_{DS} axis. The value of $|V_{DS}|$ at this intersection is the Early voltage which can be used to solve for g_{DS} or $g_{DS} \approx \frac{I_D}{|V_A|}$. While this method seems simple, it is still reliant on the accuracy of the slope of I_D versus V_{DS}.

In [34], an accurate and simple method of solving for g_{DS} and V_A empirically is presented. The general process is to simulate a collection of data points, then using the least squares method of data fitting, derive a function for the value of g_{DS}. Since this is a function based on a specific collection of data points, certain parameters need to be chosen before the data can be collected. This process also gives results which are unique to the given configuration, therefore large deviations from the chosen dimensions produce inaccurate results. Although this solution is somewhat limited, the accuracy of the results are very good. For the ON Semiconductor $0.5\mu m$ C5X models used in this thesis, the channel conductance equations are calculated in Appendix A.

The basic trend that should be noticed from the results of Appendix A is that in the active region, as the value of IC drops, the value of g_{DS} increases. As the length of the device increases, the value of g_{DS} drops. In order to increase the resistance of a device ($r_{DS} = \frac{1}{g_{DS}}$), the length of the channel should be increased. Figure 2.8 shows the change in the drain to source resistance with IC using the simpler equation for channel conductance in the triode region. Although the equation is different, the same general trends are observed.

2.2.5 Triode Region Small Signal Model

The small signal model of the MOSFET operating in the Triode region is given in Figure 2.7. Similar to the active region small signal model there are four terminals to take into account on a typical MOSFET. Each of these terminals may have a different voltage potential causing changes to various internal parameters.

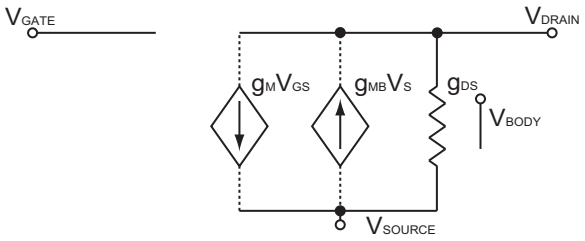

Figure 2.7: The MOSFET small signal equivalent circuit for the triode region of operation. The transconductance and body conductance are shown with dashed lines to emphasize the fact that deep in the triode region these values become very small (often negligible).

The transconductance of the MOSFET operating in the triode region is not shown on the small signal model in Figure 2.7. This is because the transconductance value is typically very small due to the drain to source voltage across the device. By taking the derivative of equation (2.4) with respect to V_{GS}, the transconductance of the MOSFET in the triode region can be found as

$$g_M = \frac{\mu C_{OX} W}{nL} V_{DS}. \tag{2.9}$$

If the drain to source voltage biases the device very close to pinchoff, the transconductance becomes non-negligible. However, for operation deep in the triode region g_M is too small to make a significant difference. Since the body effect is a factor of transconductance, the body effect is also negligible in the triode region.

The Triode Region Channel Conductance

The only parameter considered non-negligible in the triode region MOSFET model is the channel conductance [27]. Since there is a continuous channel in the triode region, the channel conductance is very easy to solve for. By taking the derivative of equation (2.4) with respect to V_{DS}, the value of g_{DS} can be found as

$$g_{DS} = \frac{\mu C_{OX} W}{nL} \left(V_{GS} - V_T \right), \tag{2.10}$$

when the $\frac{V_{DS}^2}{2}$ term in the equation is neglected.

The value of g_{DS} in the triode region is dependent both on the value of V_{GS} and V_T as well as on the dimensions of the device. If the length is increased the resistance of the device also increases. If most of the parameters in Equation (2.10) are assumed to be constant, Equation (2.10) can be rewritten to solve for r_{DS} with a constant K as

$$r_{DS} = K\frac{L}{W}. \tag{2.11}$$

The resulting behavior is shown in Figure 2.8. A higher value of IC increases the value of r_{DS}.

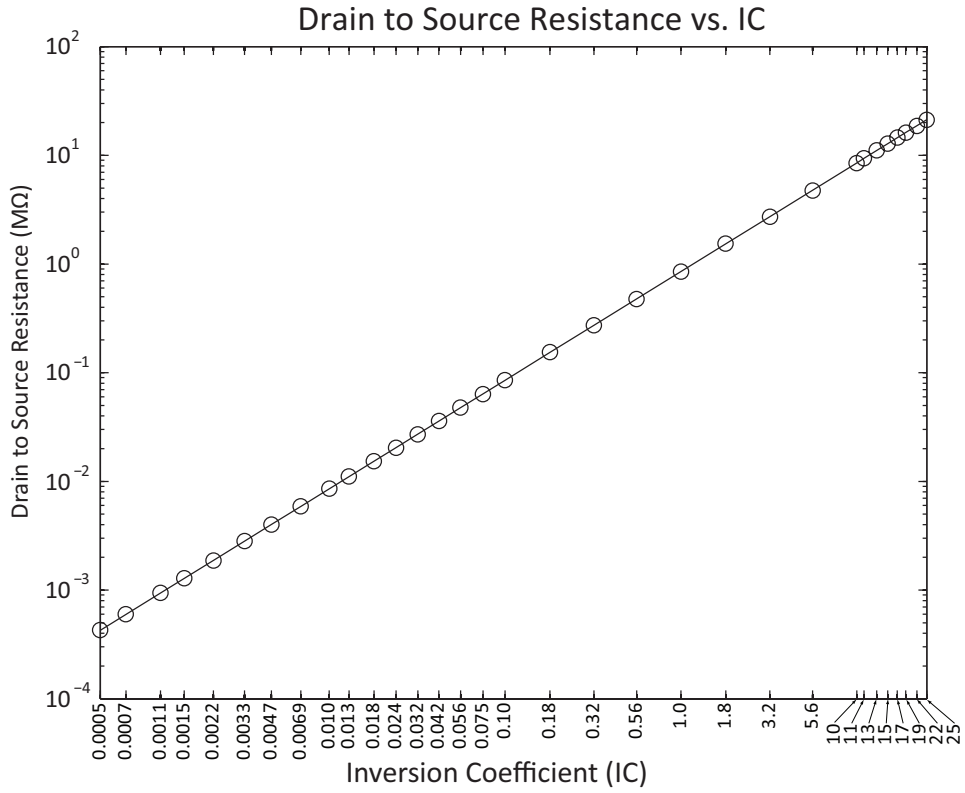

Figure 2.8: The change in drain to source resistance with respect to the value of the inversion coefficient. As the value of IC increases, the resistance increases. This figure was created with a typical average value of K=1E+6 ($\frac{A}{V}$).

2.2.6 Capacitance in the MOSFET

In both the triode and active region, the capacitance of the MOSFET is fairly similar. Each of the overlapping conductors are still present in each region and changes the output of the MOSFET at various frequencies. The small signal model for the active region including the major parasitic capacitances is shown in Figure 2.9. The small signal model for the MOSFET operating

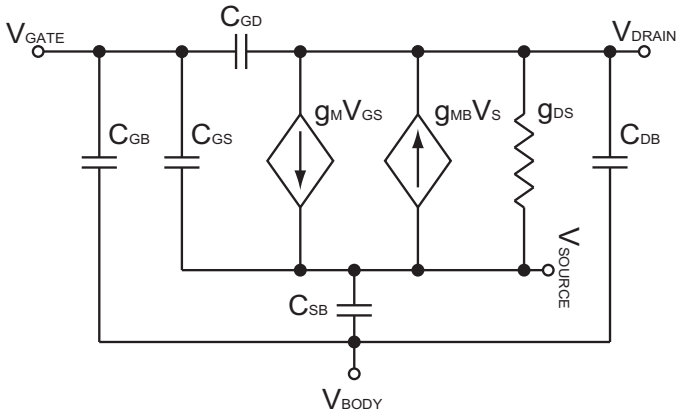

Figure 2.9: The active region MOSFET small signal equivalent circuit including parasitic capacitances.

in the triode region with parasitic capacitances is given in Figure 2.10.

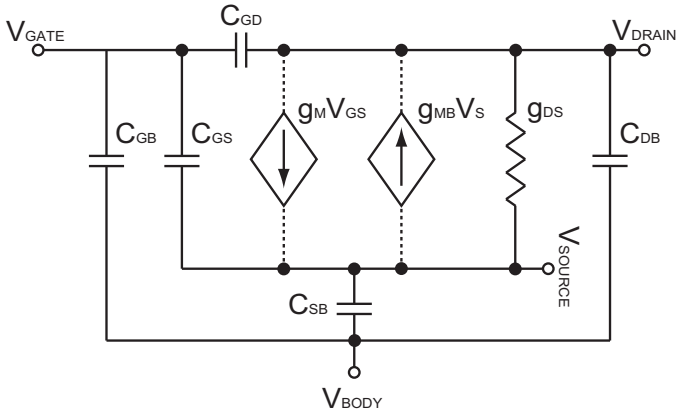

Figure 2.10: The triode region MOSFET small signal equivalent circuit including parasitic capacitances. The transconductance and body conductance are shown with dashed lines to emphasize the fact that deep in the triode region these values become very small (often negligible).

Gate to Source Capacitance

The gate to source capacitance C_{GS} is the largest capacitance in the MOSFET [27]. This is due to the overlap of the gate and the conductive channel in both the active and triode region. The capacitance of this overlap is

$$C_{GS} = \frac{2}{3} W L C_{OX}. \tag{2.12}$$

It is easily seen that the width and the length of the channel are the major factors in the size of this capacitance. The width and length multiply, increasing the capacitance very quickly.

Gate to Drain Capacitance

The gate to drain capacitance (C_{GD}) can become very large due to two factors. The first is the result of very large device widths. As the width of the device increases, so does the capacitance. The Miller effect also plays an important role in increasing the value of this capacitance. The function for gate to drain capacitance in the active region is

$$C_{GD} = W L_{OV} C_{OX}, \tag{2.13}$$

and the Miller effect capacitance, with the gate to drain capacitance reflected to the gate to ground terminals, can be found as

$$C_M = C_{GD}(1 + A_{OV}). \tag{2.14}$$

Source to Body Capacitance

The source to body capacitance (C_{SB}) is the capacitance that results from the separation of the source terminal from the body of the MOSFET. The value of C_{SB} is mostly dependent on the geometry of the source terminal. In both the active and triode region there is added capacitance due to the conductive channel. From [27], the value of C_{SB} for a MOSFET in the active region can be found as

$$C_{SB} = (A_S + WL) C_{JS} + P_S C_{J-SW}, \tag{2.15}$$

where A_S is the area of the source, C_{JS} is the depletion capacitance of the source junction, P_S is the perimeter of the source, and C_{J-SW} is the sidewall capacitance of the source. The values of C_{JS} and C_{J-SW} are related to the value of V_{SB} through

$$C_{JS} = \frac{C_{J0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_0}}}, \tag{2.16}$$

and

$$C_{J-SW} = \frac{C_{J-SW0}}{\sqrt{1 + \frac{V_{SB}}{\Phi_0}}}, \tag{2.17}$$

where C_{J0} and C_{J-SW0} are based on the fabrication of the MOSFET and Φ_0 is the built in voltage of the diode junction created by the source and body. Each of these parameters are based on the doping level of both the source and body.

Drain to Body Capacitance

The value of the drain to body capacitance C_{DB} is very similar to the value of C_{SB}. In the active region the channel is separated from the drain by the pinchoff condition. The geometry of the drain is the only contributing factor to this capacitance. For the device in the active region, the value of C_{DB} can be expressed as

$$C_{DB} = A_D C_{JD} + P_D C_{J-SW}, \tag{2.18}$$

where A_D and P_D are the area and perimeter of the drain respectively. The value of C_{JD} is very similar to the value of C_{JS} and can be found as

$$C_{JD} = \frac{C_{J0}}{\sqrt{1 + \frac{V_{DB}}{\Phi_0}}}, \tag{2.19}$$

where V_{DB} is the potential difference between the drain and the body.

Gate to Body Capacitance

The gate to body capacitance C_{GB} is typically very small compared to the rest of the parasitic capacitances in the MOSFET. This is due in part to the general equation for capacitance or

$$C = \frac{\varepsilon * Area}{Distance}. \tag{2.20}$$

For most MOSFETs, the distance separating the gate from the body is large enough to make this capacitance negligible. The effect of the source and drain to the body overpowers the effect of the gate to body capacitance very quickly. In this thesis the effect of C_{GB} is assumed to be negligible in all regions of operation.

2.3 Summary

This chapter has presented some of the recent research as well as the ideas, equations, and assumptions that are used in this thesis. Many of the later sections refer back to this section while explaining how the composite cascode stage works and how the device dimensions can easily be selected.

CHAPTER 3. THE COMPOSITE CASCODE STAGE

Transistor gain stages used in modern designs often implement a similar topography to those in older gain stages fabricated using vacuum tubes. A vacuum tube architecture that has been successfully implemented using MOSFET devices is the cascode stage. The cascode stage is implemented in vacuum tube architecture by connecting the anode of the lower device to the cathode of the upper device. The devices are in a *cascade to cathode* or *cascode* configuration. A similar configuration is implemented with MOSFETs by connecting the source of the upper device to the drain of the lower device. In the cascode architecture the gates of the Devices are independently biased. In the *composite cascode* stage the gates of the two MOSFETs are tied together, removing one of the bias voltages and simplifying the overall design. The design of the composite cascode stage has several benefits, many of which have been summarized in previous literature [5, 6].

Recently, several low-power bioinstrumentation amplifiers have been developed using the composite cascode stage [4, 19, 35]. The final systems were designed for a particular set of parameters, making general use more difficult. This chapter presents the various configurations of the composite cascode stage and shows how these configurations can be used to simplify the design process.

3.1 The Single Ended, Current Source Loaded, Composite Cascode Stage

An N-Type, single ended, current source loaded, composite cascode stage is shown in Figure 3.1. The main advantage for using this idealized stage is the current source, which presents a single impedance to the stage (R_{LOAD}). If the current source is ideal the value of R_{LOAD} is infinite. Using this configuration simplifies the derivation of both the gain and bandwidth equations as parasitic impedance from the load can be neglected.

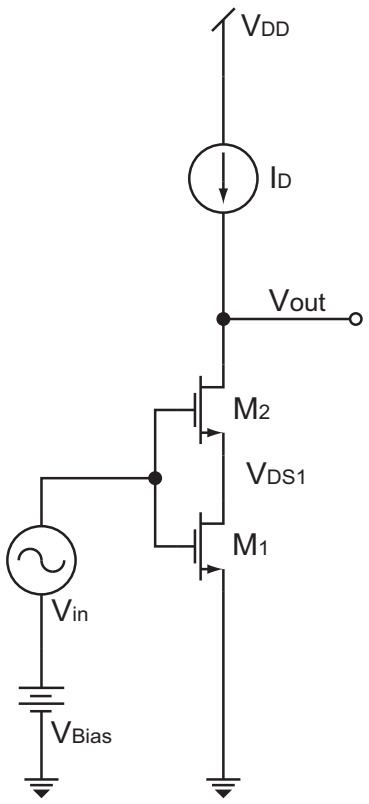

Figure 3.1: An ideal current source loaded composite cascode connection. Adapted from [17].

Some useful trends can be easily spotted while using this idealized configuration. The first is the effect of operating region on the gain and bandwidth of the stage. The value of V_{DS1} shown on the schematic can be used to determine which operating region both devices are operating in. In order to find the operating region of M_1, the following calculations can be used. If $[V_{Bias} - V_{T1} \leq V_{DS1}]$, M_1 is operating in the active region. If $[V_{Bias} - V_{T1} > V_{DS1}]$, M_1 is in the triode region. For the operating region of M_2, similar calculations are used. If $\left[(V_{Bias} - V_{DS1}) - V_{T2} \leq V_{[OUT-DC]} - V_{DS1}\right]$, then M_2 is operating in the active region. If the stage is biased such that $\left[(V_{Bias} - V_{DS1}) - V_{T2} > V_{[OUT-DC]} - V_{DS1}\right]$, then M_2 is in the triode region. Biasing M_2 into the triode region is very difficult as the value of $V_{Bias} - V_{T2} - V_{DS1}$ usually tends to be negative which ensures M_2 operation in the active region. For simplicity in this thesis, M_2 is assumed to always operate in the active region.

In [5], the authors discuss the effect of the operating region of M_1 on the composite cascode gain and bandwidth. When M_1 is operating in the pinchoff to active regions, the composite cascode gain is very high. However, the bandwidth of the stage tends to be very low. When M_1 enters the

deep triode region the gain of the composite cascode stage drops to lower values and the bandwidth becomes larger. The voltage gain drops for M_1 in the triode region because the gain of the system is mostly due to the gain of M_2. There is very little gain from M_1 as the transistor acts as a voltage controlled resistance. The output impedance of the overall stage is high compared to a single common source amplifier but the gain is similar.

3.2 The Single Ended, Composite Cascode Load, Composite Cascode Stage

A more practical version of the composite cascode stage is given in Figure 3.2. If the dimensions of the composite cascode stage are chosen correctly, the output impedance can be very high. Matching the impedance of the load to the gain stage is very simple, which enables maximum power transfer and easy selection of the dimensions of M_3 and M_4.

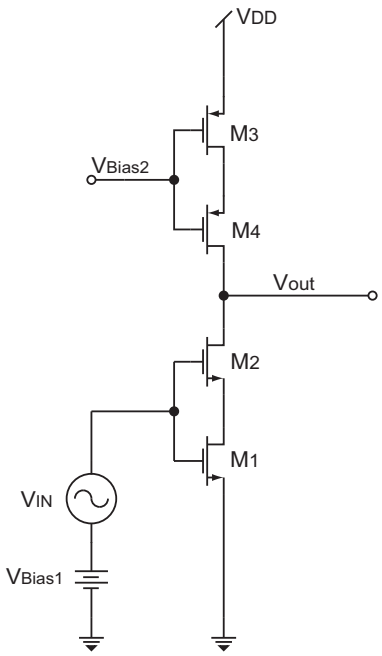

Figure 3.2: A composite cascode loaded composite cascode stage. Adapted from [17].

In order to match the top devices to the bottom devices, the current equations can be used. The MOSFETs M_3 and M_4 are P-Type devices meaning that holes instead of electrons act as the carriers. Therefore, most of the parameters which make up the drain current equations are inverted, as positive voltage ”pushes” the holes away from the gate. The drain current for the

P-Type MOSFET is

$$I_{D[P-Type]}(WI-SI) = I_0 \frac{W}{L}\left[ln\left(1+e^{\frac{-V_{GS}+V_T}{2nU_T}}\right)\right]^2, \tag{3.1}$$

where I_0 is the technology current for the P-Type device. Each of the parameters in both the drain current for the N-Type and P-Type devices are equal. The main difference in the drain current equation is the electron versus the hole mobility. Electrons typically have smaller effective mass than holes meaning that the N-Type devices are able to carry more current than similarly sized P-Type devices [31, 32]. Using this relationship, the width and length of M_3 and M_4 can be found by using the width and length of M_1 and M_2. These calculations are

Widths:

$$W_3 = \frac{\mu_n}{\mu_p}W_1 \quad \& \quad W_4 = \frac{\mu_n}{\mu_p}W_2, \tag{3.2}$$

Lengths:

$$L_3 = L_1 \quad \& \quad L_4 = L_2, \tag{3.3}$$

where μ_n is the electron mobility and μ_p is the hole mobility. By sizing the MOSFETs using these relationships, the values of r_{DS}, g_{DS}, and g_M of the load can be made approximately equal to the values of r_{DS}, g_{DS}, and g_M of the gain stage. This allows for some useful assumptions to be made which can simplify the MOSFET sizing in the composite cascode loaded stage.

3.3 The Differential Composite Cascode Stage

The final configuration of composite cascode stage is shown in Figure 3.3. There are several things to note about this configuration. The first is that the current through the stage is set by a single current source, I_D, shown on the bottom of the figure. This current source has to supply the current for both branches. Also, equations derived for differential stages usually assume the devices across from each other horizontally are matched (M_1 dimensions = M_5 dimensions, etc.). If the devices are matched the gain is highest and the gain equations are easier to solve for. Lastly, the positive and negative inputs are listed on the figure in relation to the positive and negative outputs.

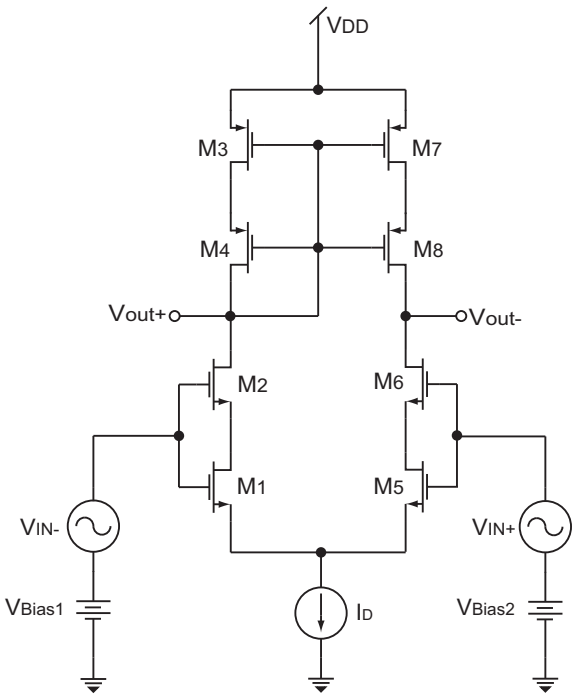

Figure 3.3: The composite cascode differential stage.

3.4 Summary

This chapter simply presented each configuration of the composite cascode stage and discussed how they may be most effectively used in design and analysis. When the stage is driven with an ideal current source, the gain equation becomes very simple. With proper sizing of the composite cascode load, the gain equation can still be very simple but the stage is more practical and can be fabricated in silicon. Finally the differential stage was presented. The differential stage is most commonly used as an input to an operational amplifier as high gain, high input impedance, low bandwidth stage. Since the trends seen in the single ended, current source driven, composite cascode stage scale up into the more complex configurations, the current source driven stage is used in the calculations for the remainder of this thesis.

CHAPTER 4. THE GAIN OF THE COMPOSITE CASCODE STAGE

The gain of the composite cascode stage is one of the most important features of the stage and is set by a combination of the drain current and MOSFET sizing [3–5, 35]. The value of I_D and the MOSFET dimensions are both considered in the inversion coefficient equation (2.1). The inversion coefficient is an effective starting place in the design of the composite cascode stage as the general behavior in each region of operation is very distinct. This chapter shows how the gain of the composite cascode stage depends on the various design parameters available to the circuit designer. Many of the simulation results in the following chapters (Chapters 4, 5, and 6) were compiled using the circuit shown in Figure 4.3. This simplified composite cascode stage will allow for a concise discussion on the behavior of the composite cascode stage.

4.1 The General Gain Behavior of the Composite Cascode Stage

In order to effectively use the composite cascode stage in a design as the main gain stage, some simplified hand calculations are needed. This section discusses the results of the equation derivations and compares them to the simulation results. These results are then analyzed for general design trends and points of interest.

4.1.1 Equations for Composite Cascode Gain

The gain equation of the composite cascode stage is derived in Appendix B.1.1 for a load impedance of R_{LOAD}. The final gain equation is

$$A_{MB} = -\frac{g_{M1}r_{DS1} + g_{M2}r_{DS2} + g_{M1}\left(g_{M2} + g_{MB2}\right)r_{DS1}r_{DS2}}{1 + \frac{1}{R_{LOAD}}\left(r_{DS1} + r_{DS2} + \left(g_{M2} + g_{MB2}\right)r_{DS1}r_{DS2}\right)}. \tag{4.1}$$

When the load is considered to be an ideal current source and $R_{LOAD} = \infty$, the gain equation can be approximated as

$$A_{MB} = -\left[g_{M1} r_{DS1} + g_{M2} r_{DS2} + g_{M1}\left(g_{M2} + g_{MB2}\right) r_{DS1} r_{DS2}\right]. \tag{4.2}$$

Using Equation (4.2), and plotting the results versus the inversion coefficient of M_2, Figure 4.1 is the result. It is easily seen from the calculations that the highest gain occurs when M_1 is in the strong inversion region and M_2 is in the subthreshold region (for a drain current of $I_D = 200nA$). Also, the lowest gain is shown to be when M_1 is in the subthreshold region and M_2 is in the weak inversion region. Finally, this plot shows that as M_2 moves deeper into the strong inversion region, the gains tend to converge to a single value.

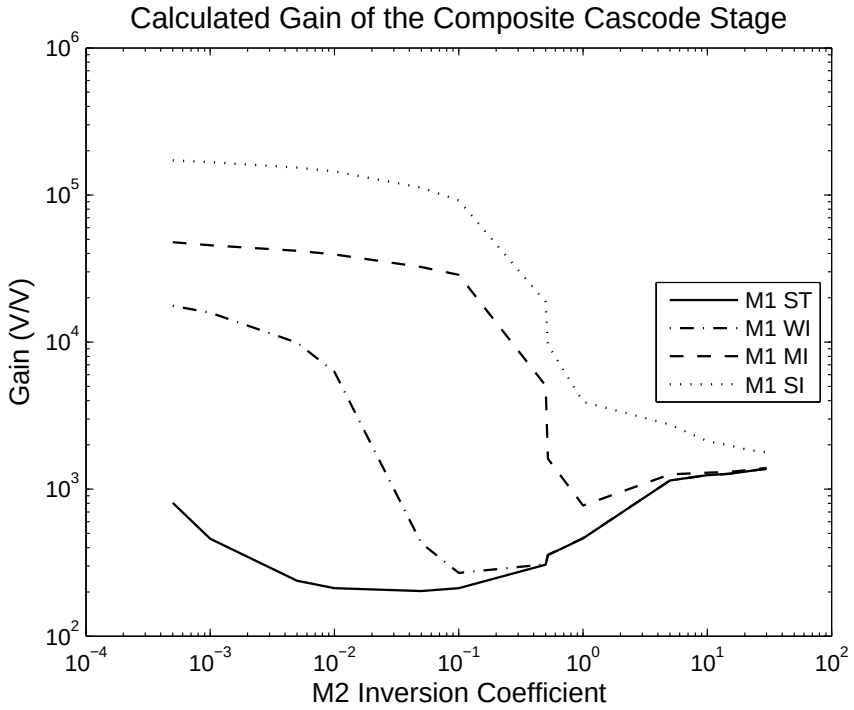

Figure 4.1: The calculated gain of the composite cascode stage with M1 IC held constant and the M2 IC swept from 0.0005 to 30.

Although the gain versus *IC* plot is useful for quick analysis, the data can be re-plotted to help visualize the effect of operating region on the composite cascode stage. Figure 4.2 shows how the gain versus $V_{Bias} - V_{T1} - V_{DS1}$ can be used to see the relation of gain to the operating region of

M_1. For $V_{Bias} - V_{T1} - V_{DS1} > 0$, M_1 is in the triode region. For $V_{Bias} - V_{T1} - V_{DS1} \leq 0$, M_1 is in the active region. The larger the magnitude of $|V_{Bias} - V_{T1} - V_{DS1}|$, the deeper into the active or triode region the device is operating in.

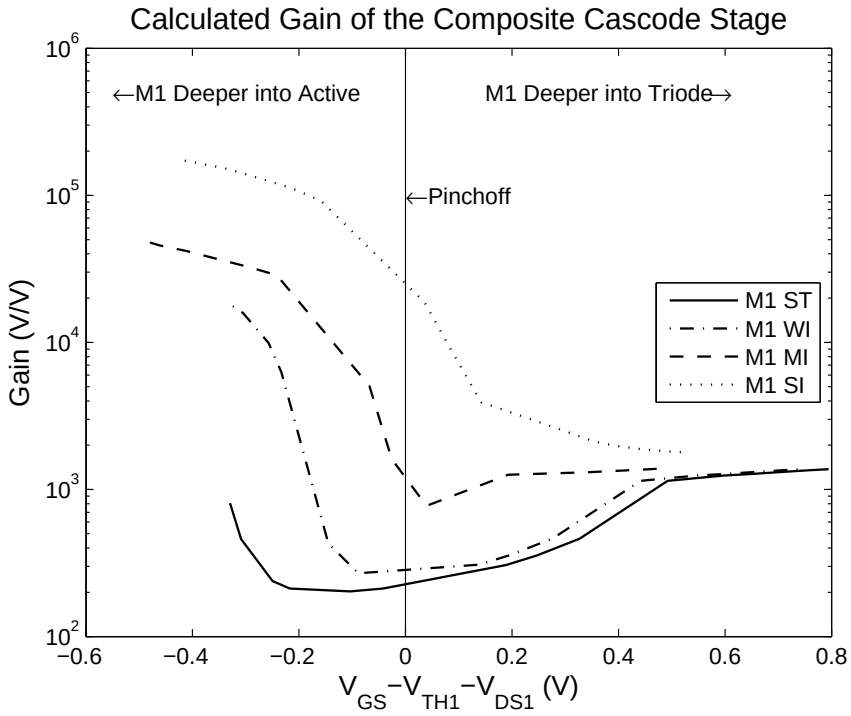

Figure 4.2: The calculated gain of the composite cascode stage with M1 IC held constant and the M2 IC swept from 0.0005 to 30. Plotted against the operating region for simpler analysis.

The equations verify the operation of the composite cascode stage as described in [5]. This operation includes low gain when M_1 is in the triode region and high gain when both devices are in the active region.

4.1.2 Simulations for Composite Cascode Gain

In order to verify the equations for the composite cascode stage, simulations were used. These simulations used the composite cascode stage shown in Figure 4.3 as the main stage for testing. This configuration was used as the number of variables present are at a minimum. The drain current through both devices can be set by setting I_D to a desired current draw. Since the current source used is ideal, the gain equation is the same as equation (4.2). After the drain current

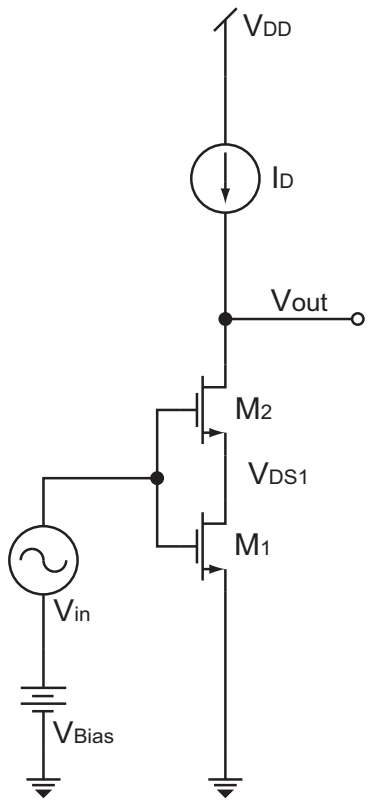

Figure 4.3: An ideal current source loaded composite cascode connection.

was set, the widths and lengths of M_1 and M_2 were selected to bias the devices into each of the four inversion levels. Equation (2.3) was used to select the widths and lengths of the devices based on the desired inversion level. The value of V_{Bias} was then adjusted until the DC value of V_{OUT} was equal to $\frac{V_{DD}}{2}$. Following this procedure ensured the only values that changed from test to test were the dimensions of the devices and the value of V_{Bias}. By limiting the number of changing variables, the resulting data is easy to analyze.

The results of the simulations using the ON Semiconductor C5X $0.5\mu m$ models in PSPICE are superimposed on the results of the equations and are shown in Figure 4.4. The accuracy is very good across most of the regions of inversion. Slight deviations exist when M_2 is deep in the subthreshold region and M_1 is in the strong inversion region. These deviations occur from the fact that deep subthreshold operation is difficult to accurately model [35].

A quick analysis of this plot shows a few important trends. The first is that when M_1 is in the triode region the gain tends to be much lower. The gain is also seen to converge at a single point in the triode region far away from the pinchoff region. This is due to the fact that M_1 is falling

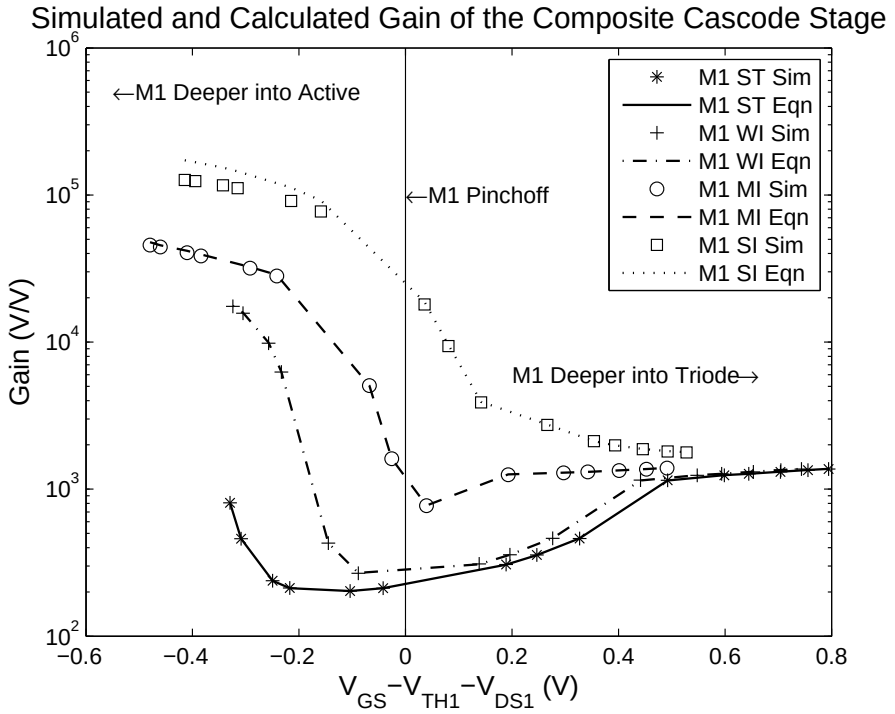

Figure 4.4: The simulated gain of the composite cascode stage with M1 IC held constant and the M2 IC swept from 0.0005 to 30. The results of the simulations are superimposed on the output of the gain equations to verify accuracy.

deeper into the triode region and acting more and more like a voltage controlled resistor. The gain begins to rely almost completely on the gain of the MOSFET M_2. This trend can be used to the advantage of the designer as is shown in Section 4.2.

4.2 Gain with the Lower Device in the Triode Region

The gain of the composite cascode stage with M_1 in the triode region is usually very low. This is because the stage acts as a common source amplifier with a single MOSFET [5]. The MOSFET M_1 acts as a resistor and adds to the overall output impedance of the stage. The benefit to using the composite cascode stage with M_1 in the triode region is lower gain, with higher bandwidth and impedance.

4.2.1 Equations for Composite Cascode Gain (M1 Triode)

When the gain of M_1 becomes very small due to the device operating in the triode region, the equation can be rewritten to simplify hand calculations. The resulting equation from Appendix B.1.2 is

$$A_{MB} = -\frac{g_{M2} r_{DS2}}{1 + \frac{1}{R_{LOAD}} \left(r_{DS1} + r_{DS2} + \left(g_{M2} + g_{MB2} \right) r_{DS1} r_{DS2} \right)}, \tag{4.3}$$

for a finite R_{LOAD}. As R_{LOAD} approaches infinity, the denominator approaches 1 and the resulting equation is

$$A_{MB} = -g_{M2} r_{DS2}, \tag{4.4}$$

which is the gain of a single, common source, MOSFET amplifier stage. For infinite loads the effect of M_1 can be neglected entirely. For finite loads, the impedance of M_1 alters the output impedance of the stage. These simplified equations can only be used for M_1 deep in the triode region.

4.3 Gain Design for the Composite Cascode Stage

Figure 4.5 can be used to help a designer develop composite cascode stages operating at 200nA. This figure was created by simulating M_1 and M_2, using the ON Semiconductor C5X models, operating at 32 different inversion levels. The bar on the right shows the magnitude of the gain in dB for the single ended, current source loaded composite cascode stage. Maximum gain ($\approx 102dB$) falls at the point where $IC1 = 15$ and $IC2 = 0.0005$. By using the IC equation and solving for $\frac{W}{L}$, the dimensions of the MOSFETs in the composite cascode stage can be quickly sized.

Figure 4.5 shows some very interesting behavior in addition to the minimum and maximum values of the gain. First, the gain of the stage seems to ”level off” for higher values of $IC2$ (the light blue region at the right of the figure). This is due to the fact that the voltage drop across M_2 increases due to much higher values of r_{DS2}. Eventually, M_1 drops into the triode region and acts simply as a source degenerating resistor.

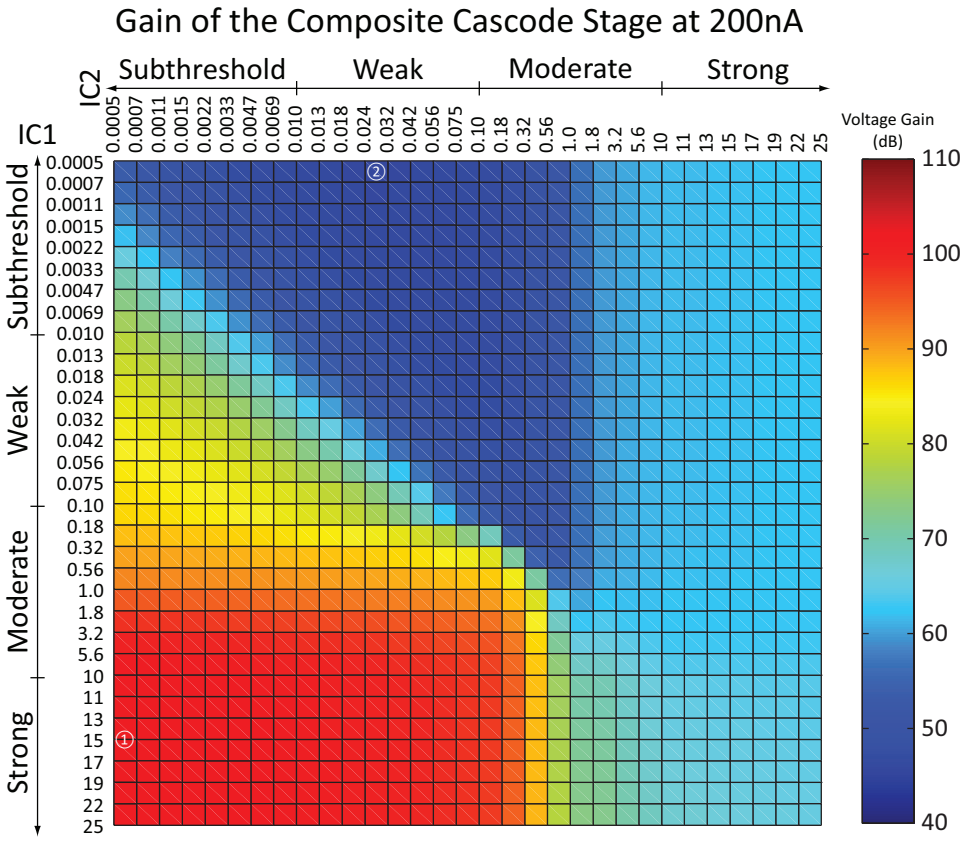

Figure 4.5: A chart showing the magnitude of the gain with respect to the inversion level of M_1 and M_2. The maximum gain is marked by a ① and the minimum gain is marked by a ②. The voltage gain in dB is given by the color gradient shown on the right.

Another interesting behavior that can be quickly noted from the chart is the wide spread of gain values available for M_2 operating in the subthreshold region. When M_2 is in the subthreshold region, the voltage drop from the drain to the source of M_2 allows for M_1 to operate in the active region. Longer lengths of M_1 increase the value of r_{DS1} while leaving the value of g_{M2} fairly constant. Increasing r_{DS1} increases the gain of the stage as is shown in Equation (4.2).

4.4 Gain with the Composite Cascode Load Configuration

For a more practical design the composite cascode load is connected to provide a high impedance for the amplifier (see Figure 4.6). As was shown in Section 3.2 the dimensions of the load devices can be chosen to match the impedance of the load to the impedance of the gain stage. In this configuration, as long as the load device ratios are equal to $\frac{\mu_n}{\mu_p}$ multiplied by the lower device

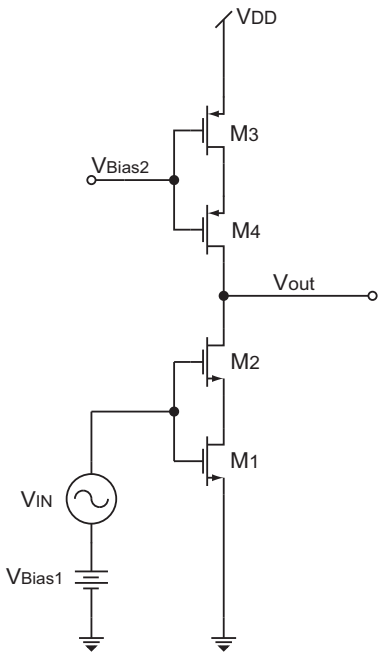

Figure 4.6: A composite cascode loaded composite cascode stage. Adapted from [17].

width to length ratios, the trends are very similar. If the impedance of the load is a multiple of the gain stage impedance, a new gain equation that can be used is

$$A_{MB} = -\frac{1}{1+m}\left[g_{M1}r_{DS1} + g_{M2}r_{DS2} + g_{M1}\left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}\right], \tag{4.5}$$

for all regions of operation, and

$$A_{MB} = -\frac{1}{1+m}\left[g_{M2}r_{DS2}\right], \tag{4.6}$$

for M_1 deep in the triode region. The value of m is

$$m = \frac{r_{DS1} + r_{DS2} + \left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}}{r_{DS3} + r_{DS4} + \left(g_{M4}+g_{MB4}\right)r_{DS3}r_{DS4}}. \tag{4.7}$$

The higher the impedance of M_1 and M_2 in relation to the impedance of M_3 and M_4, the lower the overall gain of the stage is. In the case of the ideal current source, the value of m is zero as the impedance of the load is infinite. Higher impedance for the load tends to make the gain higher, however, the gain cannot reach the same level as when there is an ideal current source. The

impedance of the load can also be used to fine-tune the gain of the composite cascode stage for an application.

4.5 Gain of the Differential Configuration

Since the differential stage is simply a mirrored version of the single-ended stage, the same trends that hold for both the current driven and composite cascode load stages hold for the differential stage. As is shown in the literature [17, 19, 27], differential gain of the composite cascode stage is the same as the equations for the single ended configurations (Equations (4.1) and (4.3)). Maximum gain is obtained when the devices across from each other horizontally are matched (M_1 dimensions = M_5 dimensions, etc.).

4.6 Summary

In this chapter, the gain of the composite cascode stage was discussed in depth. At first, only the ideal current source driven composite cascode stage was used to show the general behavior of the gain stage at various values of IC. Figure 4.5 was developed at 200nA using the C5X models to help in the selection of IC for both M_1 and M_2. Using this chart, a circuit designer can quickly and effectively choose the width to length ratio of the MOSFETs in the composite cascode stage. Later sections built on the established behavior of the stage to show how the composite cascode load can be used in both the single-ended and differential configurations.

CHAPTER 5. THE BANDWIDTH OF THE COMPOSITE CASCODE STAGE

The bandwidth of a composite cascode stage varies widely across the levels of inversion. The sizing of the devices play a major role in limiting the bandwidth of the composite cascode stage. The relationship between MOSFET dimensions and the value of *IC* play an important role in visualizing the bandwidth behavior of the composite cascode stage. This chapter presents the charts and equations useful in designing for composite cascode bandwidth.

5.1 The General Bandwidth Behavior of the Composite Cascode Stage

The bandwidth of the composite cascode stage is best analyzed through an evaluation of the composite cascode small signal model. The full composite cascode stage small signal model with parasitic capacitance is shown in Figure 5.1. Some of the capacitance has been neglected as the value of the capacitance is too small to be of any significance (C_{GB1} and C_{GB2}). Other parasitic capacitances have been neglected because the voltage potential across them is 0 (C_{SB1}). The remaining capacitance shown in Figure 5.1 has both non-negligible values and non-zero voltage potential.

5.1.1 An Equation for the Bandwidth of the Composite Cascode Stage

The general form of the bandwidth equation for MOSFET devices usually follows the bandwidth of an RC circuit. This is because there are two parasitic elements in the stage, the first being the intrinsic resistance of the devices, the second being the overlapping capacitance. The general form of the bandwidth equation is

$$f_{-3dB} = \frac{1}{2\pi R_{EQ} C_{EQ}}. \tag{5.1}$$

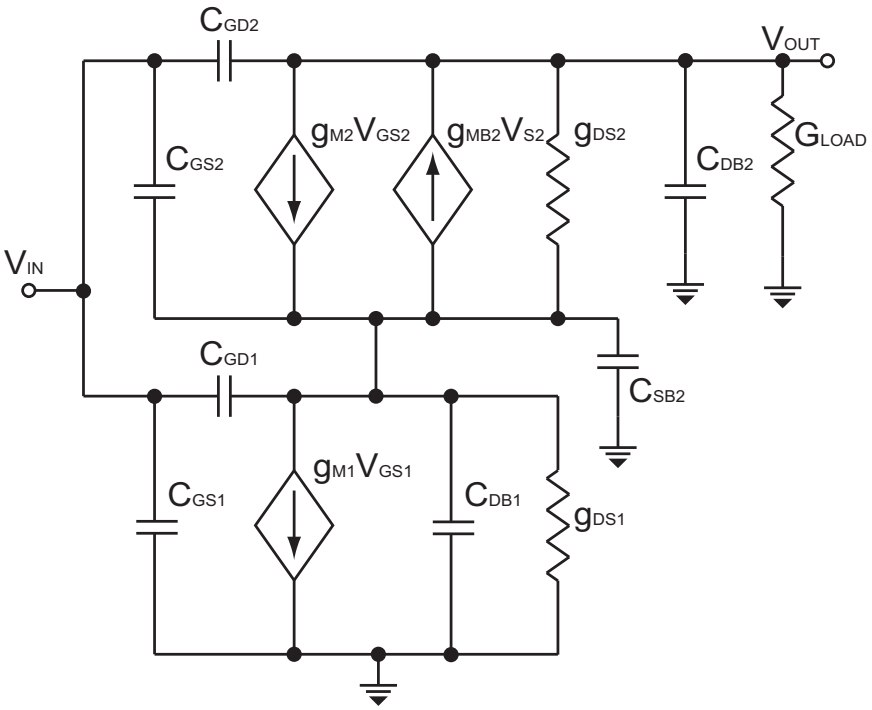

Figure 5.1: The composite cascode stage with small signal parasitic capacitances.

This function is used extensively in the chapter to estimate the bandwidth of the composite cascode stage.

5.1.2 Bandwidth Due to Nonzero Input Impedance

If the voltage source V_{IN} is not considered ideal and has a finite resistance, the frequency response of the composite cascode stage is set by the value of $R_{IN}C_{IN}$. The value of R_{IN} is equal to the equivalent resistance as seen from the gate of the MOSFET. The capacitance values must be solved for using the Miller effect. The Miller effect as described in [17] involves transforming the capacitance connecting the input to the output to simpler capacitances that connect the input and output to ground. Figure 5.2 shows the equivalent RC circuit for the input of the composite cascode stage.

Since capacitance in parallel adds, the equivalent capacitance can be written as

$$C_{EQ} = C_{GS1} + (C_{GD1} + C_{GS2})(1 + A_1) + C_{GD2}(1 + A_{OV}). \tag{5.2}$$

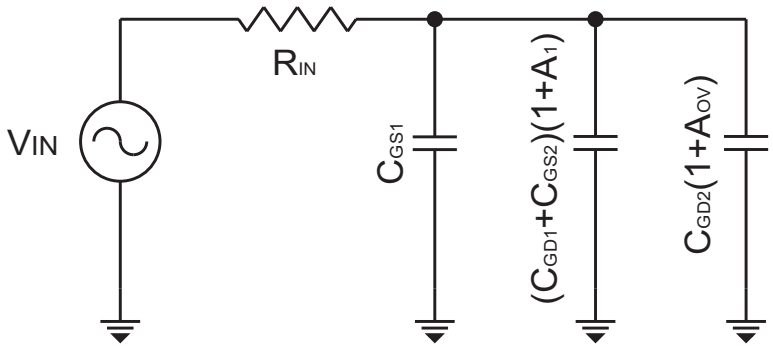

Figure 5.2: The parasitic capacitance and resistances from the input that cause frequency rolloff.

At this point the equivalent resistance and capacitance have been found and the final frequency response can be written. The frequency response due to the input of the composite cascode stage can be written as

$$f_{-3dB} = \frac{1}{2\pi R_{IN}\left(C_{GS1} + \left(C_{GD1} + C_{GS2}\right)\left(1 + A_1\right) + C_{GD2}\left(1 + A_{OV}\right)\right)}. \tag{5.3}$$

In Chapter 2 the contributing factors to these capacitances is discussed. Many of these capacitances are based on the width and the length of the channel, drain, and source of M_1 and M_2. However, since the Miller effect had been used to transform many of these capacitances to the input, the major contributing factor is the value of C_{GD2} which is multiplied by the full gain of the stage. When the gain becomes very large the bandwidth is small. For smaller gain, the bandwidth is much larger.

For practical designs, the input frequency response must be taken into account as the output resistance from the input source is not zero. In the initial design phase when the input resistance is considered to be an ideal voltage source ($R_{IN} = 0$), the frequency response goes to infinity. Also, for very low input resistance the frequency rolloff from the input may be at a high enough frequency to be neglected from the calculations.

5.2 Bandwidth from the Output Impedance

When the input voltage source has a resistance that is either very small or equal to zero, the frequency response of the stage is limited by the output impedance of the stage. As was done

in the previous section, the equivalent capacitance and the equivalent impedance of the composite cascode stage output terminals must be found. By setting $V_{IN} = 0V$ and rearranging the parasitic capacitance a very simple small signal model is obtained. The small signal model is shown in Figure 5.3. The load impedance is assumed to be infinite for simplicity in calculations.

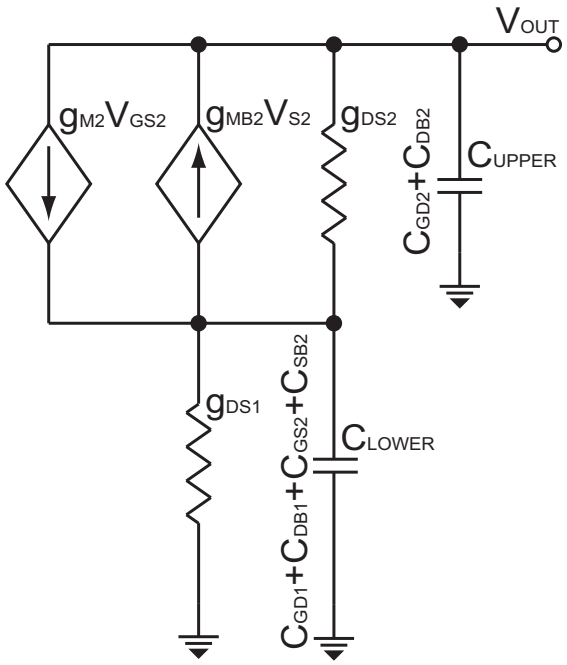

Figure 5.3: The parasitic capacitance and resistances from the output that cause frequency rolloff.

The capacitance in the composite cascode small signal model can be combined into two capacitors. The value of C_{LOWER} is

$$C_{LOWER} = C_{GD1} + C_{DB1} + C_{GS2} + C_{SB2}, \tag{5.4}$$

and the value of C_{UPPER} is

$$C_{UPPER} = C_{GD2} + C_{DB2}. \tag{5.5}$$

The equivalent impedance as seen from the terminals of C_{LOWER} and C_{UPPER} becomes R_{EQ} in the rolloff equation given in Equation (5.1). The equivalent resistance as seen from C_{LOWER} can be found using a test voltage and current. By setting V_{OUT} to zero and solving for the impedance in

terms of $\frac{V_{TEST}}{I_{TEST}}$ the resulting impedance is

$$R_{EQ-LOWER} = \frac{1}{(g_{M2} + g_{MB2}) + g_{DS1} + g_{DS2}}. \tag{5.6}$$

Since the values of g_{DS1} and g_{DS2} are usually very small compared to g_{M2} and g_{MB2}, the following approximation can be made

$$R_{EQ-LOWER} = \frac{1}{g_{M2} + g_{MB2}}. \tag{5.7}$$

The equivalent impedance as seen from the terminals of C_{UPPER} can be found using a similar approach. The result of the derivation is

$$R_{EQ-UPPER} = r_{DS1} + r_{DS2} + (g_{M2} + g_{MB2})\, r_{DS1} r_{DS2}, \tag{5.8}$$

which is the output impedance of the entire stage. The equivalent resistance as seen from the capacitance C_{UPPER} is typically several orders of magnitude larger than the resistance as seen from the capacitance C_{LOWER}. A general equation for the frequency response of the composite cascode stage can be found by neglecting the capacitance of C_{LOWER}. The final equation is

$$f_{-3dB} = \frac{1}{2\pi\,(r_{DS1} + r_{DS2} + (g_{M2} + g_{MB2})\, r_{DS1} r_{DS2})\,(C_{GD2} + C_{DB2})}. \tag{5.9}$$

Plotting this function against the inversion coefficient of M_2 allows for easy extraction of the general trends present in the composite cascode stage. Figure 5.4 shows the bandwidth of the composite cascode stage across the inversion levels of M_1 and M_2.

The highest bandwidth is seen to be at the point where M_1 is in the subthreshold or weak inversion region while M_2 is in the moderate inversion region. This is due to the fact that at the drain current this data was calculated, the dimensions of M_2 were very small in order to bias M_2 into moderate inversion. According to Chapter 2, for very small dimensions, the values of C_{DB2} and C_{GD2} are very small.

Plotting the bandwidth versus the region of operation ($V_{Bias} - V_{T1} - V_{DS1}$), some general trends with relation to operating region can be quickly spotted. Figure 5.5 show the calculated bandwidth versus the region of operation. The value of the bandwidth tends to converge toward

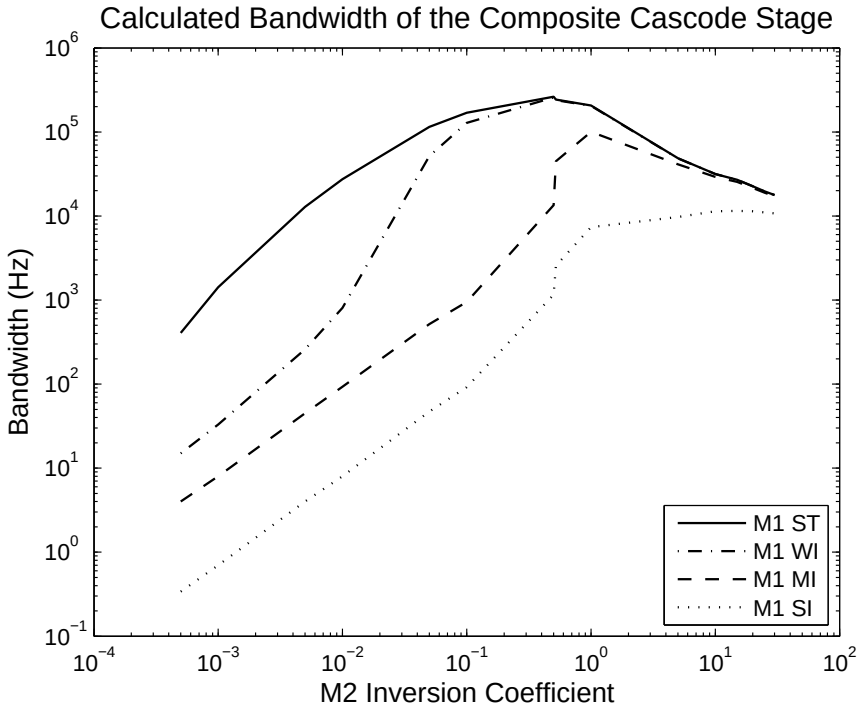

Figure 5.4: The calculated bandwidth of the composite cascode stage with the inversion coefficient of M1 held constant while sweeping IC2 from 0.0005 to 30.

a single value as was seen in the calculation of the gain. With M_2 deeper in the strong inversion region, the voltage drop across the drain to source of M_2 becomes large enough to make M_1 negligible. The capacitance of M_1 plays an even smaller role in the frequency response when the transistor is in the triode region.

When the stage is expanded into the composite cascode loaded composite cascode stage, the bandwidth can be found by using

$$f_{-3dB} = \frac{1}{2\pi \left(R_{STAGE} || R_{LOAD}\right)\left(C_{GD2} + C_{DB2} + C_{GD4} + C_{DB4}\right)}, \tag{5.10}$$

where R_{STAGE} is the impedance as seen from the output of the composite cascode stage and R_{LOAD} is the output impedance of the load. The capacitance of the output device of the load is added to the capacitance of the output device of the gain stage. While the resistance of the load and gain stage is reduced in a parallel combination, the capacitance is increased when added together. When the devices are sized according to Chapter 3.1, the bandwidth of the stage follows the same trends as shown in Figure 5.5.

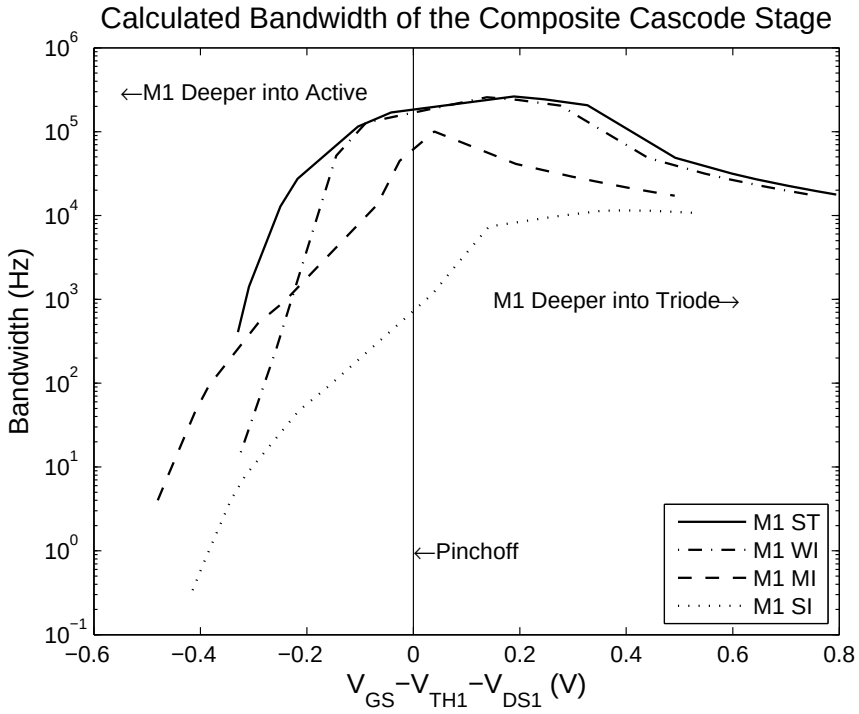

Figure 5.5: The calculated bandwidth of the composite cascode stage with the inversion coefficient of M1 held constant while sweeping IC2 from 0.0005 to 30. The results are plotted against the operating regions of M1.

5.3 Composite Cascode Bandwidth Simulations

Using the same models and simulations that were used in the gain equation simulations, Figure 5.6 was obtained. Figure 5.6 assumed the resistance of V_{IN} to be zero, resulting in the output impedance of the stage being the main contributing factor to the frequency rolloff. The accuracy of the derived equations as compared to the results of the simulations are very good.

5.4 Bandwidth Design for the Composite Cascode Stage

The bandwidth vs. *IC* chart shown in Figure 5.7 was developed using a similar method to that shown in Section 4.3. The bandwidth was simulated at 32 different values of IC_1 and IC_2 with a drain current of $I_D = 200nA$. The resulting values are plotted on a color scale with the magnitude of the bandwidth being shown in $log_{10}(Hz)$. This scale was chosen to help in the visualization of the magnitude of the bandwidth.

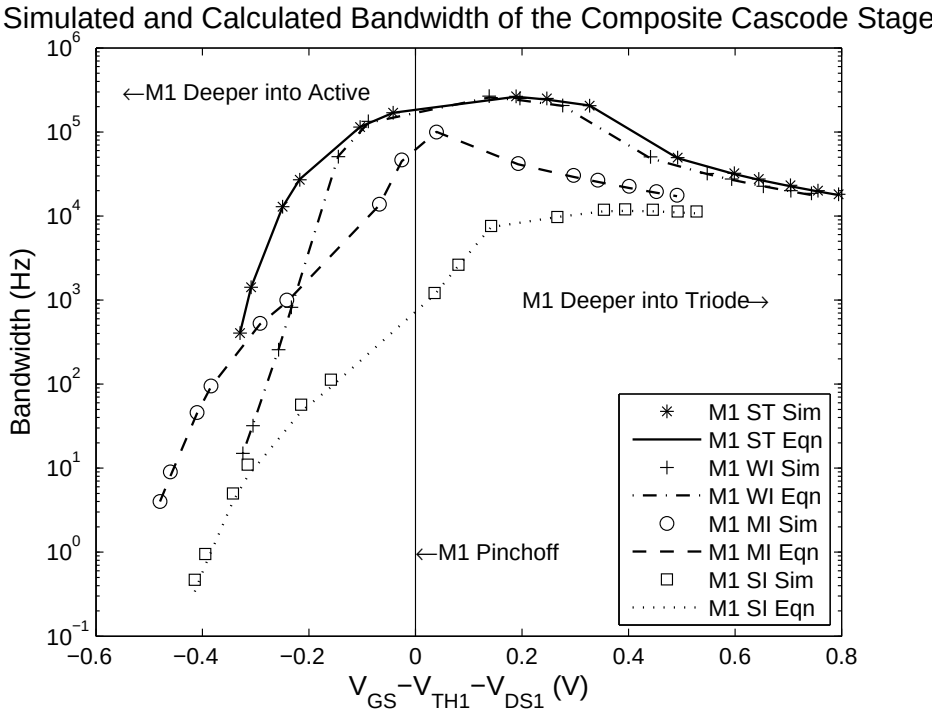

Figure 5.6: The simulated bandwidth of the composite cascode stage with the inversion coefficient of M1 held constant while sweeping IC2 from 0.0005 to 30. The results are superimposed on the calculated values to show the accuracy of the design equations.

The maximum value of the bandwidth ($275kHz$) is found in the middle of the moderate inversion region of M_2 and in the subthreshold region of M_1. At this point, the magnitudes of C_{DB2} and C_{GD2} are very small as the width to length ratio of M_2 is very close to 1. Also, the value of r_{DS1} is minimum in the subthreshold region. With minimum values of resistance and capacitance, the bandwidth is at the maximum value. The minimum bandwidth of the composite cascode stage ($0.437Hz$) falls at the point where r_{DS1}, C_{DB2}, and C_{GD2} is maximum. In Figure 5.7, this is shown to be in the lower left corner where $IC_1 = 25$ and $IC_2 = 0.0005$.

One last point of interest on Figure 5.7 is that as M_2 moves into the strong inversion region, the bandwidth tends to level off. This is again due to the fact that M_1 moves out of the active region and into the triode region. The bandwidth begins to rely solely on the the operation of M_2, as M_1 begins to act as a source degenerating resistor.

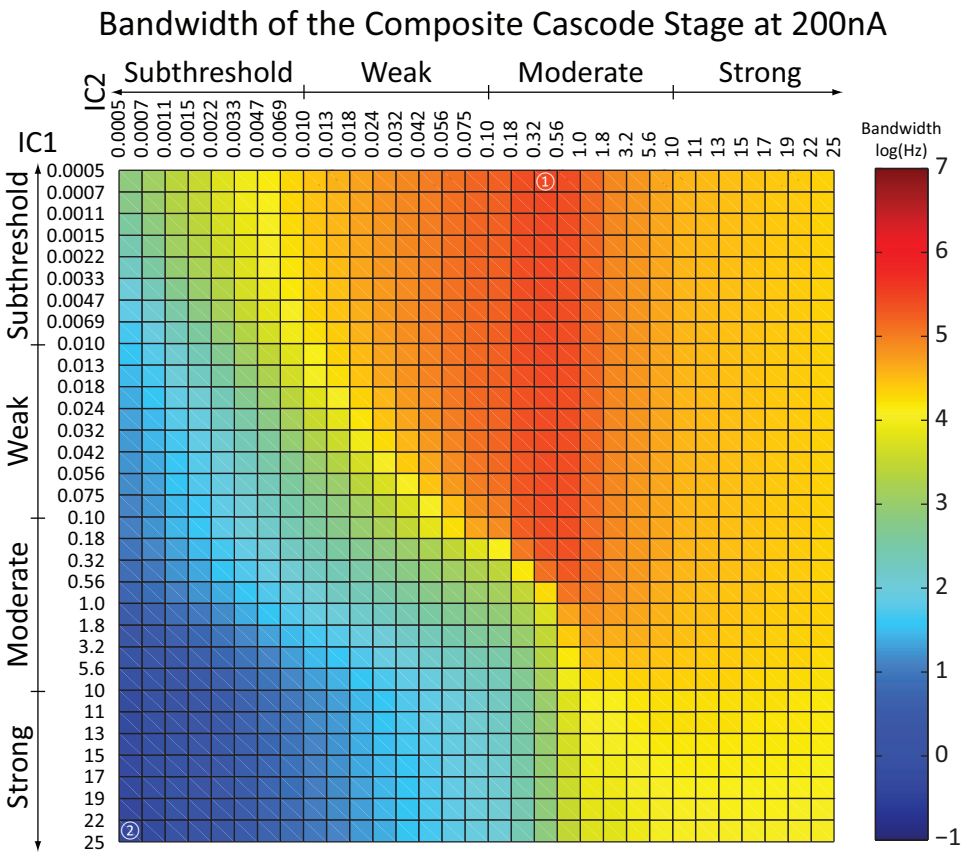

Figure 5.7: A chart showing the bandwidth with respect to the inversion level of M_1 and M_2. The maximum bandwidth is marked by a ① and the minimum bandwidth is marked by a ②. The color gradient shown on the right gives the value of the bandwidth in terms of $log_{10}(Hz)$ for easier visualization of the data.

5.5 Summary

The bandwidth of the composite cascode stage tends to be low even in higher bandwidth operation. This type of operation can be advantageous in the design of operational amplifiers as bulky compensation methods (such as pole-splitting) may be reduced or removed from the overall design [4, 27]. The equations and plots presented above show how the bandwidth of the stage can be accurately chosen through the selection of inversion coefficient.

CHAPTER 6. THE NOISE OF THE COMPOSITE CASCODE STAGE

6.1 Noise Sources in the Composite Cascode Stage

In [16] and [27] three types of noise present in MOSFETs are discussed. The noise sources in a MOSFET are thermal, flicker, and gate-current. While thermal and flicker noise tend to be the only non-negligible forms of noise in a MOSFET operating a lower frequency, each of these noise sources must be analyzed in order to ensure low noise operation of a final design. In this thesis, the general formulas for noise are presented and the effect of MOSFET sizing in the composite cascode stage versus noise is discussed.

6.1.1 Thermal Noise

The noise due to thermal effects in a MOSFET is the result of the resistance in the channel of the device. Figure 6.1 shows how thermal noise is introduced from the MOSFET into a system. The noise due to thermal effects is introduced into the system as a current source. Therefore, noise must be analyzed for MOSFET operation in both the triode region and the active region.

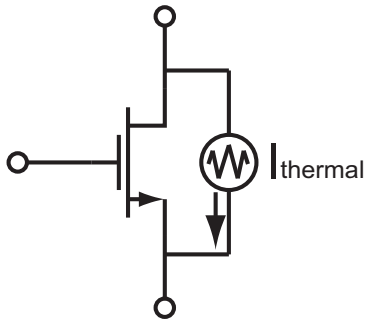

Figure 6.1: A diagram showing the introduction of thermal noise into a MOSFET. Adapted from [27].

In the triode region, the noise of a MOSFET is simply related to the resistance of the channel. The function for this relation is

$$I_{th}^2(f) = 4kTg_{DS} = 4kT\frac{\mu C_{OX}W}{nL}(V_{GS} - V_T), \tag{6.1}$$

where g_{DS} is the channel conductance as described in Chapter 2. In the triode region of operation the MOSFET noise is directly related to the ratio of width to length. The longer the length is in relation to the width, the lower the noise. When the MOSFET M_2 is operated in higher inversion regions, M_1 is forced into the triode region. The amount of gain due to M_1 is negligible, resulting in low noise. Although the width of M_1 is large compared to the length, the value of V_{GS1} tends to be approximately equal to V_{TH1} making the noise from M_1 negligible. Low noise operation is readily achieved when M_2 is operated in the moderate or strong inversion region.

In the active region the thermal noise of a MOSFET is not related to the conductance of the channel. In ideal MOSFETs, the conductance is zero and in practical MOSFETs the conductance is very small. This results in difficult calculations and inaccurate results. The value of transconductance is typically used instead. The resulting function for evaluating the thermal noise in the active region is

$$I_{th}^2(f) = 4kT\left(\frac{2}{3}\right)g_M = 4kT\left(\frac{2}{3}\right)\frac{I_0W\sqrt{IC}}{nU_TL}\frac{e^{\frac{V_{GS}-V_T}{2nU_T}}}{1+e^{\frac{V_{GS}-V_T}{2nU_T}}}, \tag{6.2}$$

where g_M is the transconductance of the MOSFET in the active region across all levels of inversion. When M_2 is in the subthreshold or weak inversion region the voltage drop across the gate to the source is small, bringing M_1 into the active region. High noise from M_1 is amplified by the MOSFET M_2. As a result, high gain tends to produce high thermal noise in the composite cascode stage.

6.1.2 Flicker Noise

As current passes through a MOSFET channel, the minority carriers move along the surface of the silicon [16, 27]. As minority carriers move across the channel, traps in the silicon "catch" the current carriers. Noise due to generation and recombination is created in the channel. Since the

noise is generated by quantum effects in the channel, the noise is usually represented as a voltage source in series with the input voltage source. This is shown in Figure 6.2

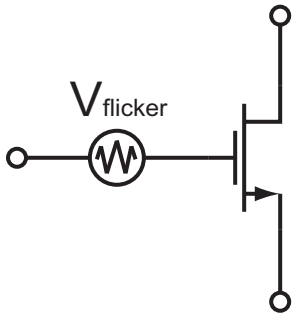

Figure 6.2: The flicker noise in a MOSFET. Adapted from [27].

The function for flicker noise in a MOSFET is

$$V_g^2(f) = \frac{K}{WLC_{OX}f}, \tag{6.3}$$

where K is a fitting term related to the fabrication of the device and f is the frequency of the input signal. This is why flicker noise is often called $\frac{1}{f}$ noise. As the frequency of the input signal drops, the noise increases. The flicker noise of a MOSFET is also related to the size of the device. The larger the dimensions the lower the flicker noise. Lower noise is one of the main advantages for M_1 operating in the subthreshold or weak inversion region. When the gain is low, the noise has very little effect on the output of the system. In addition to low gain, the large dimensions needed for subthreshold operation in M_1 help contribute to the low noise experienced when M_1 is in the subthreshold region and M_2 is in the strong inversion region. Operating M_1 in the moderate or strong inversion region increases the gain along with the noise. If low flicker noise is an important element of the design, M_1 should be sized for operation in the subthreshold or weak inversion region.

In addition to sizing, the input stage to an operational amplifier can be implemented in P-Type devices as the higher effective mass of the holes makes the carriers harder to trap than electrons [16, 27]. This is an important feature of the P-Type MOSFET that is often used to reduce noise.

6.1.3 Gate-Current Noise

The last form of noise in a MOSFET considered here is often negligible in the composite cascode stage. The lower bandwidth of the composite cascode stage reduces the effect of the gate-current noise in a device. At higher frequencies, the capacitance between the gate and the channel generate a noisy gate current that is related to the value of C_{GS}. The gate-current noise is modeled as a current source entering the gate of the MOSFET (as shown in Figure 6.3). The function for the gate-channel noise is

$$I_g^2 = \frac{16}{15} kT\omega^2 C_{GS}^2 \Delta f = \frac{16}{15} kT\omega^2 \left(\frac{2}{3} WLC_{OX}\right)^2 \Delta f, \tag{6.4}$$

where ω is the frequency in radians/second and C_{GS} is the gate to source capacitance neglecting the capacitance due to gate overlap.

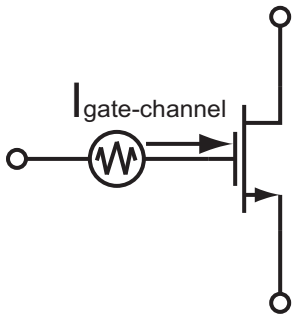

Figure 6.3: The gate-channel noise in a MOSFET. Adapted from [16, 27].

As was stated above, this source of noise is rarely considered in low frequency circuits. This noise source is related to the dimensions of the device, as well as the frequency. If the frequency of the input signal is small or if the dimensions of the device are small, this noise source can be neglected. The composite cascode stage is specifically designed for low to moderate frequency operation, therefore this thesis neglects the effects of gate-channel noise in total noise calculations.

6.2 Noise Equations for the Composite Cascode Stage

The noise of the composite cascode stage is calculated here using the circuit shown in Figure 6.4. As was mentioned in the previous sections, the only two non-negligible sources of noise are the flicker and thermal noise. Both are shown in this circuit for each MOSFET in the stage.

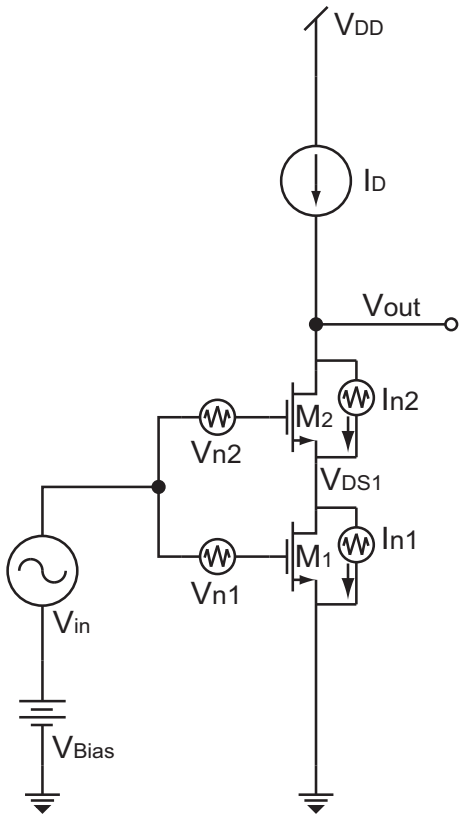

Figure 6.4: A circuit diagram showing the noise sources present in the composite cascode stage.

In [27], the authors suggest that in the low to moderate frequency range, the noise of a single MOSFET can be combined into a single voltage source on the gate of the device. This removes the noise current source I_{n1} and I_{n2}, and includes the effect in the noise voltage source V_{n1} and V_{n2}. The noise of a single MOSFET may then be written as

$$V_g^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_M} + \frac{K}{WLC_{OX}f}. \tag{6.5}$$

This equation allows for simple calculation of the total output noise. The noise output is related to the gain and bandwidth of the stage as if the noise were part of the input signal. Both the noise into M_1 and M_2 see the entire gain of the stage and simply sum together. The noise input of the stage can be written as

$$V_g^2(f) = 4kT\left(\frac{2}{3}\right)\left(\frac{1}{g_{M1}} + \frac{1}{g_{M2}}\right) + \frac{K}{C_{OX}f}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2}\right). \tag{6.6}$$

This input voltage is then multiplied by the gain of the stage as it varies from low frequency to high frequency. The frequency rolloff due to the parasitic capacitance and resistance is included in the calculations. The noise of the composite cascode stage with both devices in the active region is

$$V_g^2(f) = \frac{A_{MB}}{f_{-3dB}+f}\left[4kT\left(\frac{2}{3}\right)\left(\frac{1}{g_{M1}} + \frac{1}{g_{M2}}\right) + \frac{K}{C_{OX}f}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2}\right)\right], \tag{6.7}$$

where f_{-3dB} is the frequency rolloff given by Equation (5.9) and A_{MB} is the midband gain given by Equation (4.2). The effect of frequency is included in the equation as f. The thermal noise is different for M_1 operating in the triode region, however, a similar equation can be used. This equation is

$$V_g^2(f) = \frac{A_{MB}}{f_{-3dB}+f}\left[4kT\left(\frac{2}{3}\right)\left(\frac{1}{g_{DS1}} + \frac{1}{g_{M2}}\right) + \frac{K}{C_{OX}f}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2}\right)\right], \tag{6.8}$$

with the value of g_{DS1} taking the place of g_{M1}.

The resulting equations have been plotted against the simulations using the ON Semiconductor $0.5\mu m$ C5X model in PSPICE. The result of these simulations is in the following figures. Figure 6.5 shows the equation vs. the simulation data for M_1 operating deep in strong inversion and M_2 operating deep in subthreshold. Figure 6.5 also shows the noise when M_1 is deep in subthreshold and M_2 deep in the strong inversion region. The noise is high at very low frequencies but drops quickly after the f_{-3dB} point is reached.

The deviation of the calculations versus the simulation results occurs at a higher frequency than the f_{-3dB} point. This allows for the designer to neglect the deviation in the equations for simpler design equations. Low frequency noise is one of the most difficult problems to design for

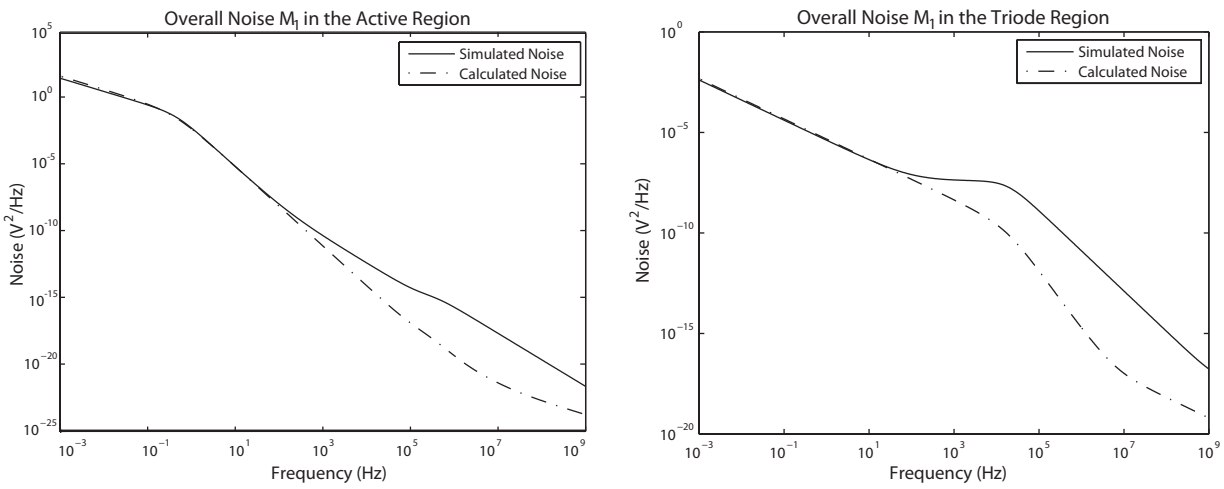

Figure 6.5: The total noise in the composite cascode stage as seen from the output of the stage for M1 in the active region (left) and M1 in the triode region (right).

when using MOSFETs at low frequency. Equations (6.7) and (6.8) are very accurate for predicting the low to moderate frequency noise present in the composite cascode stage.

6.3 Noise Design for the Composite Cascode Stage

The noise of the individual MOSFETs are shown above to be voltage or current sources which are added to the general operation of the devices. This means the flicker noise, which is the most dominant at low frequencies, is mostly related to the gain of the stage. The thermal noise becomes a major factor at higher frequencies when the gain has dropped due to parasitic capacitance. The composite cascode stage is inherently a low bandwidth stage making the thermal noise minimal in the output.

In similar fashion to Chapters 4 and 5, the general noise behavior of the stage can be found through the use of Figure 6.6. This figure shows how the inversion coefficient of M_1 and M_2 can be used to minimize the noise of the composite cascode stage.

The composite cascode stage can be a very low noise system. This is a major benefit when designing for systems that need very low noise for accurate signal measurement. The noise can be further reduced in the composite cascode stage by choosing large dimensions and using P-Type MOSFETs in the input stage.

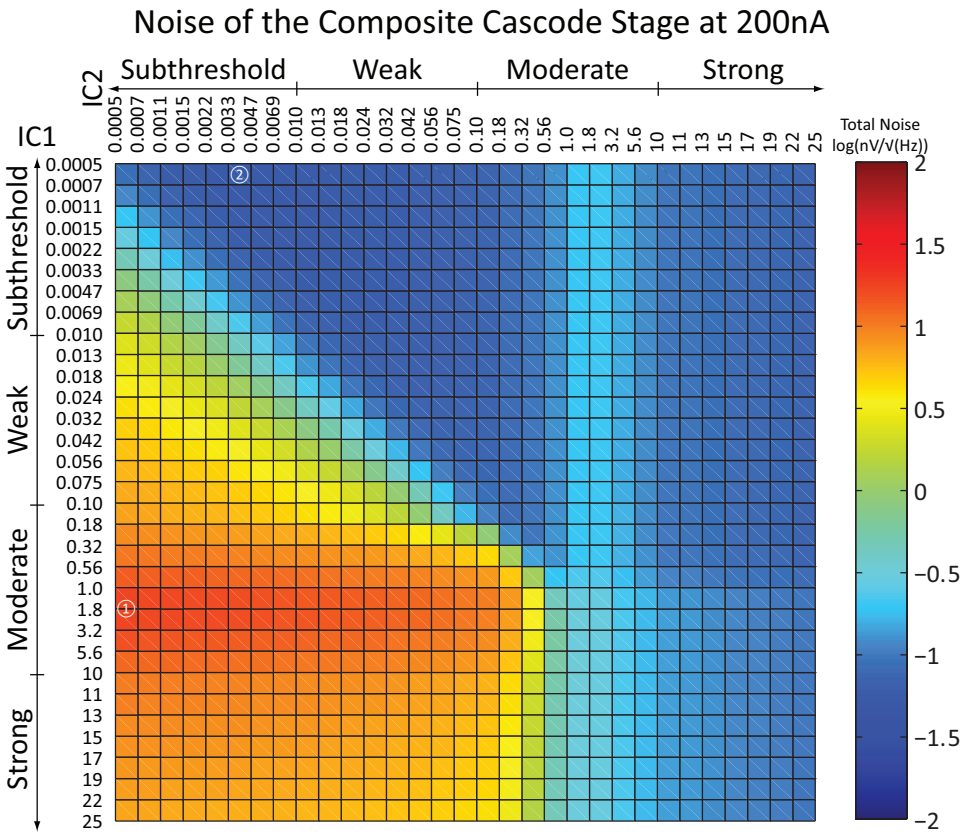

Figure 6.6: A chart showing the overall noise with respect to the inversion level of M_1 and M_2. The maximum noise is marked by a ① and the minimum noise is marked by a ②. The color gradient shown on the right gives the value of the noise in terms of $log_{10}(\frac{nV}{\sqrt{Hz}})$ for easier visualization of the data.

6.4 Summary

This chapter has discussed the noise of the composite cascode stage. Each of the noise sources of interest are discussed in the first few sections of this chapter. Equations are then derived using the small signal model of the composite cascode stage. Finally the design of the composite cascode stage in terms of noise is discussed. Suggestions for lowering the noise of the system are also given.

CHAPTER 7. A DESIGN BASIS FOR COMPOSITE CASCODE STAGES

Previous chapters have discussed the effect of the inversion coefficient on the gain, bandwidth, and total noise of the composite cascode stage. In Chapter 4, the gain was simulated across 32 different inversion levels of M_1 and M_2. A chart was then developed that compared the values of IC_1 and IC_2 to a color gradient of the gain. Spotting the desired gain value and selecting the proper MOSFET width to length ratio is simplified as a result. Similar plots for the bandwidth and total noise of the stage were also developed. This chapter seeks to expand the results from Chapters 4, 5, and 6 into a design methodology for the composite cascode stage. First a discussion on the relationship between drain current and stage behavior is presented, then the design methodology is outlined. Finally, the design methodology is used to develop an example operational amplifier optimized for biomedical applications.

7.1 Drain Current in the Design Process

One of the parameters held constant in previous chapters is the drain current (held at 200nA for each test). This is an important aspect in the design methodology presented in this thesis. One of the first steps a designer takes is to select the desired power consumption (which includes setting the supply voltage and current draw). Once the desired power is selected, the drain current in the composite cascode stage should not be changed. However, before choosing a desired current draw, the designer has some flexibility over the behavior of the composite cascode stage.

The equation used in Chapter 2 to select the width to length ratio of M_1 and M_2 is repeated here

$$\frac{W}{L} = \frac{I_D}{I_0 IC}. \tag{7.1}$$

Previously, the value of I_D was held constant at $200nA$ and the value of IC was chosen to achieve the desired behavior of the gain stage. If the value of I_D is not chosen to be $200nA$, the value of $\frac{W}{L}$ or IC must be changed in order to maintain equality. Since IC is a critical part of the design

methodology I chose to keep the value of IC constant as I_D was changed. Increasing the value of I_D increases the value of $\frac{W}{L}$ at a linear rate. The relationship between $\frac{W}{L}$ and I_D can be seen in Figure 7.1 Many of the equations for the small signal parameters are based on the value of $\frac{W}{L}$. As

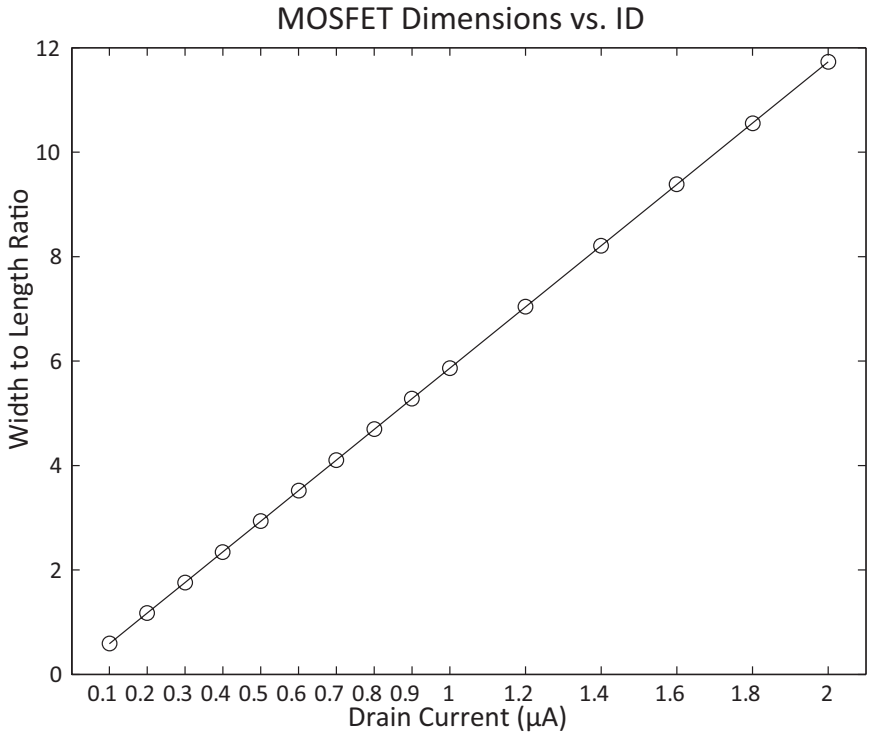

Figure 7.1: The relationship between the width to length ratio of a MOSFET and the drain current with the value of IC held constant at 1 (the middle of the moderate inversion region).

the width to length ratio increases, the small signals parameters change and the charts shown in Chapters 4, 5, and 6 do not remain the same. The following sections show the results of simulations across several levels of I_D.

7.1.1 Gain vs. Drain Current

The plots in Figure 7.2 show the effect of increasing drain current on the gain of the stage. Each plot has the same scale for the color gradient so that the behavior of the stage at higher currents can be quickly spotted. For example, on the far left plot the maximum gain is seen to fall at $IC_1 = 5.6$ and $IC_2 = 0.0005$. At these values of IC for $100nA$, the combination of r_{DS1} and

g_{M2} is at a maximum. As the drain current increases to $2\mu A$, the highest gain falls at a value of $IC_1 = 25$ and $IC_2 = 0.0005$. Overall, the gain drops as the drain current increases.

In addition to the figures presented here, more information has been collected on the relationship between the gain and the drain current. For the maximum and minimum gain of the stage at increasing drain current, Figures 7.10 and 7.11 as well as Tables 7.2 and 7.3 should be referenced (These figures are at the end of Chapter 7).

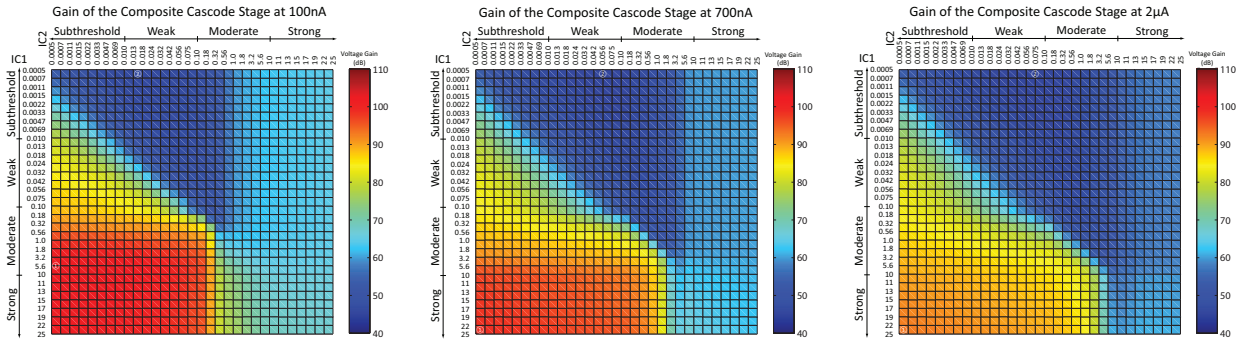

Figure 7.2: From left to right is the gain of the composite cascode stage at $100nA$, $700nA$, and $2\mu A$. Each plot is shown on the same scale to help visualize the change in gain vs. drain current. These plots are shown small here, but larger versions are available in Appendix C.

7.1.2 Bandwidth vs. Drain Current

The bandwidth of the stage vs. drain current has been plotted in a similar set of plots to those shown in Figure 7.2. The plots for bandwidth can be found in Figure 7.3. Increasing drain current has several similar effects on the bandwidth to those seen with the change in gain vs. drain current. The lowest bandwidth is always found in the lower left hand corner. Wide widths for M_2 increase the output capacitance of the composite cascode stage while long lengths for M_1 increase the value of r_{DS1}. This combination reduces the bandwidth of the stage very quickly. Maximum bandwidth is found at the point where the width to length ratio of M_2 is closest to 1. The capacitance of M_2 in the composite cascode stage as well as the low value of r_{DS1} for M_1 in subthreshold combine to give comparatively high bandwidth ($1.66MHz\ at\ 2\mu A$). The change in width to length ratio also moves the highest bandwidth peak towards larger values of IC_2 at higher drain current. Overall, the bandwidth increases with higher values of I_D.

In addition to the figures presented here, more information has been collected on the relationship between the bandwidth and the drain current. For the maximum and minimum bandwidth of the stage at increasing drain current, Figures 7.12 and 7.13 as well as Tables 7.4 and 7.5 should be referenced (These figures are at the end of Chapter 7).

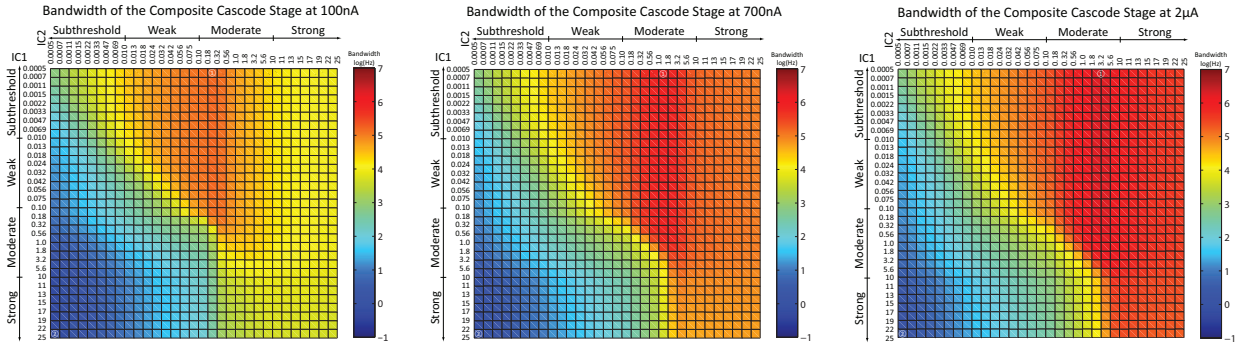

Figure 7.3: From left to right is the bandwidth of the composite cascode stage at $100nA$, $700nA$, and $2\mu A$. Each plot is shown on the same scale to help visualize the change in bandwidth vs. drain current. These plots are shown small here, but larger versions are available in Appendix C.

7.1.3 Overall Noise vs. Drain Current

Overall noise has been plotted at $100nA$, $700nA$, and $2\mu A$ in Figure 7.4. Two factors contribute to the locations of the maximum noise. First, noise is highest at higher values of gain so the plots look similar to those for gain shown in Figure 7.2. Second, noise is maximized when the area of the channel is small. When M_1 has a value of $\frac{W}{L} = 1$ the noise is very large. This is why the peak appears when M_1 is in the moderate inversion region for $100nA$ and moves into the strong inversion region for $I_D = 2\mu A$. Noise can be minimized by choosing larger dimensions for M_1 and by reducing the gain of the composite cascode stage.

In addition to the figures presented here, more information has been collected on the relationship between the total noise and the drain current. For the maximum and minimum total noise of the stage at increasing drain current, Figures 7.14 and 7.15 as well as Tables 7.6 and 7.7 should be referenced (These figures are at the end of Chapter 7).

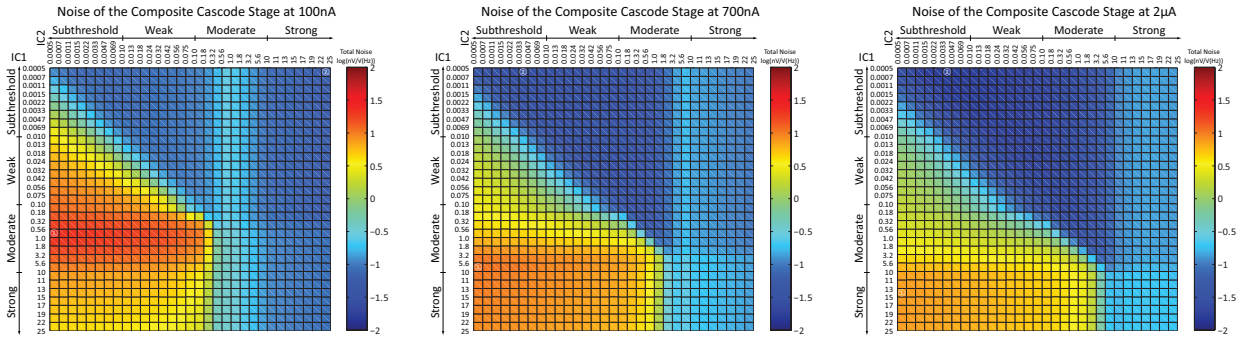

Figure 7.4: From left to right is the total noise of the composite cascode stage at $100nA$, $700nA$, and $2\mu A$. Each plot is shown on the same scale to help visualize the change in total noise vs. drain current. These plots are shown small here, but larger versions are available in Appendix C.

7.2 The General Design Methodology

Now that gain, bandwidth, and total noise of the composite cascode stage have been considered in detail, the design methodology can be outlined. The general design process is:

1. Choose a specific current draw for the composite cascode stage.

2. Select a value of IC_1 and IC_2 from the charts provided based on the desired operation of the stage.

3. Solve for the technology current (I_0) from Equation (2.2) using parameters from the target MOSFET technology.

4. Find the width to length ratio from Equation (2.3).

5. At this point the ratios of M_1 and M_2 have been selected. Extending the stage to the composite cascode loaded stage is very simple with Equations (3.2) and (3.3).

6. Finally, if a differential stage is desired, the following equalities are used:

   - $\frac{W_1}{L_1} = \frac{W_5}{L_5}$
   - $\frac{W_2}{L_2} = \frac{W_6}{L_6}$
   - $\frac{W_3}{L_3} = \frac{W_7}{L_7}$
   - $\frac{W_4}{L_4} = \frac{W_8}{L_8}$

7.3 Example Design of an Operational Amplifier

Presented in the next few sections is an operational amplifier for biomedical applications designed using the design methodology described above. Ideal current sources are used to simplify the design and show the behavior of the composite cascode input differential stage and voltage amplification stage (VAS). A few of the general parameters such as open loop gain, unity gain bandwidth, gain bandwidth product, phase margin, and gain margin are then discussed.

7.3.1 Design of the Differential Input Stage

According to the steps given in the previous section, the design of a composite cascode stage starts with the selection of the drain current. In order to reduce the power dissipation and increase the maximum gain, the drain current for the stage was chosen to be $100nA$. In addition to the drain current I chose a single sided voltage supply of $+5$ volts with the negative supply being ground. Since I am designing this example circuit for high gain, I chose $IC_1 = 5.6$ and $IC_2 = 0.0005$ from Figure C.1 in Appendix C.

The technology current of M_1 and M_2 can be found now that we know the inversion level of both devices. Using the drain current of $100nA$, $I_{01} = 254.61nA$, $I_{02} = 280.94nA$, $IC_1 = 5.6$, and $IC_2 = 0.0005$, the width to length ratio of both devices can be found using Equation (2.3). The resulting circuit and the plot of gain vs. frequency is shown in Figure 7.5. The value of V_{Bias} is set so that the value of V_{DS} from the drain of M_2 to the source of M_1 is $2.500V$.

At this point steps $1-4$ have been completed. The gain of the stage is very high at $A \approx 102dB$. In order to continue the design of the operational amplifier, the single-ended, current source loaded, composite cascode stage must be expanded to include a composite cascode load. Calculating the dimensions of M_3 and M_4 is very straight-forward. Since we know the dimensions of M_1 and M_2, M_3 and M_4 can be found through the ratio of the electron to hole mobility as shown in Chapter 3. Using a $\mu_n = 513.5602\frac{cm^2}{V-s}$ and a $\mu_p = 253.608\frac{cm^2}{V-s}$, the dimensions of M_3 and M_4 are found to be $\frac{W_3}{L_3} = \frac{2\mu m}{10\mu m}$ and $\frac{W_4}{L_4} = \frac{2000\mu m}{1\mu m}$. At this point, the schematic shown on the left in Figure 7.6 was simulated and the resulting output is shown on the right. V_{Bias} is left constant, and V_{Bias2} is set so that $100nA$ is supplied to the gain stage and the value of V_{DS} from the drain of M_2

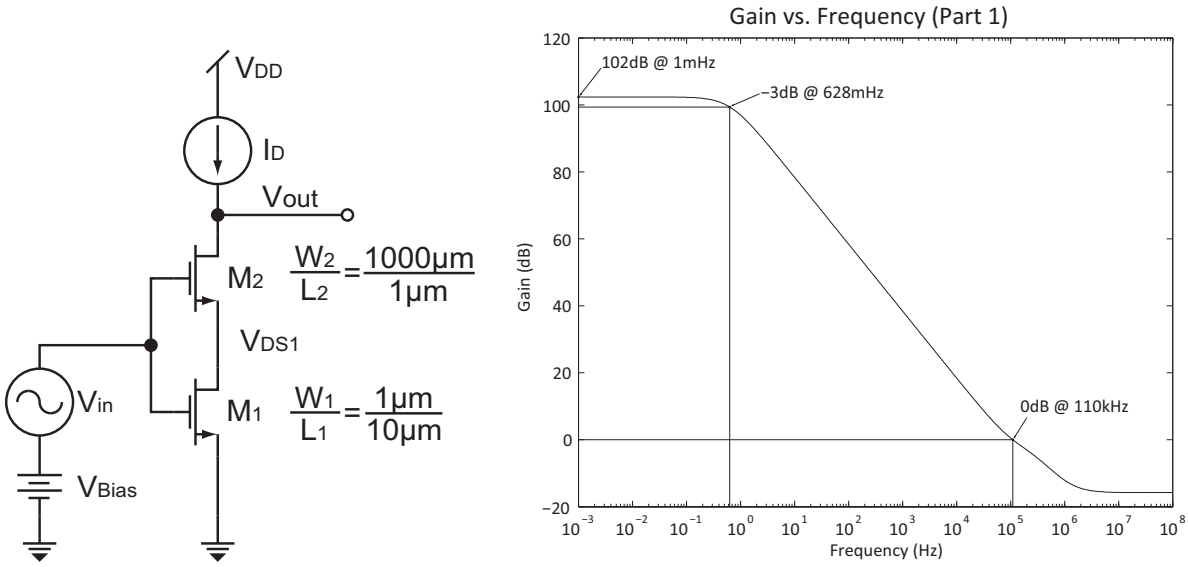

Figure 7.5: A schematic of the composite cascode stage with the dimensions of the devices is shown on the left and a plot of the gain vs. the frequency is shown on the right.

to the source of M_1 is $2.500V$. As expected, the gain is about $\frac{1}{2}$ of the single-ended, current source loaded stage.

Mirroring the single-ended composite cascode stage results in the differential stage. The P-Type devices are connected in a composite cascode current mirror, and the drain current is set by the ideal current source I_D in the schematic shown on the left in Figure 7.7. The values of V_{Bias+} and V_{Bias-} are equal. The gain stays constant in the transition from the single-ended to the differential stage although the corner frequency does drop by a little.

The differential stage with a composite cascode mirror load has been designed. High gain ($94dB$) and low bandwidth ($412mHz$) characteristic of an input stage has been achieved. At this point the VAS can be designed.

7.3.2 Design of the Voltage Amplification Stage

In order to design an effective VAS, the bandwidth should be higher and the gain should be lower. In order to get higher bandwidth I selected a drain current of $5\mu A$. This level of drain current should provide good bandwidth according to Figure 7.12. Since relatively high bandwidth is seen at the lower right hand corner of the IC vs. bandwidth chart, I chose values of $IC_1 = IC_2 = 438$.

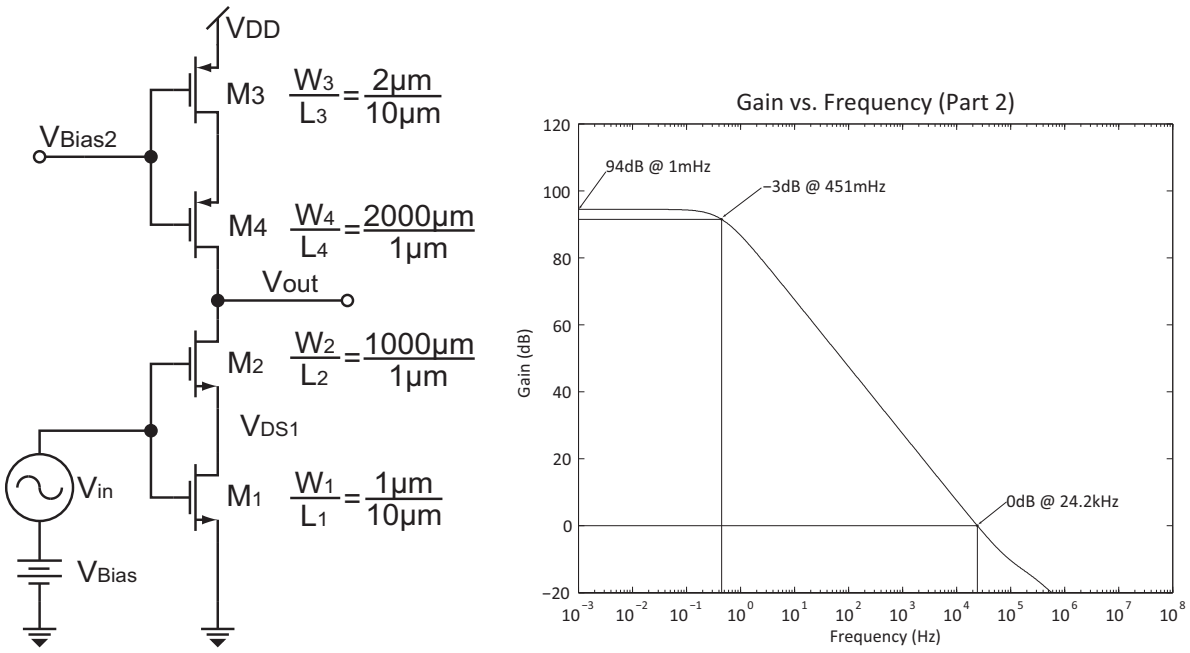

Figure 7.6: A schematic of the composite cascode stage with the dimensions of the devices is shown on the left and a plot of the gain vs. the frequency is shown on the right.

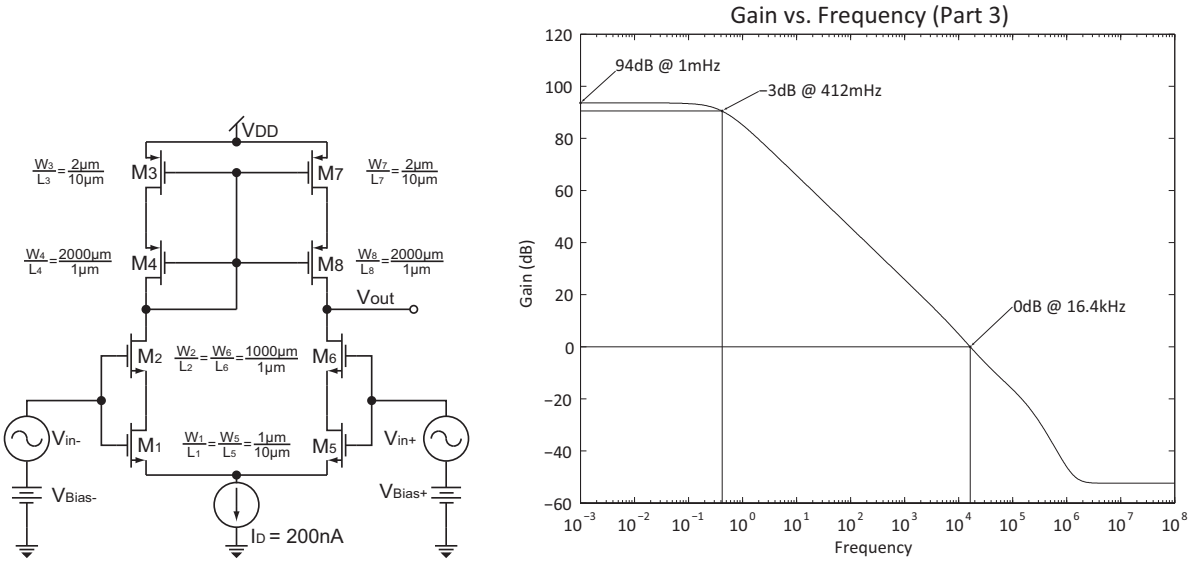

Figure 7.7: A schematic of the composite cascode stage with the dimensions of the devices is shown on the left and a plot of the gain vs. the frequency is shown on the right.

Although this is a very high value for *IC*, the level of the drain current is large enough to require deep strong inversion operation for lengths longer than widths. The resulting circuit, with an added unity gain output buffer stage, is shown in Figure 7.8 and the open loop gain vs. frequency simulation is shown in Figure 7.9. Also included is the phase vs. frequency simulations to show the good phase margin ($\approx 80^\circ$). Finally, the results of the design are shown in Table 7.1

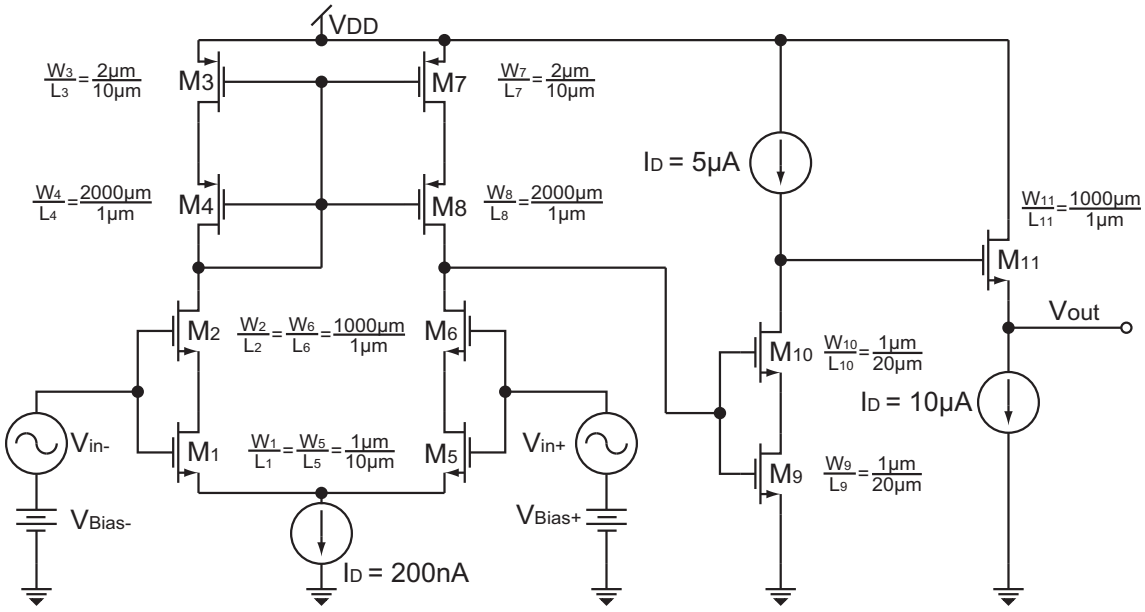

Figure 7.8: The final example op-amp used in explaining the composite cascode design methodology.

Table 7.1: A table showing the results of the example design using the design methodology for composite cascode stages.

Parameter	Value
Open Loop Gain	104dB
f_{-3dB} Point	0.403Hz
0 dB Crossover	40.7 kHz
Phase Margin	80°
Gain Margin	-26 dB at 575kHz
Unity Gain Bandwidth	146kHz

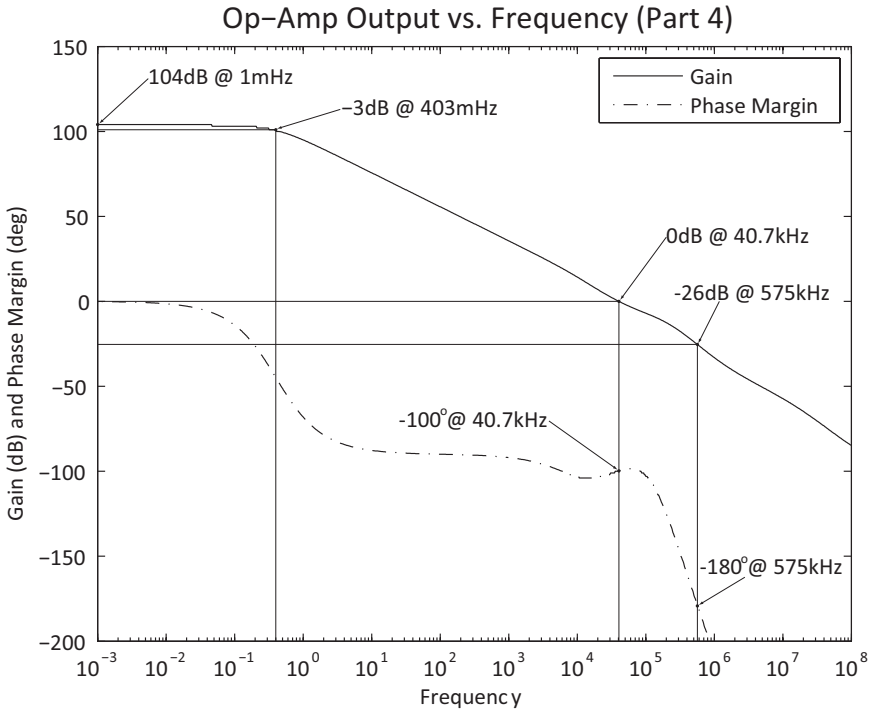

Figure 7.9: The simulation results from PSPICE for the circuit shown in Figure 7.8.

7.4 Summary

This chapter has presented three main ideas. The first is the relationship between the behavior of the composite cascode stages and the drain current. This information is then used in addition to that presented in Chapters 4, 5, and 6 to introduce the design methodology for composite cascode stages with the design charts. Finally, an example operational amplifier was designed as an example for the use of the design methodology.

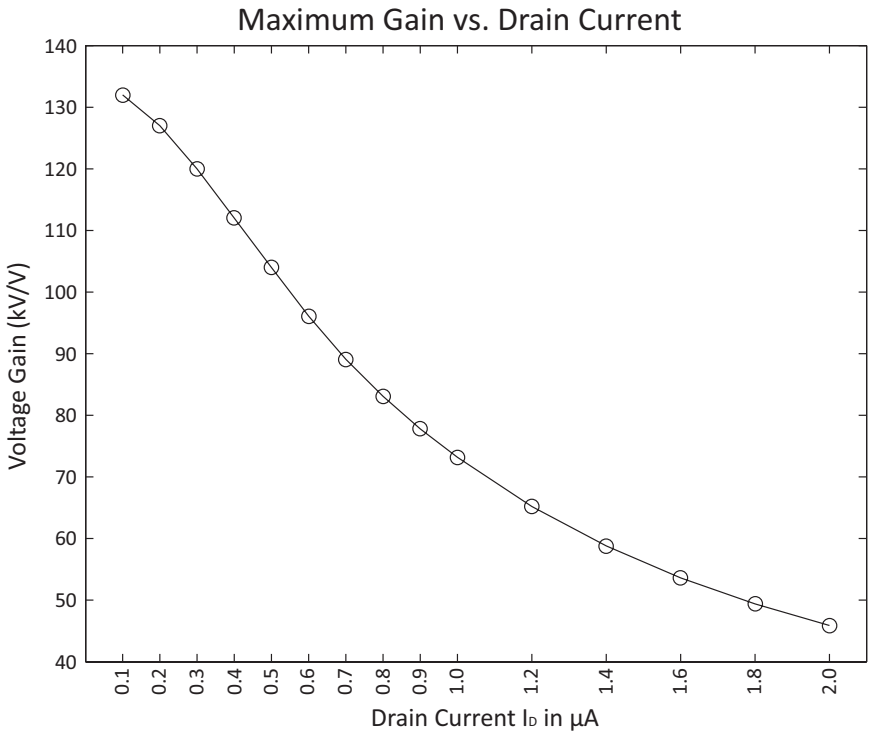

Figure 7.10: The maximum gain of the composite cascode stage with increasing drain current. Table 7.2 contains the inversion coefficients and MOSFET dimensions at each level of I_D.

Table 7.2: A table showing the inversion coefficient of M_1 and M_2 in relation to the maximum gain of the composite cascode stage. Increasing current leads to lower maximum gain.

I_D	IC_1	IC_2	$\frac{W}{L}$ for M_1	$\frac{W}{L}$ for M_2	Gain in $\frac{V}{V}$
100nA	5.6	0.0005	0.0699	709	132300
200nA	15	0.0005	0.0582	1418	127200
300nA	25	0.0005	0.0524	2127	120100
400nA	25	0.0005	0.0698	2836	112000
500nA	25	0.0005	0.0873	3545	103700
600nA	25	0.0005	0.105	4254	96060
700nA	25	0.0005	0.122	4964	89070
800nA	25	0.0005	0.140	5673	83060
900nA	25	0.0005	0.157	6382	77810
1.0μA	25	0.0005	0.175	7091	73150
1.2μA	25	0.0005	0.209	8509	65240
1.4μA	25	0.0005	0.244	9927	58800
1.6μA	25	0.0005	0.279	11345	53640
1.8μA	25	0.0005	0.314	12763	49380
2.0μA	25	0.0005	0.349	14182	45850

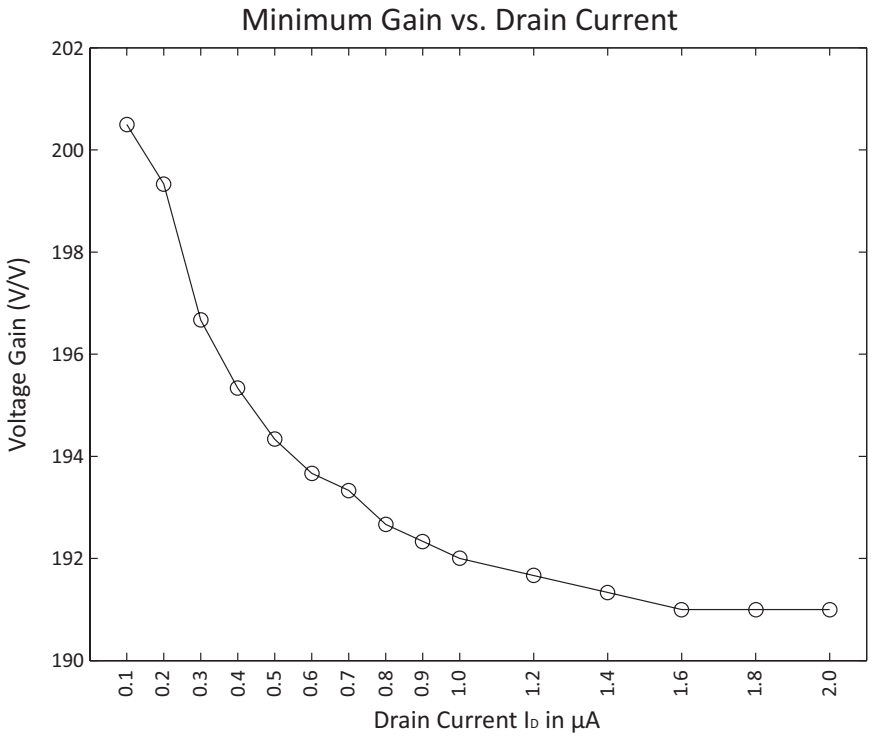

Figure 7.11: The minimum gain of the composite cascode stage with increasing drain current. Table 7.3 contains the inversion coefficients and MOSFET dimensions at each level of I_D.

Table 7.3: A table showing the inversion coefficient of M_1 and M_2 in relation to the minimum gain of the composite cascode stage. Increasing current leads to lower minimum gain.

I_D	IC_1	IC_2	$\frac{W}{L}$ for M_1	$\frac{W}{L}$ for M_2	Gain in $\frac{V}{V}$
100nA	0.0005	0.018	709	19.7	202.5
200nA	0.0005	0.024	1418	29.5	198.4
300nA	0.0005	0.032	2127	33.2	196.5
400nA	0.0005	0.032	2836	44.3	195.3
500nA	0.0005	0.042	3545	42.2	194.4
600nA	0.0005	0.042	4254	50.6	193.7
700nA	0.0005	0.056	4964	44.3	193.3
800nA	0.0005	0.056	5673	50.6	192.8
900nA	0.0005	0.056	6382	57.0	192.4
1.0μA	0.0005	0.056	7091	63.3	192.1
1.2μA	0.0005	0.056	8509	76.0	191.7
1.4μA	0.0005	0.075	9927	66.2	191.4
1.6μA	0.0005	0.075	11345	75.6	191.1
1.8μA	0.0005	0.075	12763	85.1	190.8
2.0μA	0.0005	0.075	14182	94.5	190.6

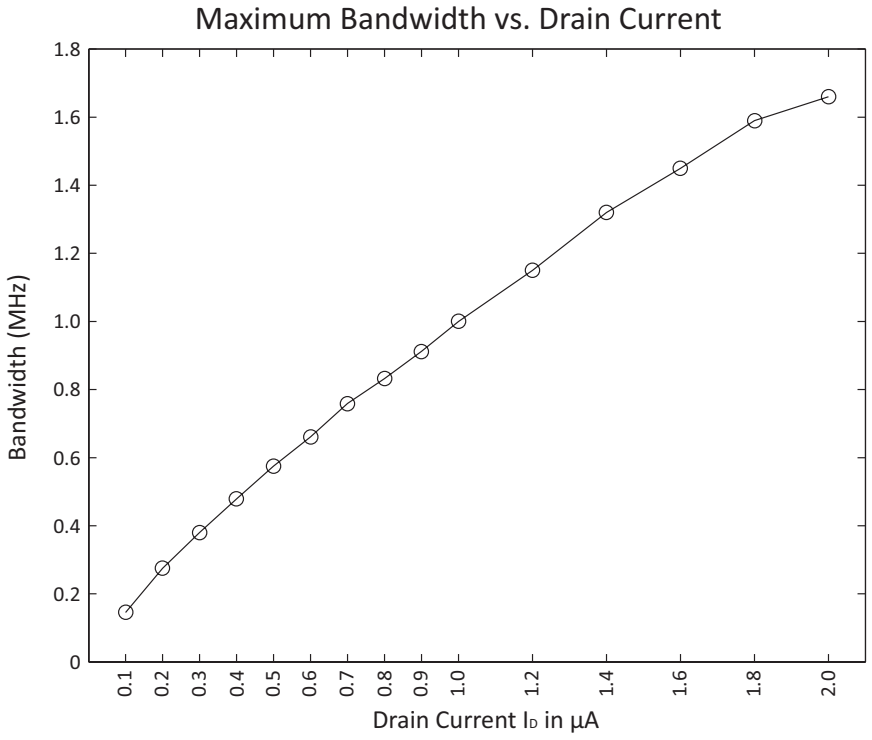

Figure 7.12: The maximum bandwidth of the composite cascode stage with increasing drain current. Table 7.4 contains the inversion coefficients and MOSFET dimensions at each level of I_D.

Table 7.4: A table showing the inversion coefficient of M_1 and M_2 in relation to the maximum bandwidth of the composite cascode stage. Increasing current leads to higher maximum bandwidth.

I_D	IC_1	IC_2	$\frac{W}{L}$ for M_1	$\frac{W}{L}$ for M_2	Bandwidth in MHz
100nA	0.0005	0.18	709	2.2	0.145
200nA	0.0005	0.32	1418	2.4	0.275
300nA	0.0005	0.56	2127	2.1	0.380
400nA	0.0005	0.56	2836	2.8	0.479
500nA	0.0005	0.56	3545	3.5	0.575
600nA	0.0005	1.0	4254	2.3	0.661
700nA	0.0005	1.0	4964	2.7	0.759
800nA	0.0005	1.0	5673	3.1	0.832
900nA	0.0005	1.0	6382	3.5	0.912
1.0μA	0.0005	1.8	7091	2.2	1.00
1.2μA	0.0005	1.8	8509	2.6	1.15
1.4μA	0.0005	1.8	9927	3.0	1.32
1.6μA	0.0005	1.8	11345	3.5	1.45
1.8μA	0.0005	1.8	12763	3.9	1.59
2.0μA	0.0005	1.8	14182	4.3	1.66

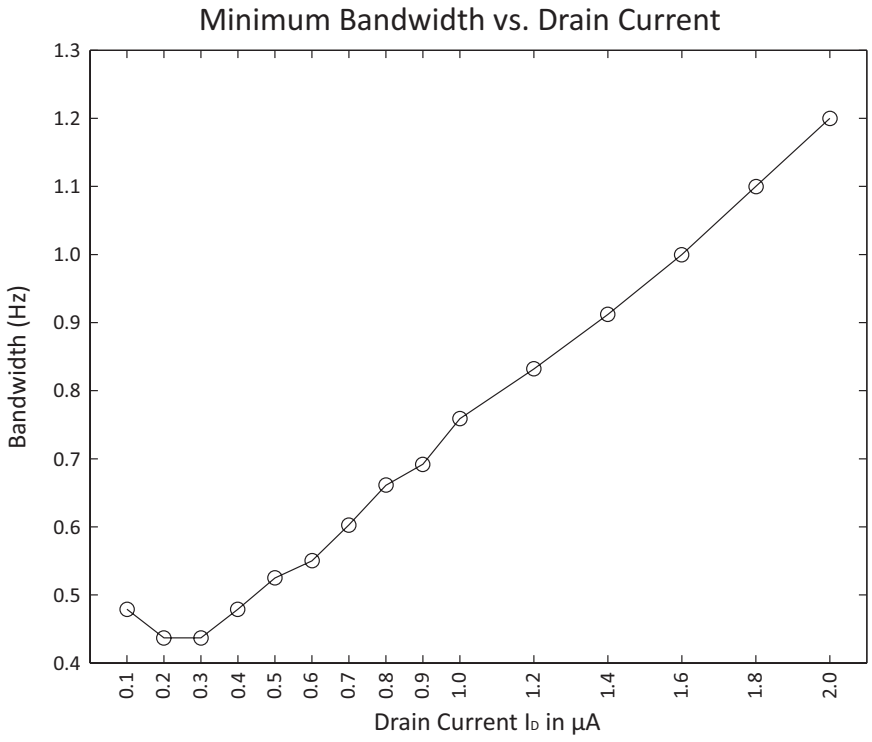

Figure 7.13: The minimum bandwidth of the composite cascode stage with increasing drain current. Table 7.5 contains the inversion coefficients and MOSFET dimensions at each level of I_D.

Table 7.5: A table showing the inversion coefficient of M_1 and M_2 in relation to the minimum bandwidth of the composite cascode stage. Increasing current leads to higher minimum bandwidth.

I_D	IC_1	IC_2	$\frac{W}{L}$ for M_1	$\frac{W}{L}$ for M_2	Bandwidth in Hz
100nA	25	0.0005	0.018	709	0.48
200nA	25	0.0005	0.035	1418	0.44
300nA	25	0.0005	0.052	2127	0.44
400nA	25	0.0005	0.070	2836	0.48
500nA	25	0.0005	0.087	3545	0.52
600nA	25	0.0005	0.105	4254	0.55
700nA	25	0.0005	0.122	4964	0.60
800nA	25	0.0005	0.140	5673	0.66
900nA	25	0.0005	0.157	6382	0.69
1.0μA	25	0.0005	0.175	7091	0.76
1.2μA	25	0.0005	0.209	8509	0.83
1.4μA	25	0.0005	0.244	9927	0.91
1.6μA	25	0.0005	0.279	11345	1.00
1.8μA	25	0.0005	0.314	12763	1.10
2.0μA	25	0.0005	0.349	14182	1.20

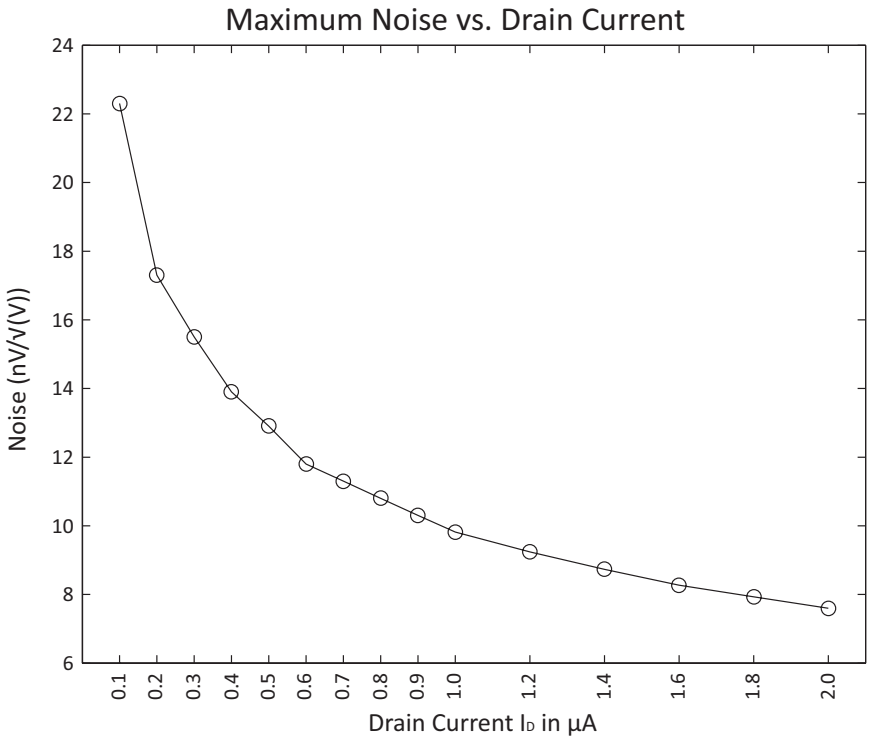

Figure 7.14: The maximum noise of the composite cascode stage with increasing drain current. Table 7.6 contains the inversion coefficients and MOSFET dimensions at each level of I_D.

Table 7.6: A table showing the inversion coefficient of M_1 and M_2 in relation to the maximum noise of the composite cascode stage. Increasing current leads to lower maximum noise.

I_D	IC_1	IC_2	$\frac{W}{L}$ for M_1	$\frac{W}{L}$ for M_2	Noise in $\frac{nV}{\sqrt{Hz}}$
100nA	0.56	0.0005	0.70	709	22.3
200nA	1.8	0.0005	0.43	1418	17.3
300nA	1.8	0.0005	0.65	2127	15.5
400nA	3.2	0.0005	0.49	2836	13.9
500nA	3.2	0.0005	0.61	3545	12.9
600nA	3.2	0.0005	0.73	4254	11.8
700nA	5.6	0.0005	0.49	4964	11.3
800nA	5.6	0.0005	0.56	5673	10.8
900nA	5.6	0.0005	0.63	6382	10.3
1.0μA	5.6	0.0005	0.70	7091	9.8
1.2μA	10	0.0005	0.52	8509	9.2
1.4μA	11	0.0005	0.56	9927	8.7
1.6μA	13	0.0005	0.54	11345	8.3
1.8μA	13	0.0005	0.60	12763	7.9
2.0μA	15	0.0005	0.58	14182	7.6

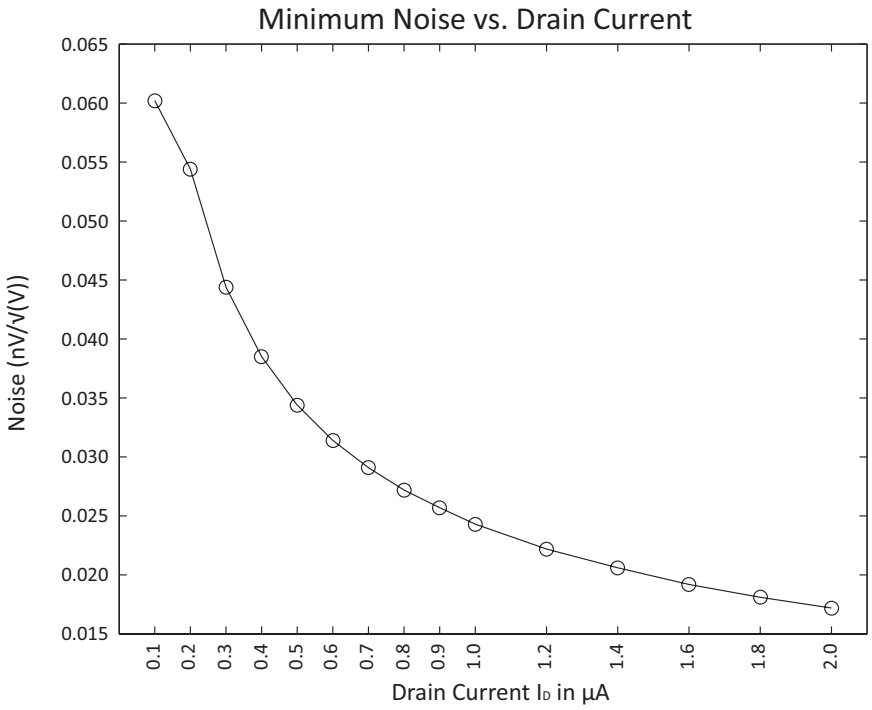

Figure 7.15: The minimum noise of the composite cascode stage with increasing drain current. Table 7.7 contains the inversion coefficients and MOSFET dimensions at each level of I_D.

Table 7.7: A table showing the inversion coefficient of M_1 and M_2 in relation to the minimum noise of the composite cascode stage. Increasing current leads to lower minimum noise.

I_D	IC_1	IC_2	$\frac{W}{L}$ for M_1	$\frac{W}{L}$ for M_2	Noise in $\frac{nV}{\sqrt{Hz}}$
100nA	0.0005	0.0033	709	107.4	0.060
200nA	0.0005	0.0033	1418	214.9	0.054
300nA	0.0005	0.0033	2127	322.3	0.044
400nA	0.0005	0.0033	2836	429.7	0.038
500nA	0.0005	0.0033	3545	537.2	0.034
600nA	0.0005	0.0033	4254	644.6	0.031
700nA	0.0005	0.0033	4964	752.0	0.029
800nA	0.0005	0.0033	5673	859.5	0.027
900nA	0.0005	0.0033	6382	966.9	0.026
1.0μA	0.0005	0.0033	7091	1074.4	0.024
1.2μA	0.0005	0.0033	8509	1289.2	0.022
1.4μA	0.0005	0.0033	9927	1504.1	0.021
1.6μA	0.0005	0.0033	11345	1719.0	0.019
1.8μA	0.0005	0.0033	12763	1933.8	0.018
2.0μA	0.0005	0.0033	14182	2148.7	0.017

CHAPTER 8. CONCLUSION

This thesis has presented a design methodology for use with composite cascode stages operating in the various regions of inversion. The design methodology allows for faster and more accurate design of ultra-low-power, high gain operational amplifier stages. The design methodology can be used with many different MOSFET technologies as the inversion coefficient is used in the main design process. The circuit designer only needs to know the desired operation and current draw of the stage in addition to the device parameters usually available in the simulation models. The original ”guess and simulate” approach is intended to be replaced by the design methodology presented in this thesis. The use of this methodology is shown through an example operational amplifier design in Chapter 7.

8.1 Topics for Future Research

Additional research into simpler methods for calculating the values of g_{DS} and other empirically derived parameters would provide a more mathematical approach to solving for the gain, bandwidth, and noise of the stage. Currently, equations are inaccurate, intensive, or simplify to transcendental functions. Also, additional research into the effects of short channels may provide more accuracy in composite cascode design with sub-$1\mu m$ channel lengths. Accurate design with smaller channel lengths and widths could reduce the size of the devices on chip.

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APPENDIX A. CHANNEL CONDUCTANCE IN THE ACTIVE REGION

The information in this appendix was obtained using the method described in [34]. Several different MOSFET dimensions were simulated and the results of those simulations are below. These figures are only valid when using the ON Semiconductor C5X 0.5μm model as this was the model used to populate the charts. Similar trends may exist in other models but the accuracy may not be good enough for actual design. The circuit used to extract this data is shown here in Figure A.1 where V_{DS} and V_{GS} are set to ensure active region operation.

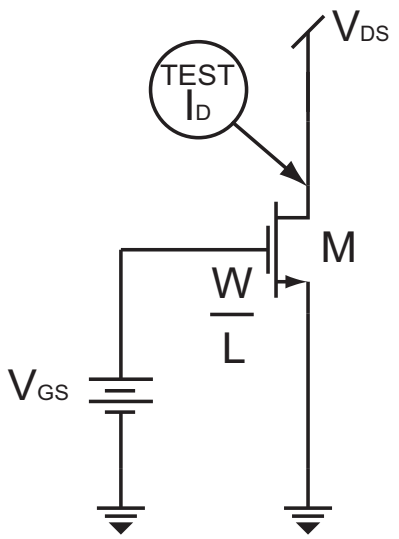

Figure A.1: Test circuit used in solving for the equation describing channel conductance. Adapted from [34].

The following sections will provide tables, graphs, and figures useful in solving for the value of g_{DS} for MOSFETs operating in the active region. If the MOSFET is in the triode region, the equation for g_{DS} in the triode region should be used for more accuracy. The general form of

the g_{DS} equation for active region operation is

$$g_{DS} = k(L)IC^{\alpha}. \tag{A.1}$$

A.1 Charts for Width Greater than Length

The first plot is a comparison of channel conductance versus inversion coefficient. Each of the lines corresponds to a different width for a length of $1\mu m$ and a height of $5\mu m$. Using the data in this graph, an equation for each of the lines can be extracted in the form of Eq. (A.1). The resulting functions are shown on the right hand side of the plot. The values recorded in this chart were chosen to provide accurate detail in areas that change more dramatically. Lower values for the width of the device cause faster changes in the value of $k(W)$. As can be seen from the resulting functions, the value of α is very constant. A value of 0.68 can be assumed for α without significant error.

The value of $k(W)$ changes with respect to the width of the device very linearly. If the values of $k(W)$ are plotted against their corresponding width, the graph in Figure A.3 can be found. The equation on the chart shows the linear regression result for the data collected. The equation for $k(W)$ based on MOSFET width is

$$k(W) = (22.807 * W - 34.9)\, nS, \tag{A.2}$$

where the result is given in Siemens, consistent with the units for the channel conductance. Using this function for $k(W)$ along with Eq. (A.1), an equation for g_{DS} in terms of width and inversion coefficient can be found. The result, for width greater than length, is

$$g_{DS} = (22.807 * W - 34.9) * IC^{0.68} nS. \tag{A.3}$$

A.2 Charts for Length Greater than Width

A similar approach is taken to that of the previous section. Using the same circuit as shown in Figure A.1, with width=$1\mu m$, and collecting data for g_{DS} versus inversion coefficient, Figure A.4 can be obtained. By using the same form of power regresssion as in the first section multiple

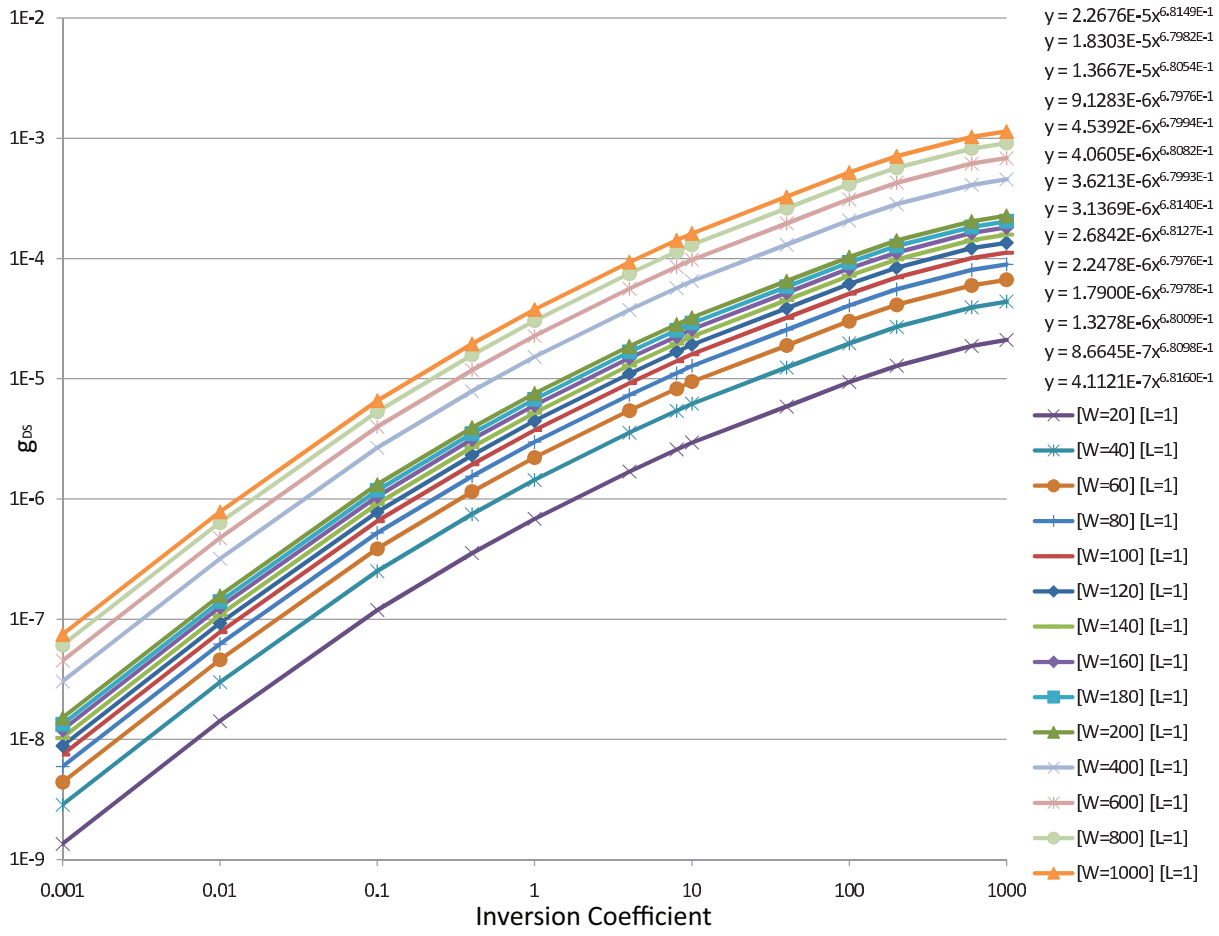

Figure A.2: Channel conductance versus inversion coefficient for width greater than length.

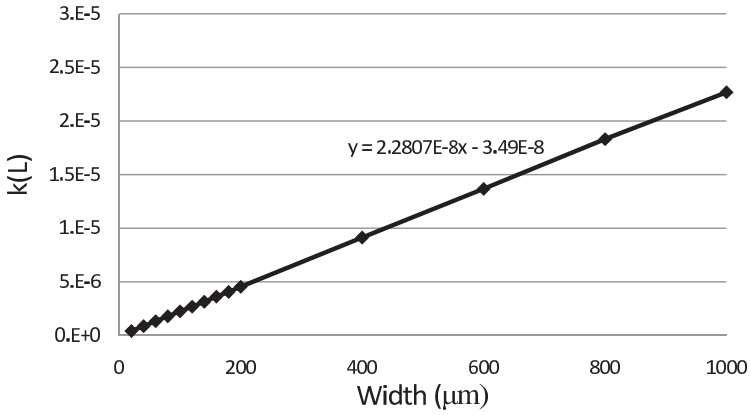

Figure A.3: k(W) term for channel conductance with width greater than length.

equations can be found to describe the change in g_{DS} versus inversion level. These equations are again displayed on the upper right side of the chart.

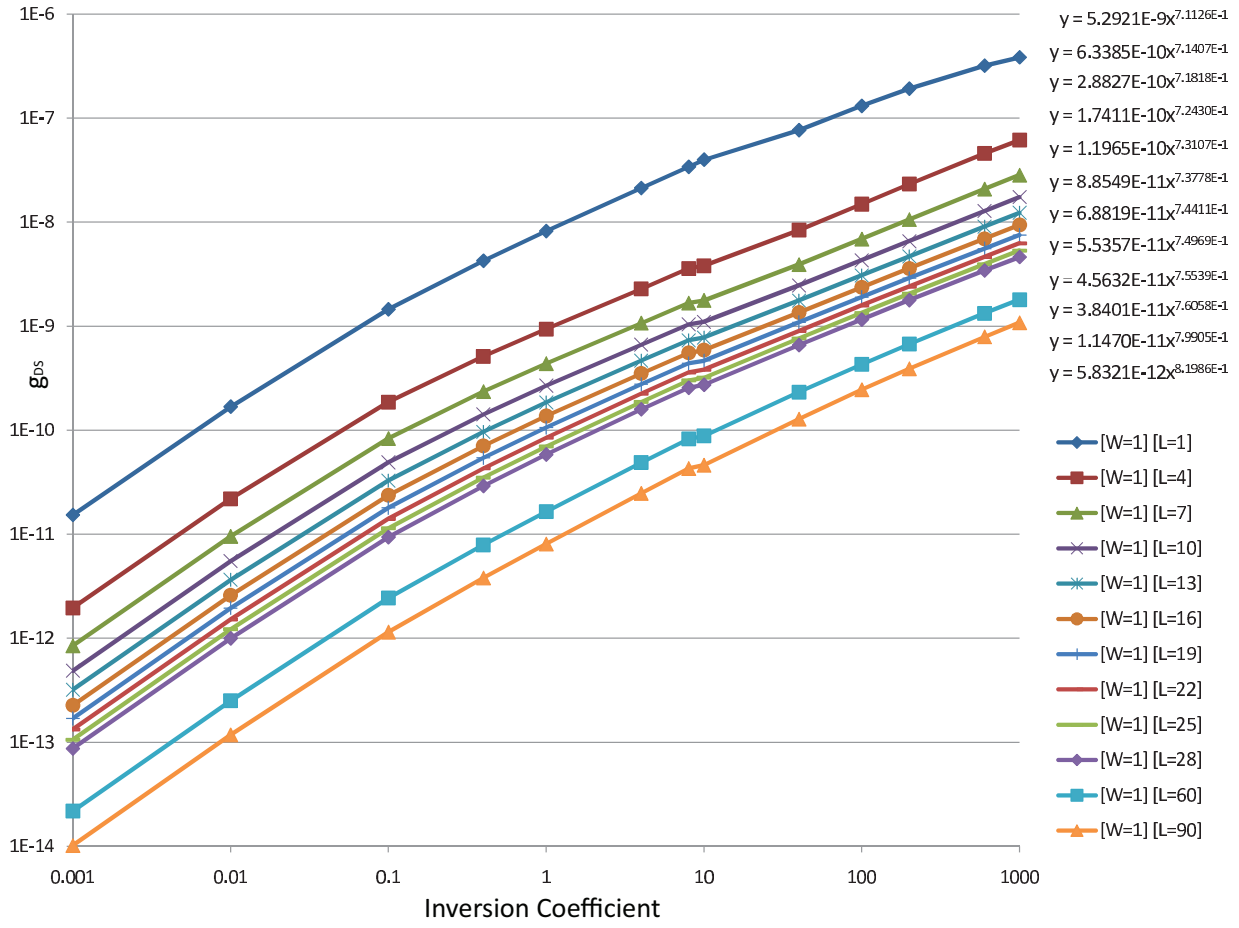

Figure A.4: Channel conductance versus inversion coefficient for length greater than width.

By creating a table of values consisting of $k(L)$ and α from the equations on the graph, equations for $k(L)$ and α can be found. The value of α changes too much to be able to assume a single value. An equation in terms of length for α must be found. By plotting the values as in Figure A.5 and finding the linear function to describe the points, an equation for α can be found. The function given on the chart is the description of α for various lengths. This equation is

$$\alpha = \left(1.274 * 10^{-3}\right) L + 0.71579, \tag{A.4}$$

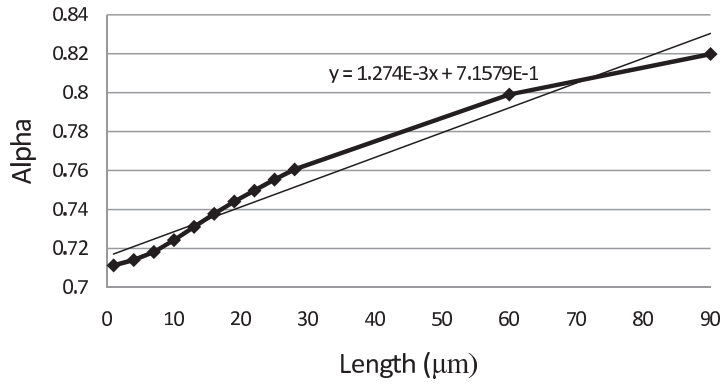

Figure A.5: The alpha term for MOSFETs with length greater than width.

where $k(L)$ is not a simple linear relationship. The value of $k(L)$ must be solved for using power regression. The plot of $k(L)$ versus MOSFET length is given in Figure A.6 and Equation (A.5) describes the value of $k(L)$ as MOSFET length increases.

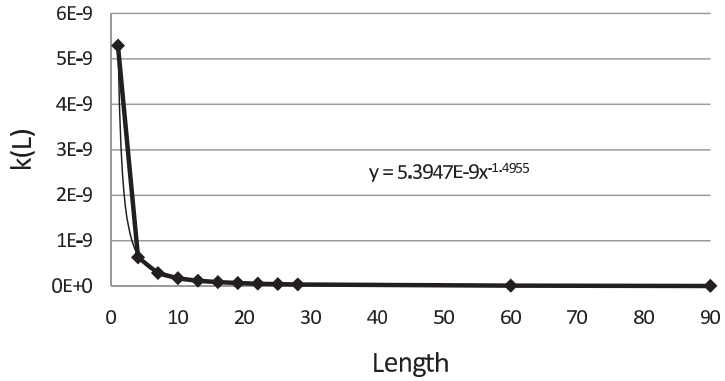

Figure A.6: k(L) term for channel conductance with length greater than width.

$$k(L) = \left(5.3947 * L^{-1.4955}\right) nS. \tag{A.5}$$

Combining Equations (A.4) and (A.5) into (A.1), a function for g_{DS} in terms of length and inversion coefficient can be found. This equation is

$$g_{DS} = \left(5.3947 * L^{-1.4955}\right) * IC^{\left(\left(1.274*10^{-3}\right)L+0.71579\right)} nS. \tag{A.6}$$

A.3 Charts for Width Equal to Length

Length changes the value of g_{DS} faster than the width. This causes the value of g_{DS} to drop as both width and length increase at the same rate. The chart of g_{DS} vs IC for width equal to length is given in Figure A.7

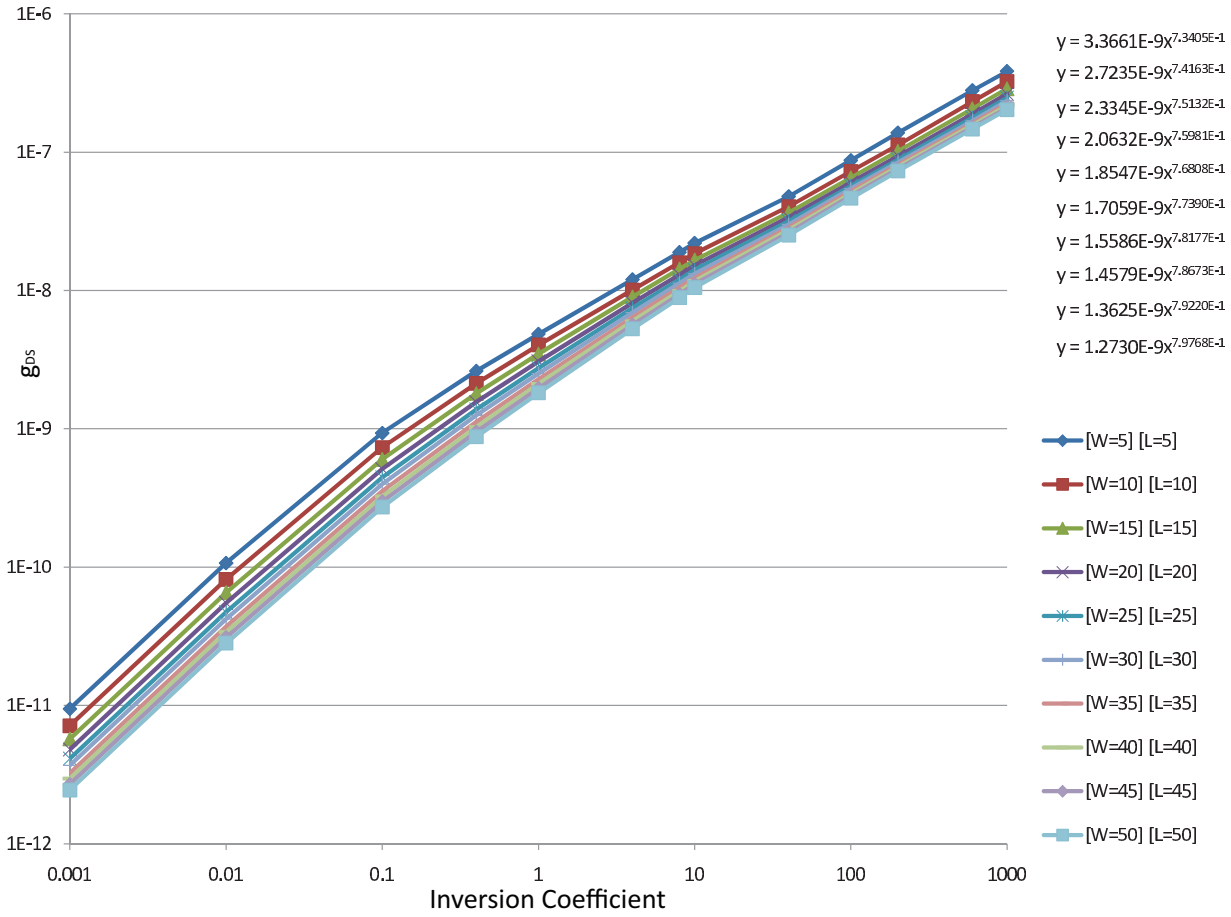

Figure A.7: Channel conductance versus inversion coefficient for width equal to length.

From the equations obtained through a power regression on the data collected, both α and $k(L)$ equations can be obtained. The values of α are plotted in Figure A.8 and the values of $k(L)$ are plotted in Figure A.9.

The equations for α and $k(L)$ are

$$\alpha = \left(1.4247 * 10^{-3}\right) L + 0.72954, \tag{A.7}$$

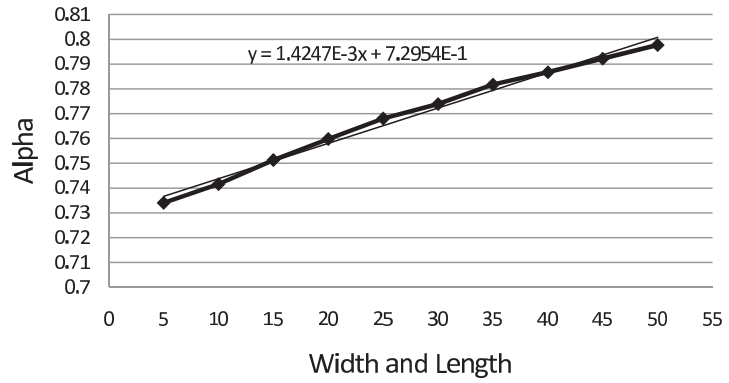

Figure A.8: The alpha term for MOSFETs with width equal to length.

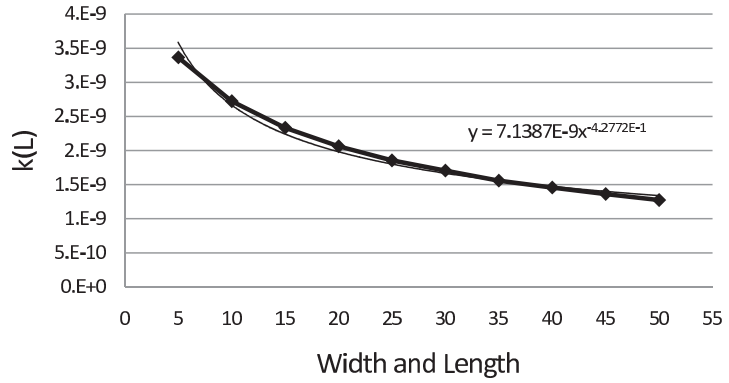

Figure A.9: k(L) term for channel conductance with width greater than length.

and

$$k(L) = \left(7.1387 * L^{-0.42772}\right) nS. \tag{A.8}$$

By combining these equations using Eq. (A.1), an equation for g_{DS} for width equal to length can be obtained. This equation is

$$g_{DS} = \left(7.1387 * L^{-0.42772}\right) * IC^{\left(\left(1.4247 * 10^{-3}\right)L + 0.72954\right)} nS. \tag{A.9}$$

A.4 A Final Note on this Procedure

As stated above, these results were obtained for the C5X model with the minimum width or length being $1\mu m$. If other sizes are needed, or if another model is used, more data needs to be

collected by the circuit designer in order to use similar equations. Alternatively, the designer can simply establish the bias voltages that is applied to the MOSFETs and find the value of g_{DS} from the DC operating points in the simulation results.

APPENDIX B. DERIVATIONS OF THE EQUATIONS

Each of the sections in this appendix will provide the derivation for a particular configuration of the composite cascode stage. The derivations are presented here as they are long and become distracting from the flow of the thesis.

B.1 Single Ended, Current Source Driven, Composite Cascode Stage

As was discussed previously in this thesis, the gain of the composite cascode stage is dependent on the operating region of M_1. When M_1 is in the active region the overall gain tends to be high. When M_1 is in the triode region the gain tends to be low but the bandwidth is higher. This section will derive the gain of the stage which can be used in all regions of operation, then show how it can be simplified if M_1 operation in the triode region is desired.

B.1.1 The Full Gain Equation

Using the small signal model shown in Figure B.1, the composite cascode gain equation can be derived. First, there are two nodes in this small signal model that need to be analyzed using Kirchhoff's current laws. The sum of all the current entering and leaving each node is found and a gain equation is derived from these node equations in terms of $\frac{V_{OUT}}{V_{IN}}$. The node equations are

Node 1:

$$0 = g_{M2}V_{GS2} - g_{MB2}V_{S2} + g_{DS2}\left(V_{OUT} - V_{S2}\right) + G_{LOAD}V_{OUT}, \tag{B.1}$$

and

Node 2:

$$0 = -g_{M2}V_{GS2} + g_{MB2}V_{S2} + g_{DS2}\left(V_{S2} - V_{OUT}\right) + g_{M1}V_{GS1} + g_{DS1}V_{S2}. \tag{B.2}$$

The gate to source voltage on M_1 and M_2 can be written in terms of V_{IN}. Since the source of M_1 is tied to ground, the value of V_{GS1} is equal to the value of V_{IN}. Because the source of M_2 is

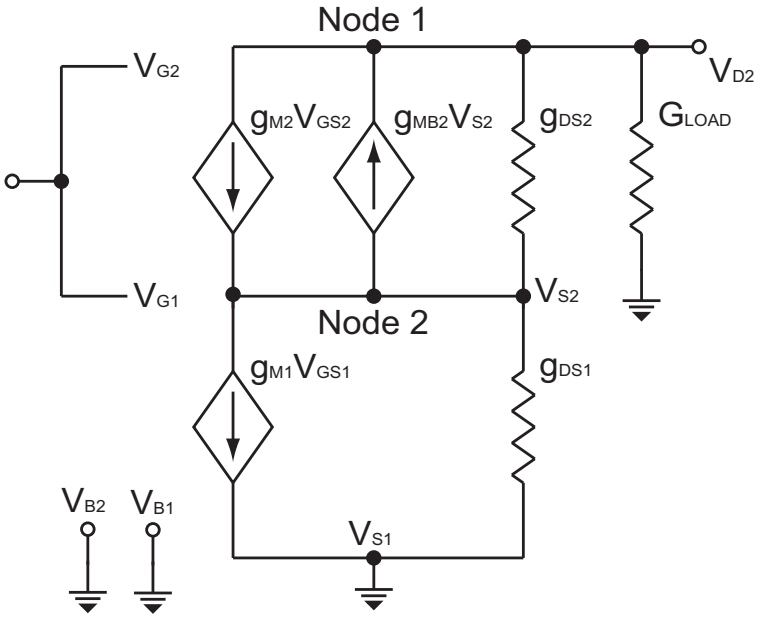

Figure B.1: The small signal model used in the gain calculation for the composite cascode stage.

not connected to ground, V_{GS2} must take into account the value of V_{S2}. The value of V_{GS2} is equal to $V_{IN} - V_{S2}$. Making these substitutions into the above node equations and solving for V_{S2}, the following equations are the result

Node 1:

$$V_{S2} = \frac{g_{M2}V_{IN} + (g_{DS2} + G_{LOAD})V_{OUT}}{g_{M2} + g_{MB2} + g_{DS2}}, \tag{B.3}$$

and

Node 2:

$$V_{S2} = \frac{(g_{M2} - g_{M1})V_{IN} + g_{DS2}V_{OUT}}{g_{M2} + g_{MB2} + g_{DS1} + g_{DS2}}. \tag{B.4}$$

The following steps show the general process used. The overall gain of the system is given in Equation (B.8). Setting both node equations (B.3) and (B.4) equal to each other gives

$$\frac{g_{M2}V_{IN} + (g_{DS2} + G_{LOAD})V_{OUT}}{g_{M2} + g_{MB2} + g_{DS2}} = \frac{(g_{M2} - g_{M1})V_{IN} + g_{DS2}V_{OUT}}{g_{M2} + g_{MB2} + g_{DS1} + g_{DS2}}. \tag{B.5}$$

Solve for V_{OUT}/V_{IN}, this gives

$$A_{MB} = \frac{V_{OUT}}{V_{IN}} = -\frac{g_{M1}g_{DS2} + g_{M2}g_{DS1} + g_{M1}(g_{M2} + g_{MB2})}{g_{DS1}g_{DS2} + (g_{M2} + g_{MB2} + g_{DS1} + g_{DS2})G_{LOAD}}. \tag{B.6}$$

Divide both top and bottom by $g_{DS1} * g_{DS2}$, which results in

$$A_{MB} = -\frac{\frac{g_{M1}}{g_{DS1}} + \frac{g_{M2}}{g_{DS2}} + \frac{g_{M1}(g_{M2}+g_{MB2})}{g_{DS1}g_{DS2}}}{1 + \frac{(g_{DS1}+g_{DS2}+g_{M2}+g_{MB2})G_{LOAD}}{g_{DS1}g_{DS2}}}. \tag{B.7}$$

Substituting $\frac{1}{r_{DS}}$ for g_{DS} and $\frac{1}{R_{LOAD}}$ for G_{LOAD} simplifies the solution and puts it into a more readable format. The final gain equations is

$$A_{MB} = -\frac{g_{M1}r_{DS1} + g_{M2}r_{DS2} + g_{M1}\left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}}{1 + \frac{1}{R_{LOAD}}\left(r_{DS1} + r_{DS2} + \left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}\right)}. \tag{B.8}$$

If an ideal current source with infinite impedance is assumed, the value of R_{LOAD} becomes infinite. The denominator of equation (B.8) goes to 1 and the resulting equation is

$$A_{MB} = -\left[g_{M1}r_{DS1} + g_{M2}r_{DS2} + g_{M1}\left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}\right]. \tag{B.9}$$

These equations can be used when both M_1 and M_2 are operating in the active or triode region. The value of $\left[g_{M1}\left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}\right]$ tends to be very high, usually becoming the only non-neglible term in the gain equation [17].

B.1.2 Lower Device in the Triode Region

When the MOSFET M_1 is in the triode region the small signal model of the lower device is more accurately described by Figure 2.7. This results in an overall small signal model more similar to Figure B.2. The lower device acts as a voltage variable resistor rather than an amplifying element. This increases the output resistance of the stage which increases the gain slightly. For the most part the composite cascode stage with the lower device in the triode region acts as a common source amplifier. The derivation of the gain equation for this configuration is very similar to that given in Appendix B.1.1. The current entering and leaving each node is

Node 1:

$$0 = g_{M2}V_{GS2} - g_{MB2}V_{S2} + g_{DS2}\left(V_{OUT} - V_{S2}\right) + G_{LOAD}V_{OUT}, \tag{B.10}$$

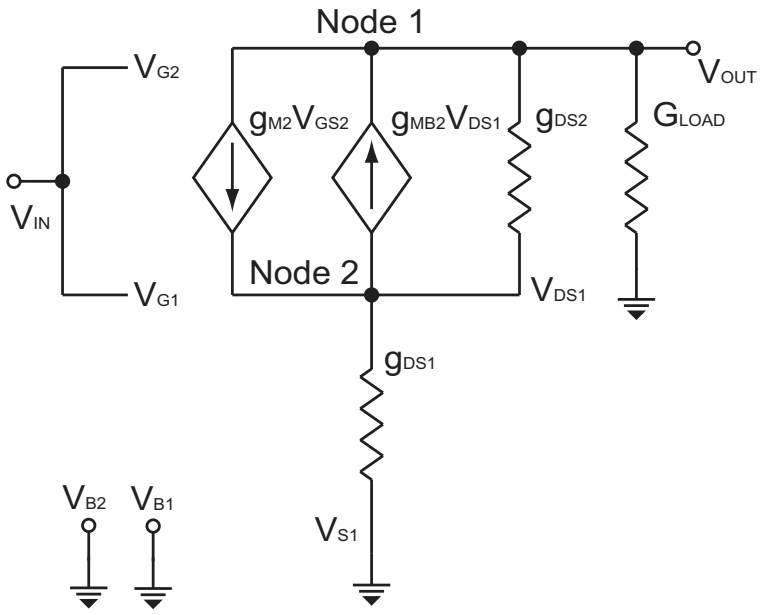

Figure B.2: The small signal model used in the gain calculation for the composite cascode stage with the lower device in the triode region. The transconductance and body conductance are removed for the lower device to emphasize the fact that deep in the triode region these values become very small (often negligible).

and

Node 2:

$$0 = -g_{M2}V_{GS2} + g_{MB2}V_{S2} + g_{DS2}\left(V_{S2} - V_{OUT}\right) + g_{M1}V_{GS1} + g_{DS1}V_{S2}. \tag{B.11}$$

Solving equations (B.10) and (B.11) for V_{S2} and noting that $V_{GS1} = V_{IN}$ and $V_{GS2} = V_{IN} - V_{S2}$ gives

Node 1:

$$V_{S2} = \frac{V_{OUT}\left(G_{LOAD} + g_{DS2}\right) + V_{IN}g_{M2}}{g_{M2} + g_{MB2} + g_{DS2}}, \tag{B.12}$$

and

Node 2:

$$V_{S2} = \frac{V_{OUT}g_{DS2} + V_{IN}g_{M2}}{g_{DS1} + g_{DS2} + g_{M2} + g_{MB2}}. \tag{B.13}$$

The following work shows the general process used in the derivation of composite cascode gain with M_1 in the triode region with Equation (B.16) showing the final equation. Setting the

Node 1 and 2 equations equal to each other and solving for V_{OUT}/V_{IN} gives

$$\frac{V_{OUT}\left(G_{LOAD}+g_{DS2}\right)+V_{IN}g_{M2}}{g_{M2}+g_{MB2}+g_{DS2}}=\frac{V_{OUT}g_{DS2}+V_{IN}g_{M2}}{g_{DS1}+g_{DS2}+g_{M2}+g_{MB2}}. \tag{B.14}$$

Solving for V_{OUT}/V_{IN} results in

$$A_{MB}=\frac{V_{OUT}}{V_{IN}}=-\frac{g_{M2}g_{DS1}}{g_{DS1}g_{DS2}+G_{LOAD}\left(g_{DS1}+g_{DS2}+g_{M2}+g_{MB2}\right)}. \tag{B.15}$$

Substituting $\frac{1}{r_{DS}}$ for g_{DS} and $\frac{1}{R_{LOAD}}$ for G_{LOAD} simplifies the solution and puts it into a more readable format. The final gain equations is

$$A_{MB}=-\frac{g_{M2}r_{DS2}}{1+\frac{1}{R_{LOAD}}\left(r_{DS1}+r_{DS2}+\left(g_{M2}+g_{MB2}\right)r_{DS1}r_{DS2}\right)}. \tag{B.16}$$

When the impedance from the load approaches infinity, the denominator of equation (B.16) approaches 1. This leaves

$$A_{MB}=-g_{M2}r_{DS2}, \tag{B.17}$$

as the gain. The overall gain is much smaller when M_1 is in the triode region because there is no gain from M_1 to be multiplied with the gain from M_2.

B.2 Composite Cascode Output Impedance

The impedance of the composite cascode stage is derived as follows. Two equations can be written to describe the currents entering the two nodes in Figure B.3. These equations are

Node 1:

$$0=g_{DS2}\left(V_{TEST}-V_{DS1}\right)-\left(g_{M2}+g_{MB2}\right)V_{DS1}-I_{TEST}, \tag{B.18}$$

and

Node 2:

$$0=\left(g_{M2}+g_{MB2}\right)V_{DS1}+g_{DS2}\left(V_{DS1}-V_{TEST}\right)+g_{DS1}V_{DS1}. \tag{B.19}$$

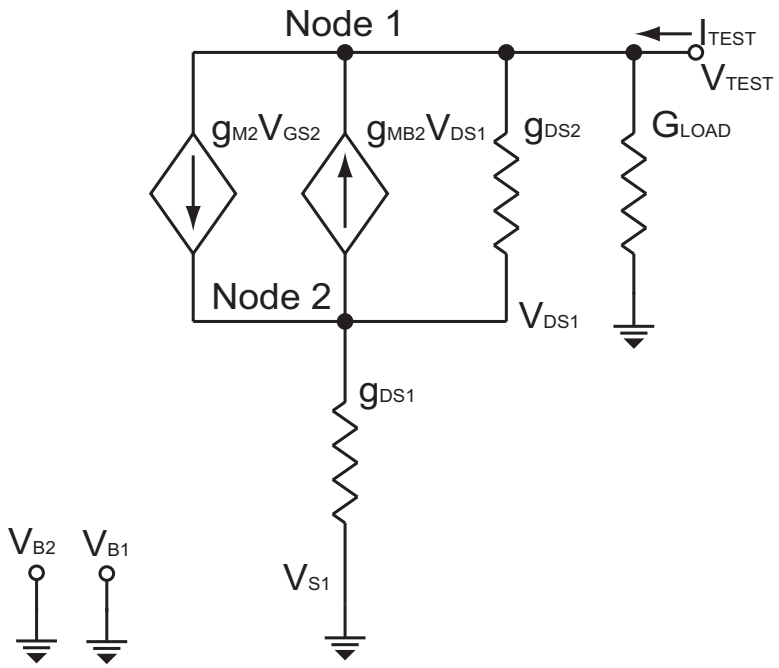

Figure B.3: The small signal model used in the impedance calculation for the composite cascode stage with the lower device in either the active or triode region. The gate to source voltage is DC only as it is biased to a particular reference voltage.

Equation (B.20) through (B.23) show the steps taken to solve for the impedance of the composite cascode stage. Solving Equation (B.19) for V_{DS1} gives

$$V_{DS1} = \frac{g_{DS2} V_{TEST}}{g_{DS1} + g_{DS2} + g_{M2} + g_{MB2}}. \tag{B.20}$$

This function is substituted into Equation (B.18), which gives the result as

$$\frac{I_{TEST}}{V_{TEST}} = \frac{g_{DS2}\left(g_{DS1} + g_{DS2} + g_{M2} + g_{MB2}\right) - g_{DS2}^2 - g_{DS2}\left(g_{M2} + g_{MB2}\right)}{g_{DS1} + g_{DS2} + g_{M2} + g_{MB2}}. \tag{B.21}$$

Grouping like terms, noting that $Z_{TEST} = \frac{V_{TEST}}{I_{TEST}}$, and simplifying gives

$$Z_{TEST} = \frac{1}{g_{DS1}} + \frac{1}{g_{DS2}} + \frac{g_{M2} + g_{MB2}}{g_{DS1} g_{DS2}}. \tag{B.22}$$

Replacing $\frac{1}{g_{DS}}$ with r_{DS} give the final solution as

$$Z_{TEST} = r_{DS1} + r_{DS2} + \left(g_{M2} + g_{MB2}\right) r_{DS1} r_{DS2}. \tag{B.23}$$

Because the value of g_{M1} and g_{MB1} are neglected, equation (B.23) is valid when M_1 is operating in either the active or the triode region.

APPENDIX C. FULL-SIZED BEHAVIOR VS. DRAIN CURRENT FIGURES

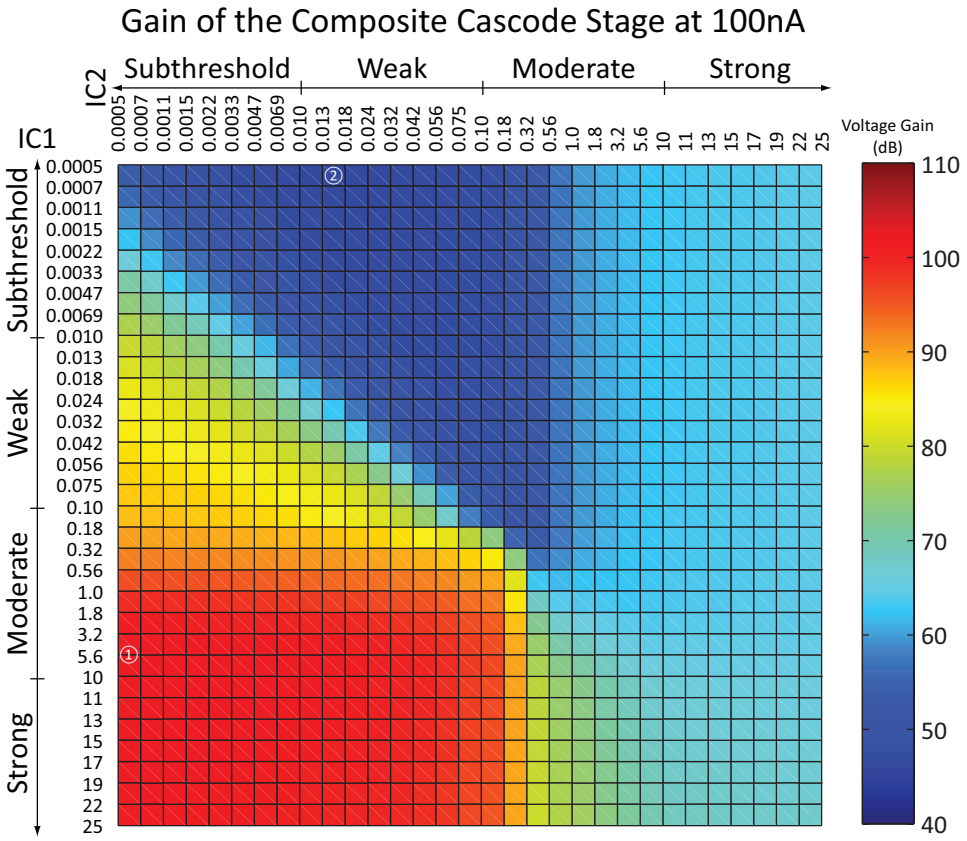

Figure C.1: A chart showing the magnitude of the gain (in dB) with respect to the inversion level of M_1 and M_2 with a drain current of $100nA$

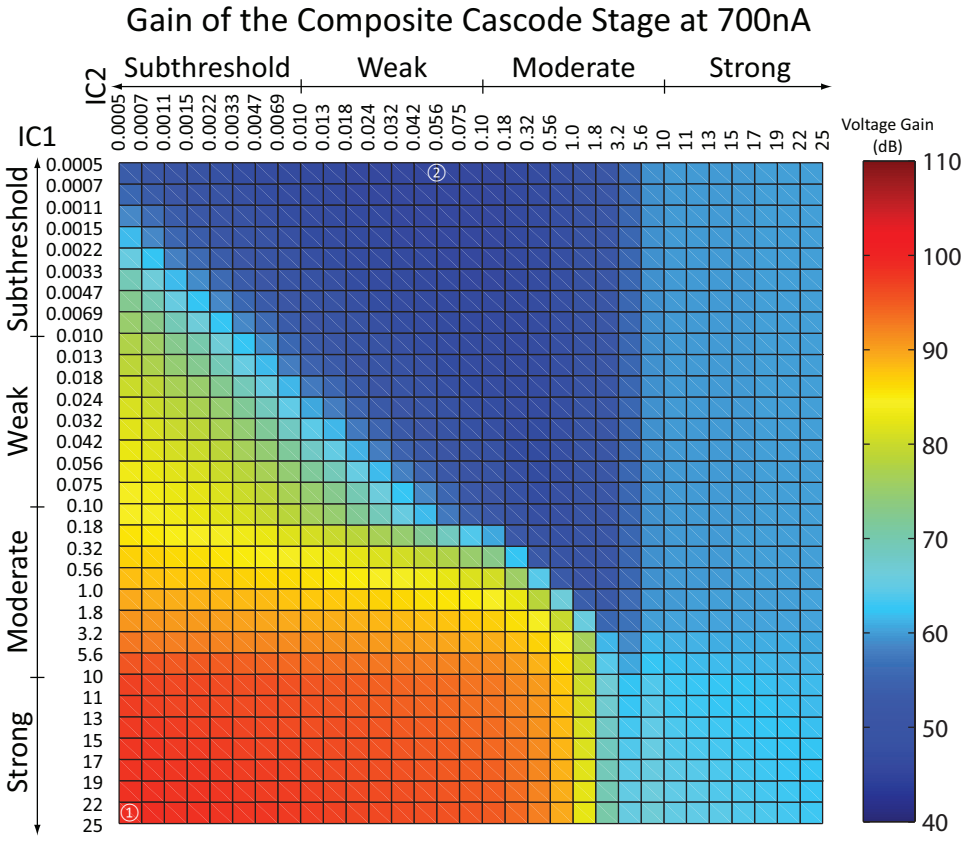

Figure C.2: A chart showing the magnitude of the gain (in dB) with respect to the inversion level of M_1 and M_2 with a drain current of $700nA$

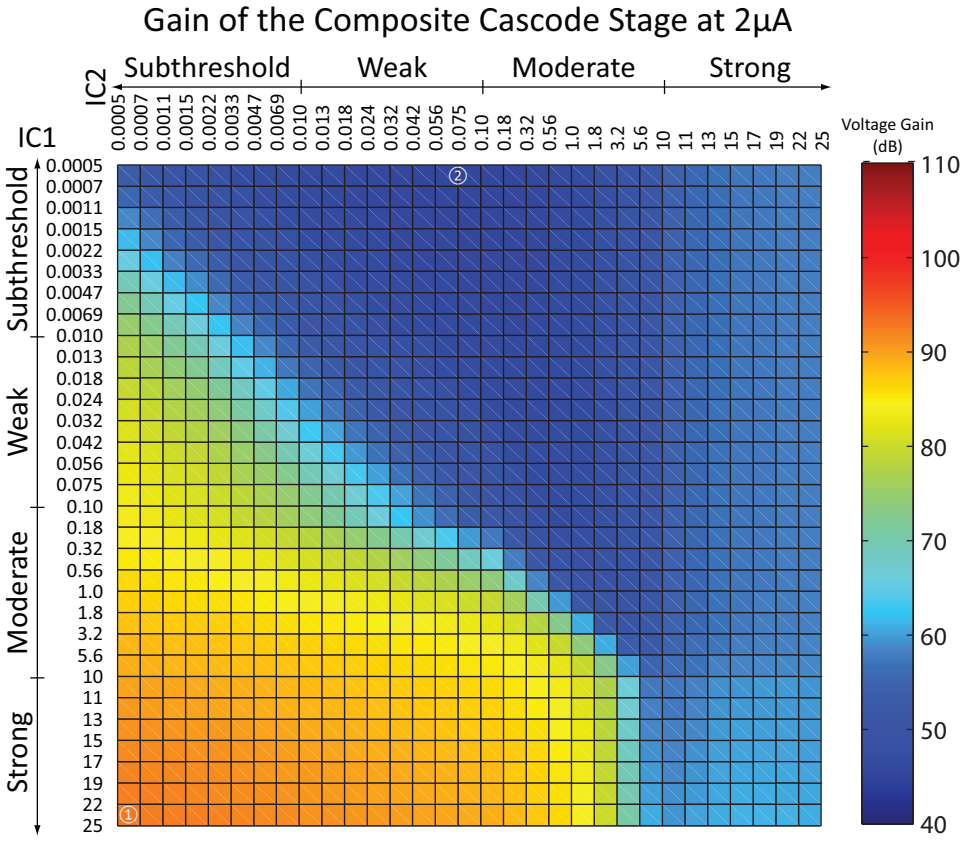

Figure C.3: A chart showing the magnitude of the gain (in dB) with respect to the inversion level of M_1 and M_2 with a drain current of $2\mu A$

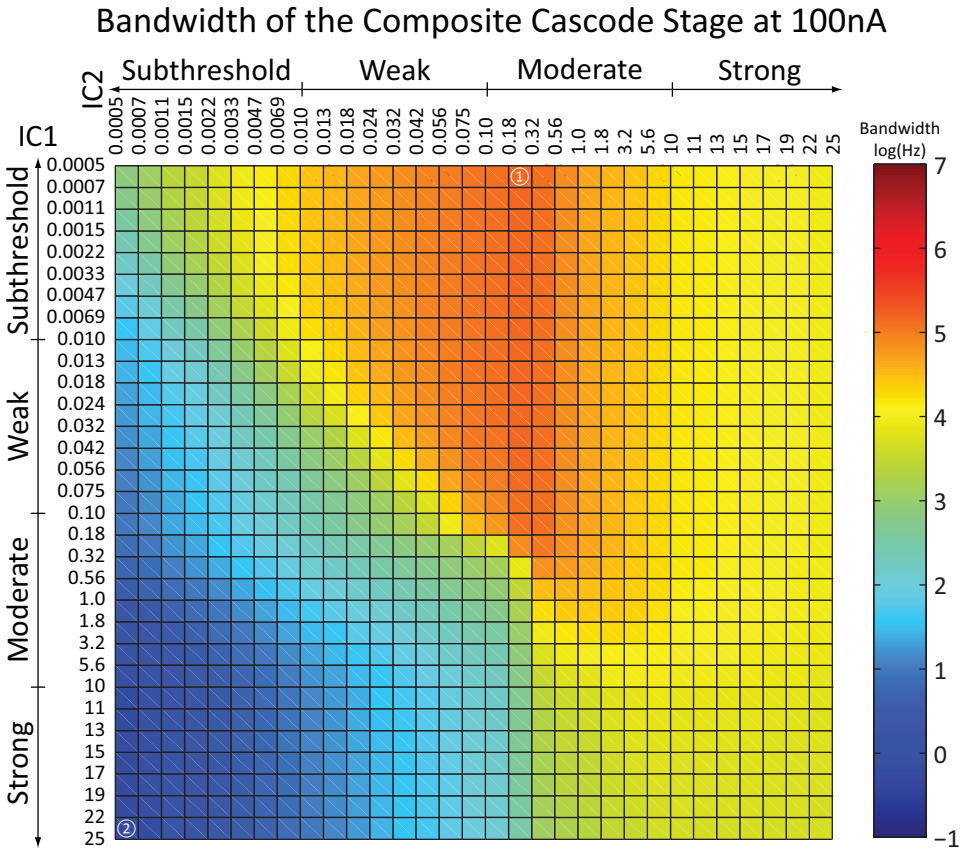

Figure C.4: A chart showing the magnitude of the bandwidth (in $log_{10}(Hz)$) with respect to the inversion level of M_1 and M_2 with a drain current of $100nA$

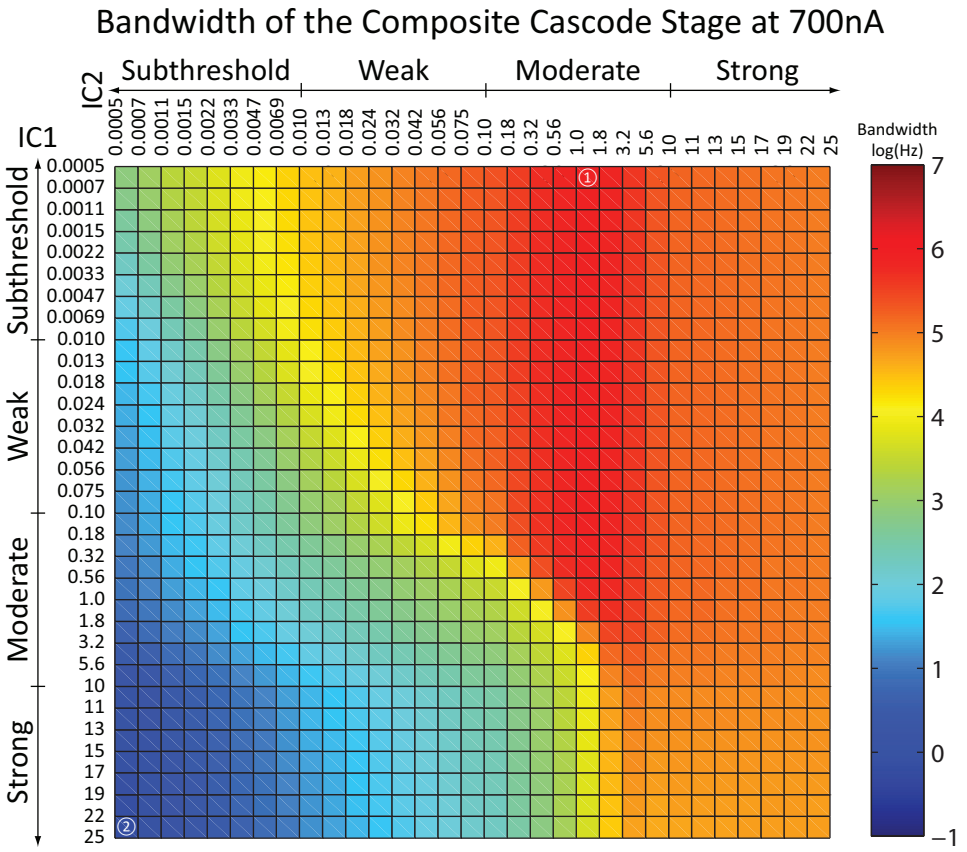

Figure C.5: A chart showing the magnitude of the bandwidth (in $log_{10}(Hz)$) with respect to the inversion level of M_1 and M_2 with a drain current of $700nA$

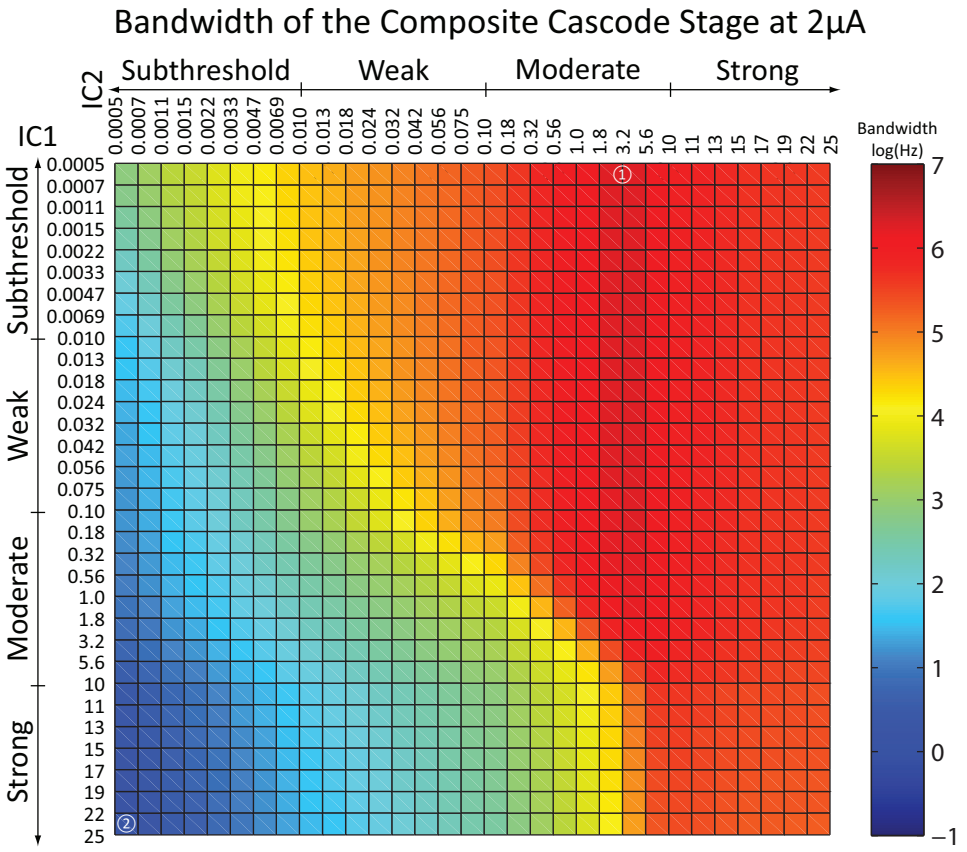

Figure C.6: A chart showing the magnitude of the bandwidth (in $log_{10}(Hz)$) with respect to the inversion level of M_1 and M_2 with a drain current of $2\mu A$

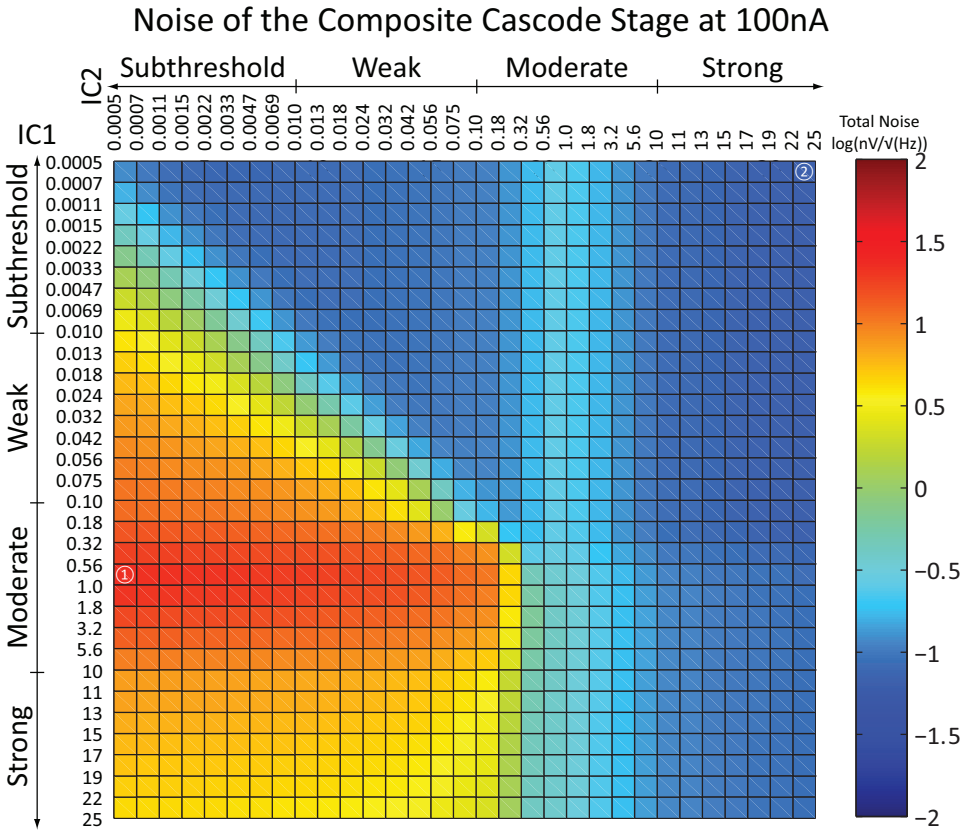

Figure C.7: A chart showing the magnitude of the total noise (in $log_{10}(nV/\sqrt{Hz})$) with respect to the inversion level of M_1 and M_2 with a drain current of $100nA$

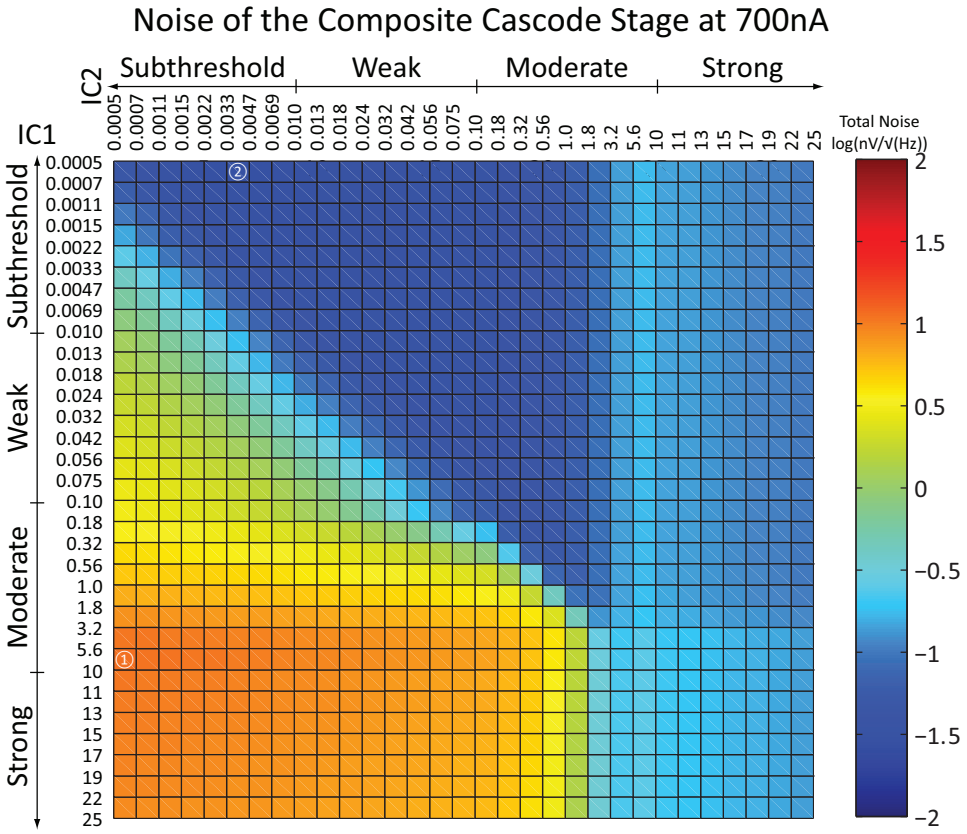

Figure C.8: A chart showing the magnitude of the total noise (in $log_{10}(nV/\sqrt{Hz})$) with respect to the inversion level of M_1 and M_2 with a drain current of $700nA$

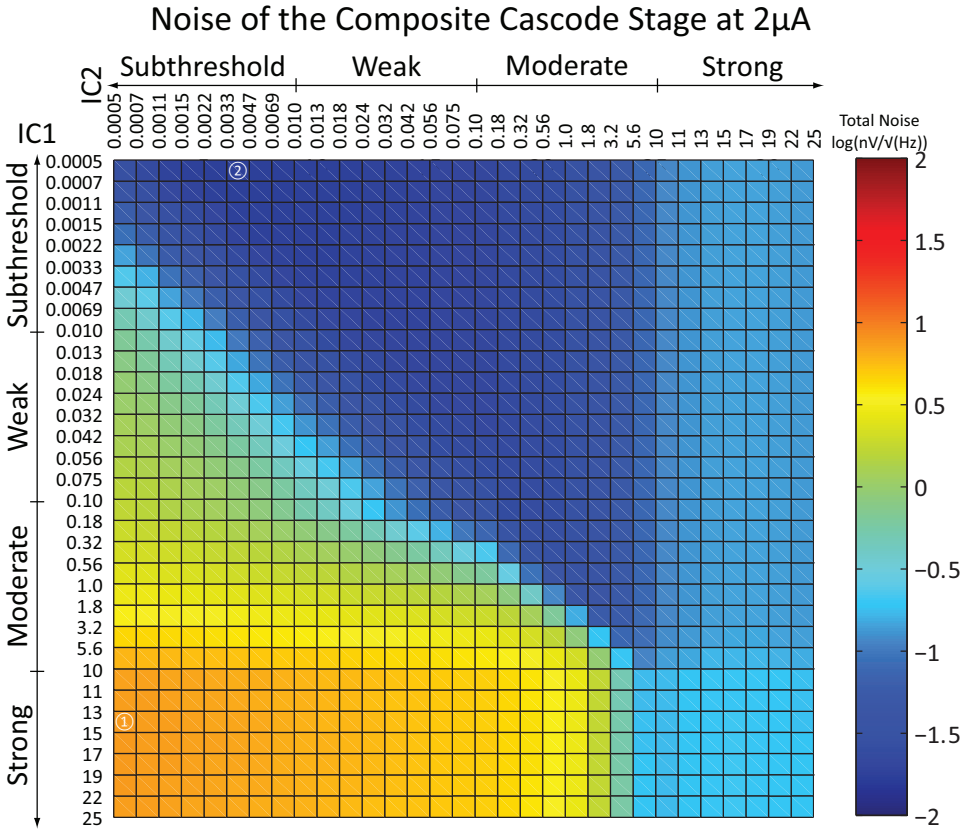

Figure C.9: A chart showing the magnitude of the total noise (in $log_{10}(nV/\sqrt{Hz})$) with respect to the inversion level of M_1 and M_2 with a drain current of $2\mu A$