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A WIDEBAND PRECISION QUADRATURE PHASE SHIFTER

Steve T. Noall

A thesis submitted to the faculty of
Brigham Young University
in partial fulfillment of the requirements for the degree of

Master of Science

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ABSTRACT

A WIDEBAND PRECISION QUADRATURE PHASE SHIFTER

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Department of Electrical and Computer Engineering

Master of Science

A new circuit is proposed that uses an RC-CR filter in a feedback configuration to achieve a wideband precision quadrature phase shift with constant amplitude response. Such a circuit can be used to perform image rejection in a low IF receiver using the Hartley method. Simulation results show that the circuit can achieve an average image rejection ratio of 50 dB over a 16 MHz bandwidth. The feedback loop enables the circuit to maintain high accuracy over process and temperature.

Keywords: image rejection, quadrature generation, wideband, gain matching, low IF, 802.11a, Hartley method, RC-CR filter, frequency detection

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Chapter 1

Introduction

Low intermediate frequency (IF) receivers inherently suffer from a noise signal called the image that is created during the first downconversion of the radio frequency (RF) signal. This noise signal must be sufficiently suppressed in order to recover the signal of interest. One method of rejecting the image signal is the Hartley method. This method requires a precise quadrature phase shift with constant amplitude response in order to achieve a high image rejection ratio (IRR). An RC-CR filter is a popular method of performing the phase shift over a small bandwidth. RC-CR filters have a phase shift of 90° at all frequencies, but can only achieve reasonably constant amplitude response over a narrow bandwidth.

This thesis introduces a new circuit which uses an RC-CR filter in a feedback configuration in order to produce a wideband quadrature phase shift with constant amplitude response. The feedback loop measures and corrects the gain error by means of a pair of level detectors, a differential amplifier, and a pair of voltage-controlled resistors (VCRs). This automatic error correction gives good performance over process and temperature. The circuit is fully differential, which is a requirement for most RF receivers.

1.1 Thesis Outline

Chapter 2 contains an analysis of the rise of RF CMOS and a description of several modern wireless technologies. Chapter 3 discusses the three most popular RF receiver architectures and their respective strengths and weaknesses. The most relevant of these to this thesis is the low IF architecture, where the proposed circuit would find application. Chapter 4 analyzes the problem of the image signal, as well as the popular methods of image rejection. Chapter 5 introduces the proposed circuit, including a system-level mathematical analysis and a presentation of the CMOS implementation. Chapter 6 analyzes the simulation results

and compares the performance to that of other systems. Chapter 7 concludes this thesis with suggestions for future research.

1.2 Contributions

The contributions of this thesis include:

- The design of a wideband precision quadrature phase shifter with equal amplitude response that achieves an IRR of 50 dB over process and temperature
- A method of frequency detection without using a PLL

Chapter 2

Wireless Communications Overview

This chapter begins by reviewing the rise of CMOS circuits in RF applications, which historically has been dominated by bipolar technology. Most of this information and all of the figures from this section come from an RF CMOS survey published in 2004 by Asad A. Abidi from UCLA [1]. Section 2.2 gives a technical overview of some of today's popular wireless standards, including the 802.11 family, Bluetooth, and Zigbee.

2.1 The Rise of RF CMOS

RF circuits are the oldest form of electronics to see widespread commercialization. They were originally dominated by vacuum tubes until semiconductor devices gained prominence. When semiconductor devices eventually found their way into RF circuits, bipolar transistors were the technology of choice for several decades. CMOS has claimed considerable market share of RF transceivers in the past decade, led in many cases by work done by pioneering university researchers. This section reviews several key milestones that have made CMOS a contender in today's RF market.

By the time academic interest began to develop in RF CMOS in the early 1990s, bipolar was a mature RF technology. RF bipolar performance was good, and new, low-risk products with fast time-to-market could be developed by using the well understood superheterodyne architecture. CMOS, on the other hand, struggled to operate at RF frequencies and completely lacked integrated inductors. The motivation for transitioning to CMOS is not immediately apparent, but RF CMOS held the future promise of lower cost and higher levels of integration.

Transitioning to CMOS was not a matter of simply replacing bipolar transistors with FETs in established circuit structures. Rather, it required new and innovative architectures

that minimized the weaknesses of CMOS compared to bipolar and exploited its strengths. University researchers freely explored new technologies that were considered too high-risk to industry. The first RF CMOS amplifier was reported in 1993 [2]. The circuit was a 2 μm CMOS differential pair that used inductive loads to produce 20 dB of gain at 900 MHz, which was an extremely high operating frequency at the time. The circuit is most notable for the first successful use of inductors in a CMOS process. Practical CMOS inductors were not available up to this point because the heavily doped CMOS substrate caused unacceptably high self-capacitance and eddy current losses in the spiral inductor. This problem was solved by replacing the substrate under the inductor with a wet selective etch. Many improved CMOS inductors followed [3, 4]. Practical CMOS inductors allowed for the use of the matched impedance, low-noise tuned amplifier, shown in Fig. 2.1.

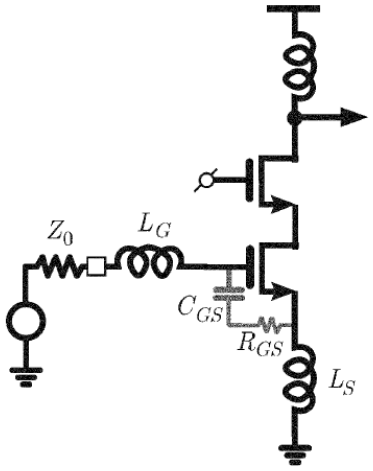

Figure 2.1: Low noise amplifier.

This circuit, called a low-noise amplifier (LNA), uses inductors and intrinsic MOS capacitance to provide a tuned input impedance of 50 ohms. The source-degenerated cascode configuration provides very high gain with a very low noise figure. The LNA is a fundamental RF building block and is found at the front end of virtually all RF CMOS receivers.

Another ubiquitous RF component is the mixer, which provides frequency translation. The first RF CMOS mixer was also reported in 1993 [5], and used a switched capacitor

track-and-hold circuit to perform signal downconversion. By sampling an RF signal at twice the modulation bandwidth, the resulting discrete-time analog signal represents the desired channel. This approach suffered from input noise aliasing, and would be replaced with a circuit topology similar to the bipolar double-balanced mixer. Despite their architectural similarities, the CMOS version relies on analog switching and is fundamentally different to the operation of the bipolar mixer.

Because of the mixed-signal nature of many CMOS designs, it is often essential for designers to use differential topologies to reject common-mode noise. Differential oscillators were thus an intuitive choice for RF CMOS voltage-controlled oscillators (VCOs). Shown in Fig. 2.2, LC VCOs were first implemented using bond-wire inductors [6] and later with on-chip spiral inductors [7].

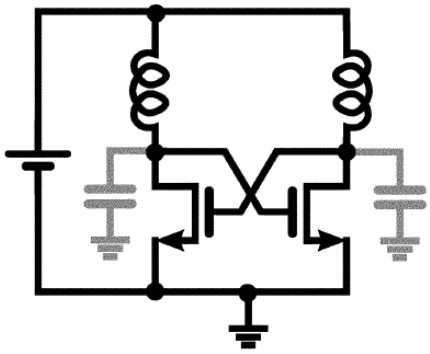

Figure 2.2: LC voltage-controlled oscillator.

Due to the low resonator quality factor (Q), the phase noise of early RF CMOS VCOs was quite poor compared to their discrete bipolar counterparts. Further research into inductor Q revealed that a heavily doped substrate contributed to low Q through eddy current losses [8]. CMOS substrates were typically heavily doped to avoid latch-up problems, but a new generation of lightly doped substrates became available that offered low substrate loss with surprisingly minimal risk of latch-up. As research continued, CMOS VCOs were discovered to have several important advantages. First, MOSFETs can support oscillation amplitudes of 2Vdd without junction forward-biasing. Second, MOSFET varactors can

withstand these large amplitude swings without failure. Oscillator phase noise is inversely proportional to the square of the amplitude, which explains why CMOS VCOs are able to perform so well in spite of low inductor Q.

The unique switching property of MOSFETs gives CMOS VCOs a superior tuning range. A technique known as band switching uses MOSFETs as switches to enable the discrete switching of capacitive elements in an LC tank. Shown in Fig. 2.3, this allows the VCO to operate over several different frequency ranges by switching capacitors in and out of the VCO LC tank. Band switching is a standard technique in commercial CMOS VCOs.

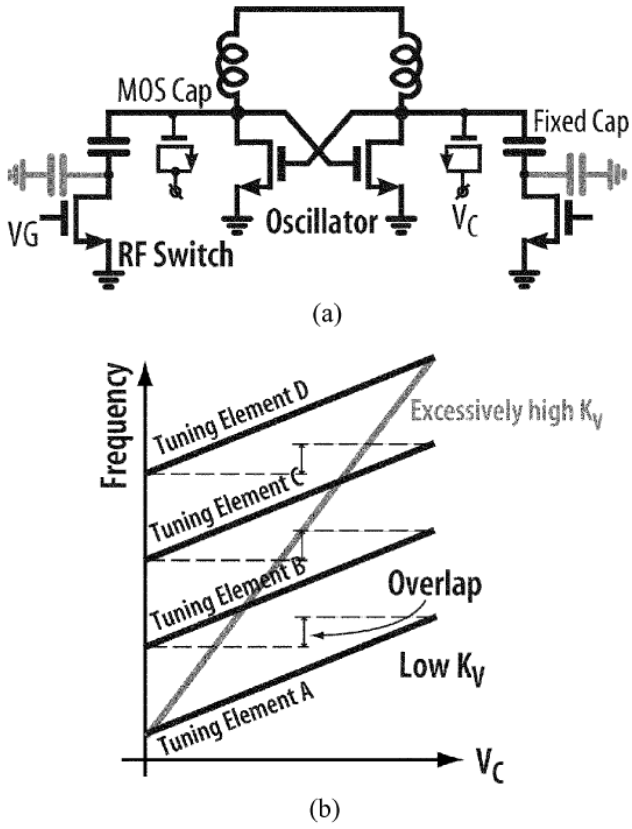

Figure 2.3: a) VCO with band switching. b) Resulting linear tuning ranges.

By 1997 the RF CMOS components thus described eventually made their way into fully functional, single-chip transceivers [3, 4, 9, 10, 11]. In just a few more years CMOS would be found in commercial cordless telephones and in systems that used newly created

wireless standards such as 802.11 and Bluetooth. The economics of wireless local area network (WLAN) systems were entirely different than that of bipolar cellular systems. WLAN electronics were not subsidized by service providers. Rather, the cost of WLAN systems is what determined their street price. This provided much incentive to use CMOS technology, where it reigns supreme in terms of cost and level of integration. With the attention it had been given by university researchers in the 1990s, by the year 2001 RF CMOS had finally reached a level of performance sufficient for widespread deployment in commercial WLAN systems.

In 2001 the first wave of commercial 2.4 GHz CMOS Bluetooth transceivers was announced [12]. This would be followed by the release of new 802.11 systems, which were manufactured almost exclusively in CMOS. The common 0.18 μm CMOS process has proven itself able to produce quality 5 GHz radios. Thanks in large part to the innovation and persistent efforts of university researchers, today CMOS has a dominant presence in the wireless industry.

2.2 Wireless Technologies

Several popular wireless standards have emerged in the past decade or so including 802.11, Bluetooth, and Zigbee. These three standards can all be used in low IF architectures where image-reject filters are necessary. Each standard has specific applications, and as such, each standard has a different set of technical specifications. One of the most important specifications in a WLAN system is the physical layer (PHY). The PHY consists of the basic hardware transmission technologies of a network. Among other things, the modulation scheme and broadcast frequencies are specified in the PHY.

802.11, also known as WiFi, is a family of wireless communication protocols that is popular in many modern WLAN devices. The most popular PHY extensions in the 802.11 family are 802.11a, 802.11b, 802.11g, and 802.11n. The 802.11a standard operates in the 5 GHz band and offers 12 non-overlapping channels. It uses a modulation technique known as orthogonal frequency-division multiplexing (OFDM) and offers data rates of 6-54 Mbps. 802.11b operates in the 2.4 GHz ISM band and has only 3 non-overlapping channels. It uses the complementary code keying (CCK) modulation scheme and supports data rates of 5.5

and 11 Mbps. 802.11g also operates in the 2.4 GHz band and is backward compatible with 802.11b. It uses OFDM to provide high data rates of 6-54 Mbps.

The recently approved 802.11n protocol operates in both the 2.4 and 5 GHz bands. It boasts drastically improved data rates and operational range through higher order constellations, increased bandwidth, and multiple in, multiple out (MIMO) techniques. 802.11n is fully backward compatible with the previously mentioned 802.11 standards.

Bluetooth is a short-range, low-bandwidth wireless protocol operating in the 2.4 GHz band. It was created to eliminate wires to enable wireless personal area networks (WPAN). Bluetooth uses a technique known as frequency-hopping spread spectrum (FHSS) which distributes data in small chunks on up to 79 bands of 1 MHz each. Common applications include wireless mobile phone headsets, PC input/output devices, and short range data transmission.

Zigbee is another WPAN standard, designed to be simpler and less expensive than Bluetooth. It operates in both the 2.4 GHz and 900 MHz bands which offer data rates of 250 kbps and 40 kbps, respectively. It is intended for applications that require long battery life, low bandwidth, and secure networking. Zigbee is often used in wireless monitoring and control systems.

2.3 Conclusion

RF electronics were initially dominated by the vacuum tube, followed by the bipolar transistor, and finally today, the complimentary MOS transistor. CMOS is now found is a wide variety of radios employing wireless technologies such as 802.11, Bluetooth, and Zigbee. All of these wireless standards can be used in low IF receivers requiring image-reject filters where the circuit of this work would find application.

Chapter 3

Receiver Architectures

There are three main types of RF receiver architectures: superheterodyne, low IF, and direct conversion (also known as zero IF or homodyne). Each has inherent strengths and weaknesses, and each must include unique circuitry to address those weaknesses. The superheterodyne architecture is the oldest of the three. It is also the most widespread architecture in use today if all radio types are included (instead of just WLAN radios). The low IF receiver was very popular for many years, but today its WLAN use is limited to mostly narrowband systems. The direct conversion receiver was not widely used for many years because of limited performance, but recent advances have made it a popular choice for wideband systems. Except where noted, all of the information and figures in this chapter were sourced from [13].

3.1 Superheterodyne

Figure 3.1 shows the general form of the superheterodyne architecture with frequency planning applied to the 802.11a standard. The RF signal is first passed through an off-chip band-pass ceramic or surface acoustic wave (SAW) filter. The signal is amplified by an LNA after which it passes through an image-reject SAW filter. The signal is then mixed down to a fixed IF. Since the IF is fixed, the local oscillator (LO) frequency is adjusted such that the difference between the LO and RF channel center frequency is always equal to the IF. The LO adjustment might be performed manually in the case of FM radio or automatically by a digitally controlled frequency synthesizer. After the mixing stage the signal passes through a channel-select SAW filter. The level of the signal is then adjusted through a programmable gain amplifier (PGA), separated into I and Q components, and mixed down to baseband

through a set of quadrature mixers. Additional filtering and level adjusting then take place, after which the signal is passed to an analog-to-digital converter (ADC).

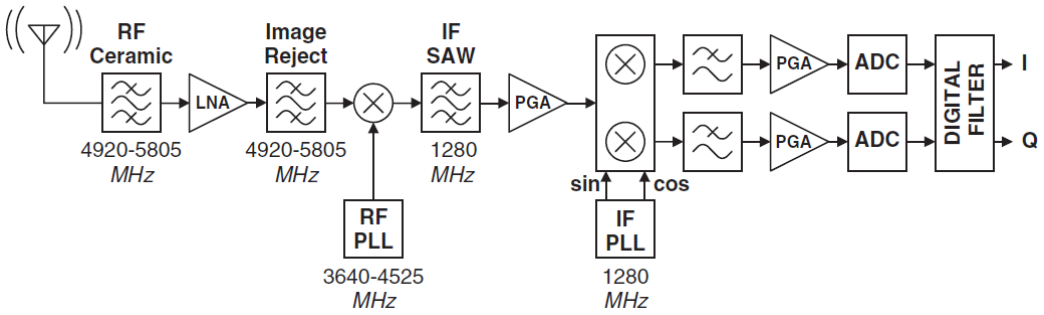

Figure 3.1: Superheterodyne receiver architecture.

The band-select filter that precedes the LNA serves to prevent saturation and desensitization of the LNA. Since the antenna will pick up a broad range of signals, the large voltage swing of the received RF signal may cause the LNA to saturate. The band-select filter prevents this by filtering out-of-band noise. The band-select filter may not be necessary, however, if the LNA has a tuned input and load impedance. In such a case, the image-reject filter also performs the function of band selection. All the RF components that precede the channel-select filter must have a high degree of linearity since they will contain all the channels over the entire band and will thus have a large voltage swing.

The IF in a superheterodyne receiver must be carefully chosen as the choice of IF directly impacts the filtering requirements of the system. There are two main system blocks that impact the choice of IF: the image-reject filter and the channel-select filter. The image frequency is a problem that is inherent in the superheterodyne and low IF architectures. It will be defined and discussed in detail in Ch. 4. For now the image will be concisely defined as a noise signal that must be suppressed in order to recover the desired signal. Image rejection is accomplished at the front end of the receiver by passing the desired RF band and rejecting all other frequencies. An off-chip high Q filter is required since image rejection takes place at RF where the ratio of the lowest channel frequency to the highest

image frequency is quite small. This creates the need for a filter with a very sharp roll-off in order to sufficiently reject the image without attenuating the desired RF band.

To ensure that all possible image frequencies are located outside the band of desired channel frequencies, the IF should be greater than the difference between the highest and lowest desired channels frequencies. In the case of 802.11a, the IF should be greater than 5805 MHz - 4920 MHz = 885 MHz. If this requirement is not met, the image signal will fall within the desired channel bandwidth and will not be rejected by the front-end filter.

Since the Q of the channel-select filter is proportional to the IF ($Q = \frac{f_{IF}}{channel\,bandwidth}$), the high IF required in super heterodyne receivers necessitates another off-chip high Q filter for channel selection. Transmission line effects must be considered when going off-chip, which complicates the design process. The off-chip filters in the superheterodyne receiver increase the size, complexity, and cost of the system and are the primary drawbacks of this architecture.

The image frequency is somewhat difficult to design for since it is not regulated by the same standard as the desired band. The IF should be selected such that the power level of the corresponding image band is kept at a minimum. This relaxes the IRR requirement of the image-reject filter. For a given IF, the corresponding band of image frequencies must be analyzed in each area of the world in which the product will be used since the same image band will contain different amounts of energy depending on location.

Once a minimum value of IF has been determined, there is still much freedom in choosing the IF. The higher the IF, the more relaxed the image-reject filter requirement will be, since a high IF will push the image frequency farther away from the desired RF signal ($f_{RF} - f_{IM} = 2_{fIF}$). But as the IF increases, so does the required filtering performance of the channel-select filter. A balance between the requirements of the image-reject filter and the channel-select filter is one of the most important criteria in choosing the IF.

The superheterodyne receiver does not suffer much from DC offset and flicker noise because of the large gain that is present in the receiver prior to baseband conversion. A DC offset is created in a receiver when the LO signal couples back to one of the pre-mixer stages, eventually making its way back to the mixer where it mixes with itself. In a superheterodyne receiver, the RF LO signal is outside of the band of interest and is easily rejected through

high-pass filtering in the form of AC coupling between stages. This prevents the stray LO signal from reaching the mixer input. One final advantage to this architecture is that the quadrature conversion takes place at the IF stage where quadrature matching is more easily achieved. Other architectures require generating quadrature signals at the RF stage, which is more difficult.

In summary, the superheterodyne architecture has the following strengths and weaknesses:

Pros

- It is the most mature and well-understood architecture and therefore has relatively low-risk and fast time-to-market compared to other architectures
- Flexible IF planning
- Minimal DC offset and flicker noise problems
- Good quadrature matching
- Newer architectures have reasonably low power-consumption

Cons

- Expensive and large compared to other architectures due to off-chip filtering requirements
- Transmission line effects must be considered due to need to go off-chip
- Image frequency can be problematic since it is not regulated by the same standard as the desired channel
- Finding a suitable IF for a broadband input can be difficult
- Difficult to design a multi-mode system using the superheterodyne architecture since programmable channel bandwidth and selectivity are not possible with SAWs

3.2 Low IF

The low IF architecture is very similar to the superheterodyne architecture, but as the name suggests, it uses a low IF that is close to baseband. This approach overcomes some of the disadvantages of other receiver architectures, but creates other problems unique to this architecture. The low IF has characteristics of both the superheterodyne and zero IF architectures and attempts to combine the strengths and minimize the weaknesses of both.

There are many choices in determining the exact structure of a low IF receiver. Two forms will be reviewed and analyzed. Figure 3.2 shows one form of the low IF architecture with frequency planning applied to the 802.11a standard. The RF signal is first band-pass filtered and differentially applied to an LNA by a balun. The tunable RF mixers perform quadrature conversion and translate the desired signal to the IF. The signal is then low-pass filtered, level-adjusted by the PGAs, and passed to the ADC. Since the image is still present at this point, the ADC must have a large dynamic range to accommodate the potentially large image signal. Once in the digital domain, image rejection and final conversion to baseband take place.

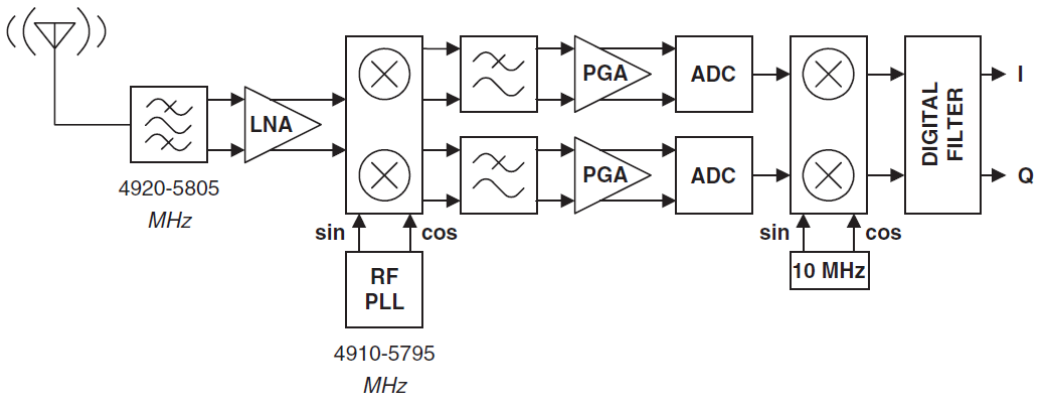

Figure 3.2: Low IF architecture.

Figure 3.3 shows a second low IF form. In this scheme the image rejection takes place in the analog domain using complex filters (discussed more fully in Section 4.3.3). While this adds complexity to the analog filters, it also reduces the dynamic range requirement of

the ADC since the image is no longer present at that point. One approach is not inherently better than the other, but the system designer should be aware that this trade-off is available.

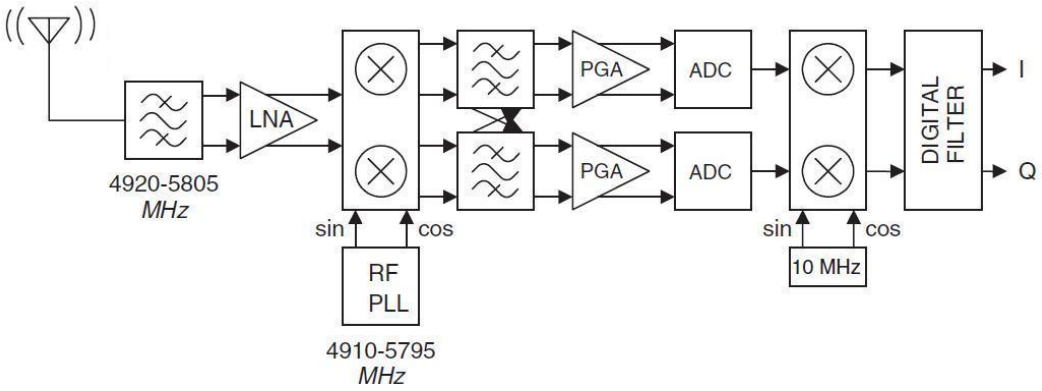

Figure 3.3: Low IF architecture with complex filters.

Using a low IF places the image frequency within the band of desired frequencies. This creates the need to perform image rejection in a manner different from that of the superheterodyne receiver, but it eliminates the need for a high Q off-chip image-reject filter at the front end of the receiver. Also, since channel selection takes place at the RF stage, the channel-select filter can be implemented on-chip. Elimination of the off-chip filters makes the low IF receiver highly integrable. This reduces the cost, size, and complexity of the system.

Since the image frequency falls within the band of desired frequencies, it is bound by the same regulatory standard as the desired channel. This guarantees that the power level of the image frequency is below some maximum value. This simplifies the planning of the image-reject filter and helps guarantee that after image rejection has taken place, the worst-case power level of the image is always below an acceptable value regardless of what external interference is present.

The problem of DC offset is avoided by either performing baseband conversion in the digital domain or by filtering. If baseband conversion takes place in the analog domain, the desired channel will be located far enough away from DC that any offset can be eliminated

through high-pass filtering in the form of AC coupling. This problem is not as easily solved in the direct conversion architecture and will be discussed further in the next section.

When selecting an IF, the designer must ensure that the IF is greater than half the bandwidth of the channel in order to avoid aliasing of the signal at baseband. Flicker noise can sometimes be problematic if the IF is particularly low. On the other hand, a wideband signal requires a higher IF, which increases power consumption. This is the primary disadvantage to using the low IF receiver in wideband applications.

In summary, the low IF architecture has the following strengths and weaknesses:

Pros

- Eliminates off-chip filtering components
- High level of integration
- The image frequency is well-defined because it is bound by the same regulatory standard as the desired channel
- DC offset is minimal and can be easily eliminated

Cons

- Requires high performance ADC or high performance complex filters, depending on where image rejection takes places
- Requires generation of RF quadrature signals, which is more difficult than at lower frequencies
- Flicker noise may be a problem at very low IF frequencies
- Wideband signals require a higher IF which increases power consumption

3.3 Direct Conversion

The direct conversion, or zero IF, receiver is shown in Fig. 3.4. The direct conversion receiver is nearly identical to the low IF receiver with a few important modifications. First,

the RF local oscillators are tuned to the center frequency of the desired channel. This mixes the channel directly down to baseband, eliminating the IF stage. As a consequence, the image band is the desired channel itself, so the problem of image frequency is avoided with this architecture. Second, since there is no IF stage, the IF mixers that are present in the low IF architecture are eliminated in this scheme.

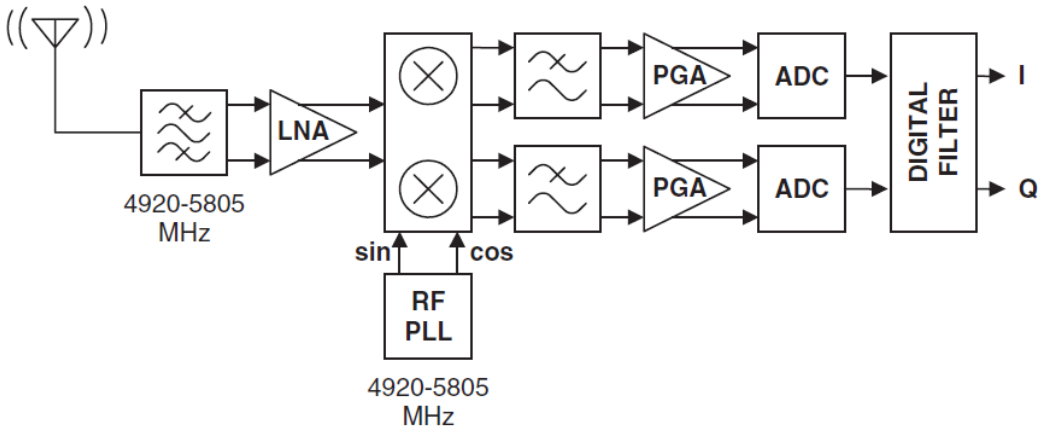

Figure 3.4: Direct conversion architecture.

In the past the direct conversion architecture has been plagued with problems that made it unpopular. However in recent years innovation has overcome many of these problems, and direct conversion is now a very popular choice for receiver architectures. In fact, the majority of WLAN transceivers produced today use a direct conversion receiver. Among the problems that must be overcome are LO leakage, DC offset, and flicker noise.

As explained in Sec.3.1, the problem of LO leakage is easily solved in the super-heterodyne receiver through high-pass filtering. This approach doesn't work in the direct conversion receiver because the LO signal is at the same frequency as the RF signal. The problem must therefore be dealt with in a different manner. LO leakage can be caused by insufficient reverse isolation of the RF components, asymmetric layout, coupling of the VCO signal to the LNA input or mixer inputs, and LO re-radiation. LO re-radiation occurs when the local oscillator signal couples back to the receiver and radiates through the antenna. This radiated signal can then be picked up by the antenna and fed to the RF mixer. In all

cases this results in self-mixing, which produces a DC offset. One method of preventing LO re-radiation is to run the VCO at a harmonic or sub-harmonic of the incoming RF frequency. The required LO frequency can then be generated after the VCO stage.

Since there is little gain present in a direct conversion receiver prior to the baseband stage, any DC offset introduced by self-mixing is usually heavily amplified by the PGA at baseband. A large DC offset can cause total desensitization of the PGA. A DC offset is not easily filtered because it lies exactly in the middle of the desired channel in a direct conversion receiver. High-pass filtering would remove part of the desired signal along with the offset. To overcome this problem, the zero-order carrier is eliminated in the WLAN OFDM standard. The DC offset can then be removed through cautious high-pass filtering.

In summary, the direct conversion architecture has the following strengths and weaknesses:

Pros

- Eliminates off-chip filtering components
- Highest level of integration among the three receiver types
- Lowest cost
- Image problem is avoided
- Newer designs are low power and high performance

Cons

- Requires generation of RF quadrature signals, which is more difficult than at lower frequencies
- LO re-radiation can be problematic
- DC offset problem
- Susceptible to flicker noise

3.4 Conclusion

The strengths and weaknesses of each receiver architecture determine their suitability for a new wireless design. The direct conversion architecture is currently the most popular choice due to its low cost, high level of integration, and high performance. The low IF architecture is also low cost and highly integrable and is a very popular choice for narrowband wireless applications such as Bluetooth and Zigbee. The superheterodyne architecture is less popular for WLAN use due to its higher cost and lower level of integration [14].

Chapter 4

Image Rejection

Frequency translation in a wireless transceiver is accomplished by means of a device called a mixer. A mixer is a device that approximates the multiplication operation. When two sinusoids are multiplied (or "mixed") together, two new frequencies are produced that are the sum and difference frequencies of the two inputs. When mixing down in a receiver, only the difference frequency is desirable and the sum frequency is filtered out. For a given RF frequency, there is another frequency equidistant from the LO that will mix down to the same frequency as the RF signal. The result is two signals that are superimposed on top of one another: the RF signal and an undesired signal. The undesired signal is known as the image.

The image problem is best explained by example. Suppose an RF signal at 5180 MHz is mixed with an LO running at 5170 MHz. The mixer will produce sum and difference frequencies of 10 MHz and 10.35 GHz. The higher frequency signal is undesirable and is easily eliminated through high-pass filtering. Whatever content is present at 5160 MHz will also mix with the LO signal to produce a difference frequency of 10 MHz. Thus, two different frequencies equidistant from the LO will both translate down to 10 MHz, superimposed on top of each other.

Anytime an IF frequency is produced in a wireless receiver, an image frequency is created. The image must be sufficiently suppressed if the desired signal is to be recovered. Superheterodyne and low IF receivers must both deal with the image problem, although their different architectures require them to suppress the image in different ways. The image problem is largely avoided in a direct conversion architecture since the image signal is the desired signal itself. However if the LO is not tuned exactly to the incoming RF signal, an image signal will result which may need to be suppressed.

Figures 4.1, 4.2, and 4.5 from this section were sourced from [14].

4.1 Image Rejection Methods

The following sections discuss the popular analog methods of image rejection in wireless receivers.

4.2 Bandpass Filter

A bandpass filter is often used at the front end of a superheterodyne receiver to pass the band of interest to the LNA and suppress all other frequencies, including the image band. Superheterodyne receivers typically have one or two stages of image rejection (see Fig. 3.1). This method only works if the image band does not overlap with any of the channels of interest. Otherwise, some of the desired channels would be filtered at the front end of the receiver along with the image, making them unrecoverable at later stages. The IF should be greater than the difference between the highest and lowest desired channels frequencies to ensure that the image band does not overlap with any of the desired RF channels.

The farther away the image band is from the desired band, the more relaxed the filtering requirement will be. A high IF will increase the distance between the image band and the desired channel since $f_{RF} - f_{IM} = 2f_{IF}$. Since the image band is not regulated by the same standard as the desired channel, the image signal may be at a much higher power level than the desired channel. Thus high Q filters are needed to sufficiently suppress the image.

4.3 Hartley Method

For a low IF receiver the image band will overlap with the desired band at least to some degree. Because of this, a bandpass filter cannot be used for image rejection and other methods must be employed. The Hartley method is one such method that can be used for image rejection in a low IF receiver. One might naturally think that after the RF and image signals have been translated down to the same frequency then separation of these two signals would be impossible. The Hartley method accomplishes exactly such a separation

and cancellation through clever exploitation of trigonometric identities. Figure 4.1 shows the general form of the Hartley method of image rejection.

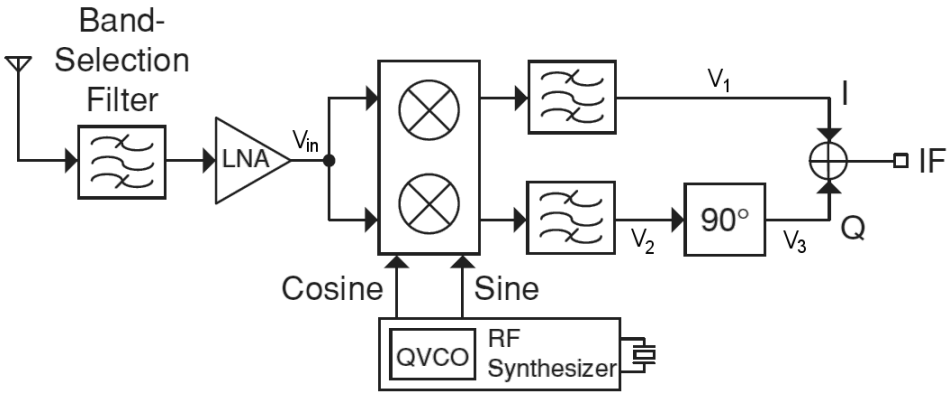

Figure 4.1: Hartley method of image rejection.

If both the RF and image signal are present at the input of the mixers such that

$$V_{in} = \cos\,\omega_{RF}t + \cos\,\omega_{IM}t, \tag{4.1}$$

and assuming $\omega_{LO} > \omega_{RF}$, then after low-pass filtering,

$$V_1 = \frac{1}{2}\cos(\omega_{LO} - \omega_{RF})t + \frac{1}{2}\cos(\omega_{IM} - \omega_{LO})t \tag{4.2}$$

and

$$V_2 = -\frac{1}{2}\sin(\omega_{RF} - \omega_{LO})t - \frac{1}{2}\sin(\omega_{IM} - \omega_{LO})t. \tag{4.3}$$

Since $\omega_{RF} - \omega_{LO}$ is negative and $\sin(-x) = -\sin(x)$, V_2 becomes

$$V_2 = \frac{1}{2}\sin(\omega_{LO} - \omega_{RF})t - \frac{1}{2}\sin(\omega_{IM} - \omega_{LO})t. \tag{4.4}$$

The quadrature path undergoes an additional 90° phase shift which produces

$$V_3 = \frac{1}{2}\cos(\omega_{LO} - \omega_{RF})t - \frac{1}{2}\cos(\omega_{IM} - \omega_{LO})t. \tag{4.5}$$

The output is then equal to

$$V_{out} = \cos(\omega_{LO} - \omega_{RF})t. \tag{4.6}$$

With perfect quadrature mixing, a precise 90° phase shift (also known as a quadrature phase shift), and a constant amplitude response, the image signal is exactly canceled out leaving the desired signal perfectly intact. In practice, such a circuit is not possible. There will always be some quadrature mismatch, and the phase shift network will always have some combination of phase and gain error.

There is in fact no network that can provide both a constant 90° phase shift and a constant amplitude response over an infinite range of frequencies [15]. However, there are several circuits that can approximate such a response over a limited range. The following three sections compare and contrast three methods of quadrature shifting for use in the Hartley method of image rejection.

4.3.1 RC-CR Filter

Figure 4.2 depicts the quadrature shift from Fig. 4.1 implemented using an RC-CR filter [15].

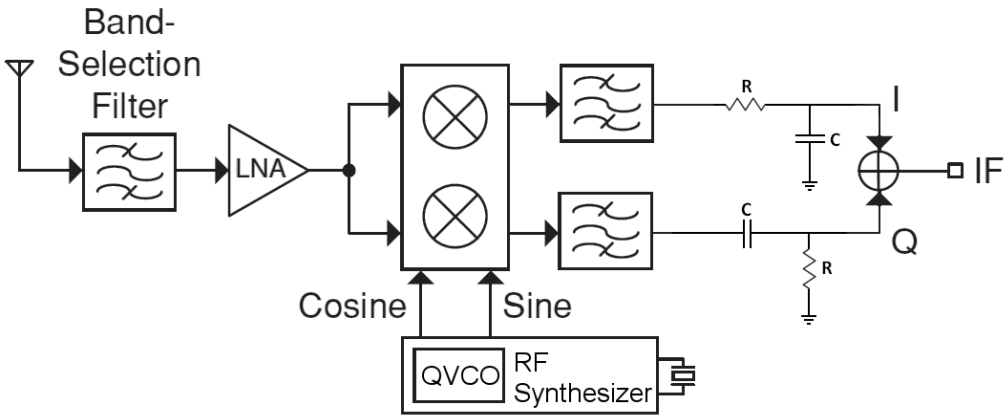

Figure 4.2: Hartley method of image rejection using an RC-CR filter.

The transfer functions and corresponding magnitude and phase responses at points I and Q are

$$I = \frac{1}{(1+sCR)} \Rightarrow \frac{1}{\sqrt{(1+(\omega CR)^2}} \ \angle - tan^{-1}(\omega CR) \tag{4.7}$$

and

$$Q = \frac{sCR}{(1+sCR)} \Rightarrow \frac{\omega CR}{\sqrt{(1+(\omega CR)^2}} \ \angle 90^\circ - tan^{-1}(\omega CR). \tag{4.8}$$

Although the phase shifts in the individual I and Q paths change as a function of frequency, the phase difference between the two branches remains constant at 90° over all frequencies. The gain, however, changes as a function of frequency and is only matched at the pole frequency

$$\omega = \frac{1}{RC}. \tag{4.9}$$

The gain error increases proportional to the deviation of the operating frequency from the pole frequency. When choosing values of R and C, the gain error can be minimized by setting the pole frequency in Eq. (4.9) equal to the IF. The RC-CR has poor wideband performance, but it is a popular method for generating quadrature signals over a narrow frequency band [15].

4.3.2 All-Pass Filter

Figure 4.3 shows the general form of an all-pass filter. The transfer function and corresponding magnitude and phase responses are

$$H(s) = \frac{(sCR-1)}{(sCR+1)} \Rightarrow 1 \ \angle 180^\circ - 2tan^{-1}(\omega CR). \tag{4.10}$$

The all-pass filter has a gain of 1 at all frequencies and a phase shift that is a function of frequency. The phase shift is 90° at the pole frequency (see Eq. (4.9)). When choosing values of R and C, the phase error can be minimized by setting the pole frequency equal to the IF.

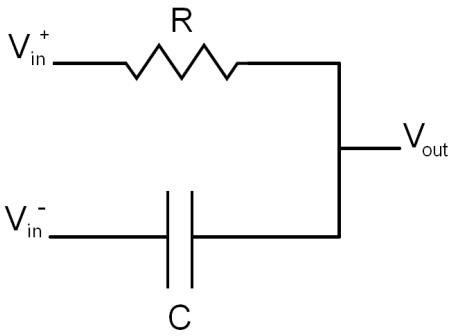

Figure 4.3: All-pass filter.

As shown in Fig. 4.3, the all-pass filter requires a differential input. Low IF receivers are much more susceptible to noise than superheterodyne receivers, so it is common to implement a balun at the front end and run the I and Q paths differentially. Thus, a differential signal is generally available in the IF stage of a low IF receiver where the all-pass filter would find application.

4.3.3 Polyphase Filter

Another very useful method of image rejection uses a polyphase filter to perform the quadrature phase shift. Figure 4.4 shows a two-stage polyphase filter. This filter has inputs and outputs at different phase relationships and is therefore known as a polyphase filter. It is part of a class of filters known as complex filters. A traditional filter's magnitude response is only a function of input frequency. A complex filter's magnitude response is a function of both input frequency and phase. Subsequently, a complex filter has at least two inputs which together provide the necessary frequency and phase information. In a typical two-input complex filter, the inputs would represent the real and imaginary components of a signal. In the case of an RF receiver, such a signal can be created by separating a signal into its I and Q components through quadrature down conversion. Image rejection can then take place using a polyphase filter.

In a polyphase filter each stage typically provides a gain error of under 0.2 dB over a 10% bandwidth [15]. The required number of stages is thus determined by the bandwidth requirement of the channel. When designing a polyphase filter, the geometric mean of the

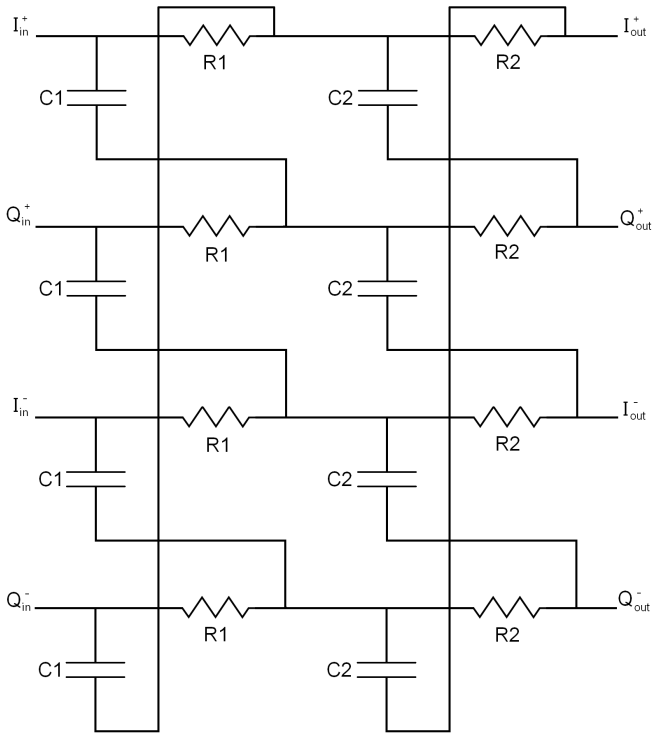

Figure 4.4: Two-stage polyphase filter.

RC pole values is chosen equal to the desired center frequency. So for a two-stage filter with a center frequency of 1 GHz, the RC poles might be selected to be 900 MHz and 1.1 GHz. It is common practice to choose a single capacitor value for the entire filter and vary the resistance across the stages to achieve the desired pole values [15]. The polyphase filter can provide good constant gain matching and quadrature precision. The disadvantages are high overall attenuation and noise, the need to add extra stages to accommodate large process variations in the RC product, and excessive layout space for wideband, multi-stage filters.

The transfer functions for one-stage and two-stage polyphase filters are

$$H(s) = \frac{1 + \omega RC}{1 + j\omega RC} \tag{4.11}$$

and

$$H(s) = \frac{(1 + \omega R_1 C_1)(1 + \omega R_2 C_2)}{1 - \omega^2 R_1 C_1 R_2 C_2 + j\omega(R_1 C_1 + R_2 C_2 + 2R_1 C_2)}. \tag{4.12}$$

The transfer functions become extremely complex for stage numbers greater than two, but they are available in research publications [16].

4.4 Weaver Method

The Weaver method of image cancellation operates similarly to the Hartley method, but uses an additional pair of mixers to eliminate the need for a quadrature phase shift. Figure 4.5 shows the general form of a Weaver image reject filter.

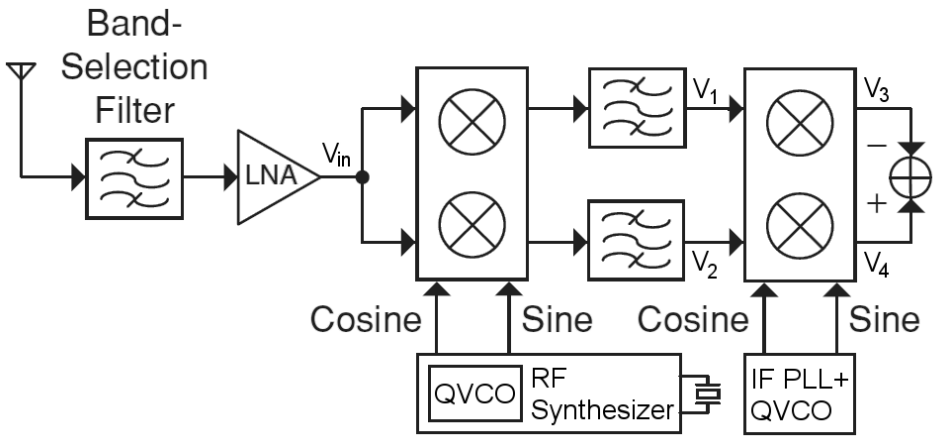

Figure 4.5: Weaver method of image rejection.

With an input of

$$V_{in} = \cos\,\omega_{RF}t + \cos\,\omega_{IM}t, \tag{4.13}$$

and assuming $\omega_{LO1} > \omega_{RF}$, then after low-pass filtering,

$$V_1 = \frac{1}{2}\cos(\omega_{LO1} - \omega_{RF})t + \frac{1}{2}\cos(\omega_{IM} - \omega_{LO1})t \tag{4.14}$$

and

$$V_2 = -\frac{1}{2}\sin(\omega_{RF} - \omega_{LO1})t - \frac{1}{2}\sin(\omega_{IM} - \omega_{LO1})t. \tag{4.15}$$

Since $\omega_{RF} - \omega_{LO1}$ is negative and $\sin(-x) = -\sin(x)$, V_2 becomes

$$V_2 = \frac{1}{2}\sin(\omega_{LO1} - \omega_{RF})t - \frac{1}{2}\sin(\omega_{IM} - \omega_{LO1})t. \tag{4.16}$$

At this point in the signal path the signals are identical to those in the Hartley method. V_1 and V_2 undergo additional quadrature mixing to obtain

$$V_3 = \frac{1}{4}\cos(\omega_{LO2} - \omega_{LO1} + \omega_{RF})t + \frac{1}{4}\cos(\omega_{LO2} - \omega_{LO1} + \omega_{IM})t \tag{4.17}$$

and

$$V_3 = \frac{1}{4}\cos(\omega_{LO2} - \omega_{LO1} + \omega_{RF})t - \frac{1}{4}\cos(\omega_{LO2} - \omega_{LO1} + \omega_{IM})t, \tag{4.18}$$

neglecting the sum frequencies. The output is then equal to

$$V_{out} = \frac{1}{2}\cos(\omega_{LO2} - \omega_{LO1} + \omega_{RF})t. \tag{4.19}$$

With perfect quadrature mixing and constant gain through the I and Q paths, the image signal is exactly canceled out. As with all image-reject methods, such precision is never possible and a finite IRR results.

4.5 Other Methods

Tunable notch filters may also be used for image rejection [17, 18, 19]. Such a filter would use a varactor to vary the resonant frequency of the tuned filter. The varactor control signal might be generated using a PLL that produces a voltage proportional to the image frequency. This type of filter would be suitable for use in both superheterodyne and low IF receivers.

All of the image-reject filters discussed so far use analog circuitry to perform the rejection. The image rejection can also take place in the digital domain using DSP methods. The trade-off is a higher performance requirement for the DAC. Since the image signal would be present at the DAC input when using DSP methods, the DAC must have a higher dynamic range to accommodate the image signal.

4.6 Conclusion

The image is a noise signal created through mixer down-conversion that is present in superheterodyne and low IF receivers. In a superheterodyne receiver the image is typically rejected using a high Q off-chip bandpass filter. The designer of a low IF receiver has many more options available. Common methods of image rejection are the Hartley method and the Weaver method. The Hartley method requires a filter that can produce a precise 90° phase shift while maintaining constant amplitude response. Practical phase shift filters can only approximate these requirements. For wideband systems a multi-stage polyphase filter is most frequently used. Image rejection filters using the Weaver method require highly matched mixers to produce good results. Tunable notch filters and DSP methods can also be used for image rejection.

Chapter 5

A Wideband Precision Quadrature Phase Shifter

As discussed in Ch. 4, the primary limitations on IRR using the Hartley method of image rejection are quadrature precision and constant amplitude response. Wideband quadrature precision and constant amplitude response can be achieved using multi-stage polyphase filters, but such filters can require copious amounts of layout space and have considerable attenuation. A wideband, precision quadrature phase shift circuit is proposed which uses an RC-CR filter in a feedback configuration in order to achieve constant amplitude response. Such a circuit can be used to perform image rejection using the Hartley method, which was discussed in Sec. 4.3.

5.1 System-Level Description

As discussed in Sec. 4.3.1, the basic RC-CR filter consists of parallel low-pass and high-pass filters with equal pole frequencies. A basic RC-CR filter is shown again in Fig. 5.1 for convenience.

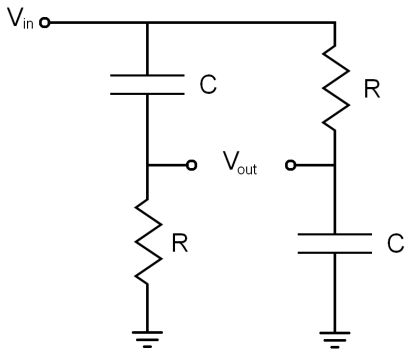

Figure 5.1: RC-CR filter.

The output is taken as the difference between the low-pass and high-pass filter outputs. The RC-CR filter has a phase shift equal to 90° at all frequencies and equal amplitude response at the pole frequency. Wideband constant amplitude response can thus be achieved if the value of R can be dynamically adjusted as a function of frequency, such that the pole frequency always equals the frequency of the input signal. Figure 5.2 demonstrates this from the frequency response plot of an RC-CR filter. At the pole frequency f_1, both the low-pass and high-pass branches of the filter have equal magnitudes. When the input frequency changes to f_2, then the magnitudes of the two filter branches are no longer equal if the values of R and C are fixed. But if R is dynamically changed to move the pole frequency to f_2, the filter will then have an equal amplitude response at this frequency as well.

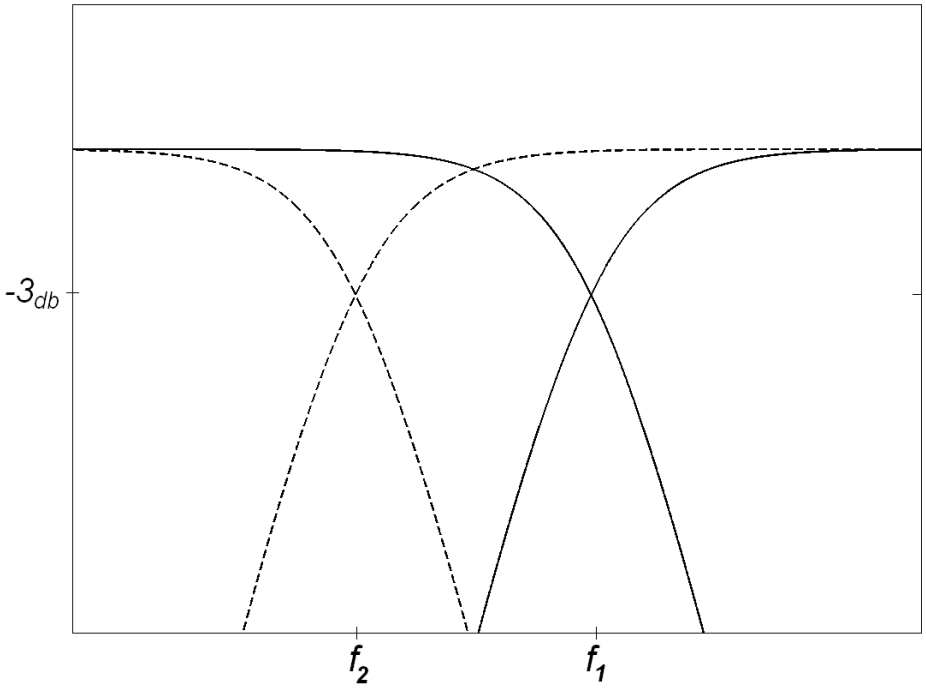

Figure 5.2: Constant amplitude response by shifting the pole frequency.

Directly monitoring the input frequency requires a circuit such as a PLL that can produce a control signal proportional to input frequency. However, a much simpler approach is to indirectly monitor the input frequency by comparing the amplitudes of the RC-CR

filter outputs. The difference in peak voltages between the RC and CR branches produces an error voltage that uniquely represents some deviation from the pole location. Figure 5.3 demonstrates this idea from the RC-CR frequency response plot.

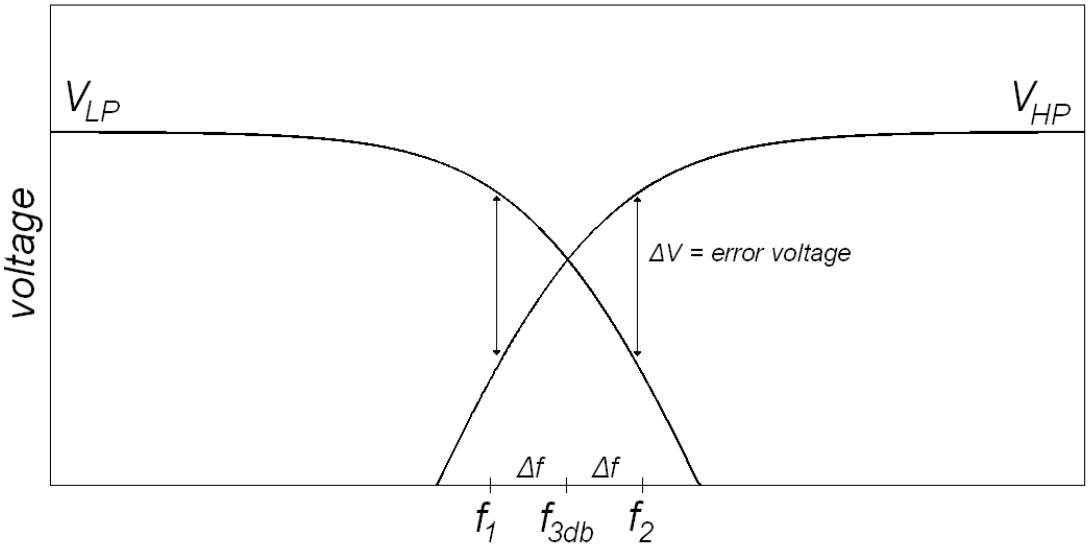

Figure 5.3: Detecting frequency deviation through amplitude error.

The error signal is defined as

$$V_{err} = V_{HP}(f) - V_{LP}(f) \tag{5.1}$$

where $V_{HP}(f)$ and $V_{LP}(f)$ are respectively the high-pass and low-pass filter peak output voltages for some nominal input voltage. An error signal of $V_{err} = V_{HP}(f_1) - V_{LP}(f_1)$ uniquely corresponds to an input frequency of $f_1 = f_{3db} - \Delta f$. When the input shifts to $f_2 = f_{3db} + \Delta f$, then $V_{err} = V_{HP}(f_2) - V_{LP}(f_2)$, which is equal in magnitude but opposite in sign compared to the previous error signal. The error signal is thus proportional to the input signal's deviation from the pole frequency. Such a signal can be created by taking the difference between the peak values of the RC-CR outputs. This can be practically implemented using two peak detectors and a differential amplifier.

A block diagram of the proposed quadrature phase shifter is shown in Fig. 5.4. The system consists of three stages: an RC-CR filter (with variable R) and a feedback loop consisting of two peak detectors and a differential amplifier. The amplified error signal generated from the feedback loop is connected to the control ports of a pair of variable resistors. This signal will drive the two resistances up or down until the pole frequency is equal to the frequency of the input signal. At this point the RC-CR outputs have equal amplitude response.

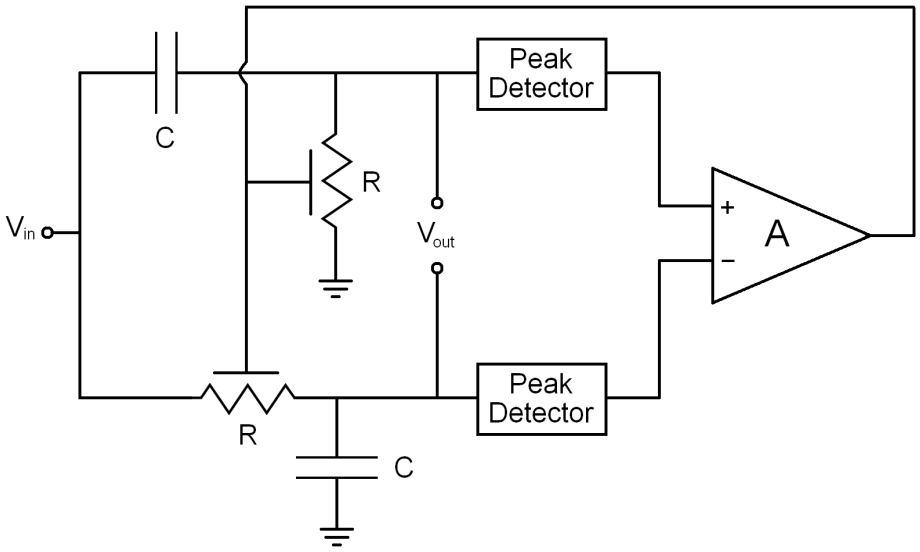

Figure 5.4: Block diagram of RC-CR filter with constant amplitude response.

5.2 Mathematical Analysis

The following two sections mathematically analyze the gain error, bandwidth, and mismatch of the system in Fig. 5.4 as a function of system parameters.

5.2.1 Gain Error

As shown in Fig. 5.4, the error signal previously defined in Eq. (5.1) is amplified by gain A. The resulting control voltage is thus defined as

$$A \cdot (V_{HP} - V_{LP}) = V_{CTRL}. \tag{5.2}$$

The resistance of the voltage-controlled resistors (VCR) is defined as

$$R = \frac{R_o}{V_{CTRL}} \tag{5.3}$$

where R_o is a constant measured in ohm-volts. The resistance is defined in this way because it models how the VCRs will be practically implemented in CMOS. Next, the gain error, G, is defined as

$$G = 1 - \frac{V_{LP}}{V_{HP}} \tag{5.4}$$

where V_{LP} and V_{HP} are the peak voltages of the filter outputs. When the filter outputs are equal, the gain error is zero. V_{LP} and V_{HP} are equal to

$$V_{LP} = \frac{1}{\sqrt{1 + (\omega CR)^2}} \cdot V_{in} \tag{5.5}$$

and

$$V_{HP} = \frac{\omega CR}{\sqrt{1 + (\omega CR)^2}} \cdot V_{in} \tag{5.6}$$

where V_{in} is the magnitude of the input signal. Substituting Eqs. (5.5) and (5.6) into Eq. (5.2) yields

$$A \cdot V_{in} \cdot \frac{\omega CR - 1}{\sqrt{1 + (\omega CR)^2}} = V_{CTRL}. \tag{5.7}$$

Equations (5.3), (5.4), and (5.7) will now be combined to form a mathematical description of the system. First, Eq. (5.3) is solved for V_{CTRL} and substituted into Eq. (5.7) to give

$$A \cdot V_{in} \cdot \frac{\omega CR - 1}{\sqrt{1 + (\omega CR)^2}} = \frac{R_o}{R}. \tag{5.8}$$

Next, Eqs. (5.5) and (5.6) are substituted into Eq. (5.4) and solved for R to obtain

$$R = \frac{1}{\omega C(1-G)}. \tag{5.9}$$

Equation (5.9) is now substituted into Eq. (5.8) which gives

$$A \cdot V_{in} \cdot \frac{\frac{1}{1-G} - 1}{\sqrt{1 + \frac{1}{(1-G)^2}}} = R_o \omega C(1-G). \tag{5.10}$$

After rearranging terms, Eq. (5.10) becomes

$$A = \frac{R_o \omega C(1-G)^2 \sqrt{1 + \frac{1}{(1-G)^2}}}{G\, V_{in}}. \tag{5.11}$$

Equation (5.11) defines the amplifier gain as a function of gain error. This equation can be used to calculate the necessary amplifier gain to achieve a desired gain error for a given set of parameters. Taking the limit of Eq. (5.11) as the gain error goes to zero,

$$\lim_{G \to 0} A = \infty. \tag{5.12}$$

This shows that the amplifier gain is one of the fundamental performance limitations for this system. Assuming $G \ll 1$ and solving for G, Eq. (5.11) becomes

$$G \approx \frac{R_o \omega C \sqrt{2}}{A\, V_{in}}. \tag{5.13}$$

Equation (5.13) shows that the gain error is proportional to C and inversely proportional to V_{in}, which would suggest using small capacitors and a large input signal. However, the following section on bandwidth shows that there is a trade-off involved in selecting the size of the RC-CR filter capacitors. Additionally, in the CMOS implementation performance is actually degraded with a large input signal due to non-idealities in the VCRs, as explained in Sec. 5.3.1.

5.2.2 Bandwidth

This section describes the bandwidth over which constant amplitude response can be achieved as a function of system parameters. The bandwidth is defined as

$$\Delta\omega = \omega_{max} - \omega_{min} \tag{5.14}$$

where ω_{min} and ω_{max} are respectively the minimum and maximum operating frequencies of the system. Using the pole frequency equation, the maximum and minimum values of R that are required for a given bandwidth are

$$R_{max} = \frac{1}{\omega_{min}C} \tag{5.15}$$

and

$$R_{min} = \frac{1}{\omega_{max}C}. \tag{5.16}$$

The range of R is therefore defined as

$$\Delta R = R_{max} - R_{min} = \frac{\Delta\omega}{C(\omega_{max}\omega_{min})}. \tag{5.17}$$

Using Eq. (5.3), the control voltage range is similarly defined as

$$\Delta V_{CTRL} = V_{CTRL-max} - V_{CTRL-min} = R_o\frac{\Delta R}{(R_{max}R_{min})}. \tag{5.18}$$

Substituting Eq. (5.17) into Eq. (5.18) gives

$$\Delta V_{CTRL} = \frac{R_o}{C}\frac{\Delta\omega}{R_{max}R_{min}\omega_{max}\omega_{min}}. \tag{5.19}$$

Equation (5.19) shows that the bandwidth of the system is limited by the available supply voltage (or more precisely, the output swing of the differential amplifier). The necessary voltage range can be reduced by using large C, however Eq. (5.13) shows that the gain error increases as C increases. This trade-off will be discussed more fully in Sec. 5.3.1.

5.2.3 Mismatch

The preceding sections have assumed perfectly matched resistors and capacitors in the RC-CR filter. Unfortunately, perfect matching is never possible, so this section analyzes the effect of mismatch on system performance. First, Eqs. (5.5) and (5.6) are redefined as

$$V_{LP} = \frac{1}{\sqrt{1 + (\omega C_{LP} R_{LP})^2}} \cdot V_{in} \tag{5.20}$$

and

$$V_{HP} = \frac{\omega C_{HP} R_{HP}}{\sqrt{1 + (\omega C_{HP} R_{HP})^2}} \cdot V_{in} \tag{5.21}$$

where C_{LP} and R_{LP} are the low-pass filter components, and C_{HP} and R_{HP} are the high-pass filter components. Since there is a point of intersection in Eqs. (5.20) and (5.21), the feedback network of the system shown in Fig. 5.4 will still drive the system to constant amplitude response when mismatch is present (this is explicitly proven in Appendix A). However, the frequency where the amplitudes of the filter outputs are equal no longer occurs at the pole frequency. This introduces a phase error in the output. The frequency where constant amplitude response occurs can be expressed by setting Eqs. (5.20) and (5.21) equal to each other and solving for ω. Solving for this frequency gives

$$\omega = \frac{1}{\sqrt{R_{LP} R_{HP} C_{LP} C_{HP}}}. \tag{5.22}$$

The validity of this equation can be verified by noting that if $R_{LP} = R_{HP}$ and $C_{LP} = C_{HP}$, then Eq. (5.22) reduces to the familiar pole equation.

The phase shifts corresponding to Eqs. (5.20) and (5.21) were defined previously (see Eqs. (4.7) and (4.8)) but are repeated here for convenience

$$\theta_{LP} = -tan^{-1}(\omega C_{LP} R_{LP}), \tag{5.23}$$

$$\theta_{HP} = 90^\circ - tan^{-1}(\omega C_{HP} R_{HP}). \tag{5.24}$$

The phase error, $\Delta\theta$, is defined as

$$\Delta\theta = \theta_{HP} - \theta_{LP} - 90^\circ = -tan^{-1}(\omega C_{HP} R_{HP}) + tan^{-1}(\omega C_{LP} R_{LP}) \tag{5.25}$$

which gives the deviation from 90°. Equation (5.22) is now substituted into Eq. (5.25) to give

$$\Delta\theta = -tan^{-1}\frac{R_{HP}C_{HP}}{\sqrt{R_{LP}R_{HP}C_{LP}C_{HP}}} + tan^{-1}\frac{R_{LP}C_{LP}}{\sqrt{R_{LP}R_{HP}C_{LP}C_{HP}}} \tag{5.26}$$

which now describes the phase error as a function of the mismatched resistor and capacitor pairs.

To facilitate the analysis of Eq. (5.26), the following two relationships are now defined,

$$R_{HP} = m_R R_{LP} \tag{5.27}$$

and

$$C_{HP} = m_C C_{LP}, \tag{5.28}$$

where m_R and m_C are the mismatch parameters that define the relative mismatch between the resistor and capacitor pairs. Perfect matching occurs only when $m_R = m_C = 1$. Any deviation from this value in either parameter signifies a mismatch. Substituting Eqs. (5.27) and (5.28) into Eq. (5.26) gives

$$\Delta\theta = -tan^{-1}\frac{m_R m_C}{\sqrt{m_R m_C}} + tan^{-1}\frac{1}{\sqrt{m_R m_C}} \tag{5.29}$$

which describes the phase error as a function of the mismatch parameters. When $m_R = m_C = 1.005$, which means that the high-pass components are 0.5% larger than the low-pass components, the phase error is 0.29°. This would result in a best-case IRR of 52 dB, which is a good figure. With such a mismatch, the system could tolerate a gain error of 0.4% and still maintain an IRR above 50 dB. In practice, component matching of 0.1% can be achieved in most standard processes. The corresponding phase error of 0.05% is so small that the gain error would likely be the limiting factor in the resulting IRR value. In conclusion,

although good matching is required in order to guarantee good performance, it is achievable in standard CMOS processes.

5.3 CMOS Implementation

This section describes how the components from Sec. 5.1 are implemented in 0.25 μm CMOS. The circuit operates with a 3 V power supply.

5.3.1 RC-CR Filter

The RC-CR filter shown in Fig. 5.5 is implemented using capacitors, resistors, and a pair of NMOS devices biased in the deep triode region. The NMOS devices act as voltage-controlled resistors with the transistor gates used as the control terminals.

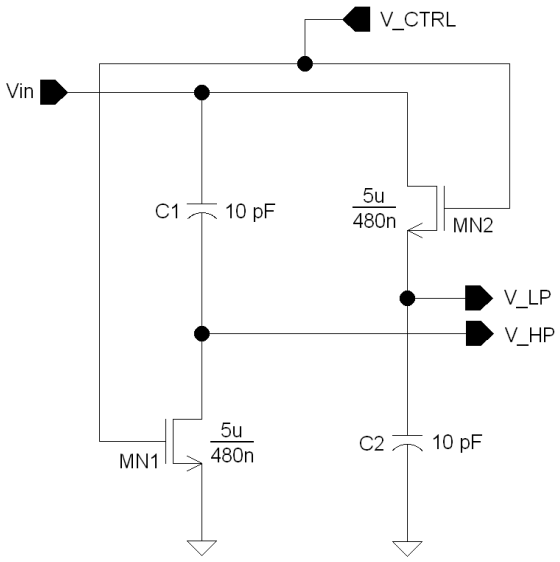

Figure 5.5: RC-CR filter schematic.

Equation (5.30) shows the channel resistance as a function of NMOS and system parameters,

$$R_{on} = \frac{L}{\mu_n C_{ox} W[V_{CTRL} - (V_S + V_{TH})]} \tag{5.30}$$

where W is the transistor channel width, L is the channel length, μ_n is the carrier mobility, C_{ox} is the transistor gate capacitance per unit area, V_{TH} is the threshold voltage, V_{CTRL} is the control voltage applied to transistor gate, and V_S is the transistor source voltage. This equation shows that since V_S also acts as a control signal, this terminal should ideally be grounded. Unfortunately, MN2 in Fig. 5.5 cannot have its source grounded, which will cause the channel resistance of MN2 to be slightly different from that of MN1. As explained in the preceding section on mismatch, this introduces a phase error at the RC-CR output. The source voltage of MN2 must therefore be kept small in order to minimize the channel resistance mismatch of MN1 and MN2. This limits the input of this circuit to small voltage swings. This problem can be mitigated by keeping V_{CTRL} as large as possible, which reduces the dependence of the channel resistance on V_S.

Equation (5.30) is only accurate when $V_{DS} \ll 2(V_{GS} - V_{TH})$ [20], where the I-V relationship is approximately linear. Expressed in terms of system parameters, this requirement becomes

$$V_D \ll 2(V_{CTRL} - V_{TH}) - V_S. \tag{5.31}$$

Satisfying this requirement reinforces the need to keep V_{CTRL} as large as possible and V_S as small as possible. The inequality of (5.31) also introduces the need to keep V_D small, which once again limits the RC-CR input to small voltage swings.

Using the same approach from Sec. 5.2.1, an expression can be derived showing the relationship between amplifier gain and gain error,

$$A \approx \frac{[\omega LC(1-G)^2 + \mu_n C_{ox} W V_{th}(1-G)]\sqrt{1 + \frac{1}{(1-G)^2}}}{\mu_n C_{ox} W G\, V_{in}} \tag{5.32}$$

where the approximation has been made that the source voltage of MN2 is equal to zero. Assuming $G \ll 1$ and solving for G, Eq. (5.32) becomes

$$G \approx \frac{[\omega LC + \mu_n C_{ox} W V_{th}]\sqrt{2}}{\mu_n C_{ox} W A\, V_{in}}. \tag{5.33}$$

Equation (5.33) shows that for a given amplifier gain, the gain error can be minimized by choosing small L and C. But as discussed in the previous section, a small C requires a large ΔV_{CTRL} (Eq. (5.19)). Since it is desirable to keep all possible values of V_{CTRL} as large as possible, C is chosen so as to make $V_{CTRL-max}$ as large as possible and ΔV_{CTRL} as small as possible. $V_{CTRL-max}$ should not be allowed to reach V_{DD} at nominal process and temperature, however, since $V_{CTRL-max}$ will need to go to higher values over process and temperature. Using these constraints as a guideline, precise values of W and C were chosen through iterative simulations. Additionally, despite the inverse proportionality between G and V_{in}, a small input voltage must be used to minimize phase error, as previously explained.

5.3.2 Level Detector

The peak detectors from Fig. 5.4 are replaced with level detectors in the CMOS implementation. The level detectors produce scaled versions of the peak filter outputs, V_{LP} and V_{HP}. As long as the peak values in Eqs. (5.5) and (5.6) are scaled by the same amount, then an added scale factor in Eq. (5.4) will cancel out and all of the previously derived equations still apply. The CMOS level detector is shown in Fig. 5.6.

The circuit accepts a differential input, V_{in+} and V_{in-}. As mentioned in Sec. 3.2, a differential signal is typically available at the IF stage of an RF circuit. This design uses two unbalanced source-coupled pairs with a cross-coupled input stage and parallel-connected output stage [21]. The output is a full-wave rectified version of the input. One device in each input differential pair is scaled by a factor of K relative to the other input device. This results in an output current (labeled in Fig. 5.6) of

$$I_{out} = -2(K-1)K\beta V_{in}^2 - 4K\beta\,|V_{in}|\sqrt{(K+1)\frac{I_o}{\beta} - KV_{in}^2} + \frac{2KI_o}{K+1} \tag{5.34}$$

where K is the scale factor, $\beta = \mu_n(C_{ox}/2)(W/L)$, I_o is the bias current for each differential pair, and V_{in} is the input voltage. When $K = 1$ (corresponding to balanced input pairs), the first V_{in}^2 term is eliminated and the rectification property of this circuit is lost.

R5 is present to convert the rectified output current to a voltage. The average value of the rectified output voltage is equal to a scaled version of the peak input voltage. A

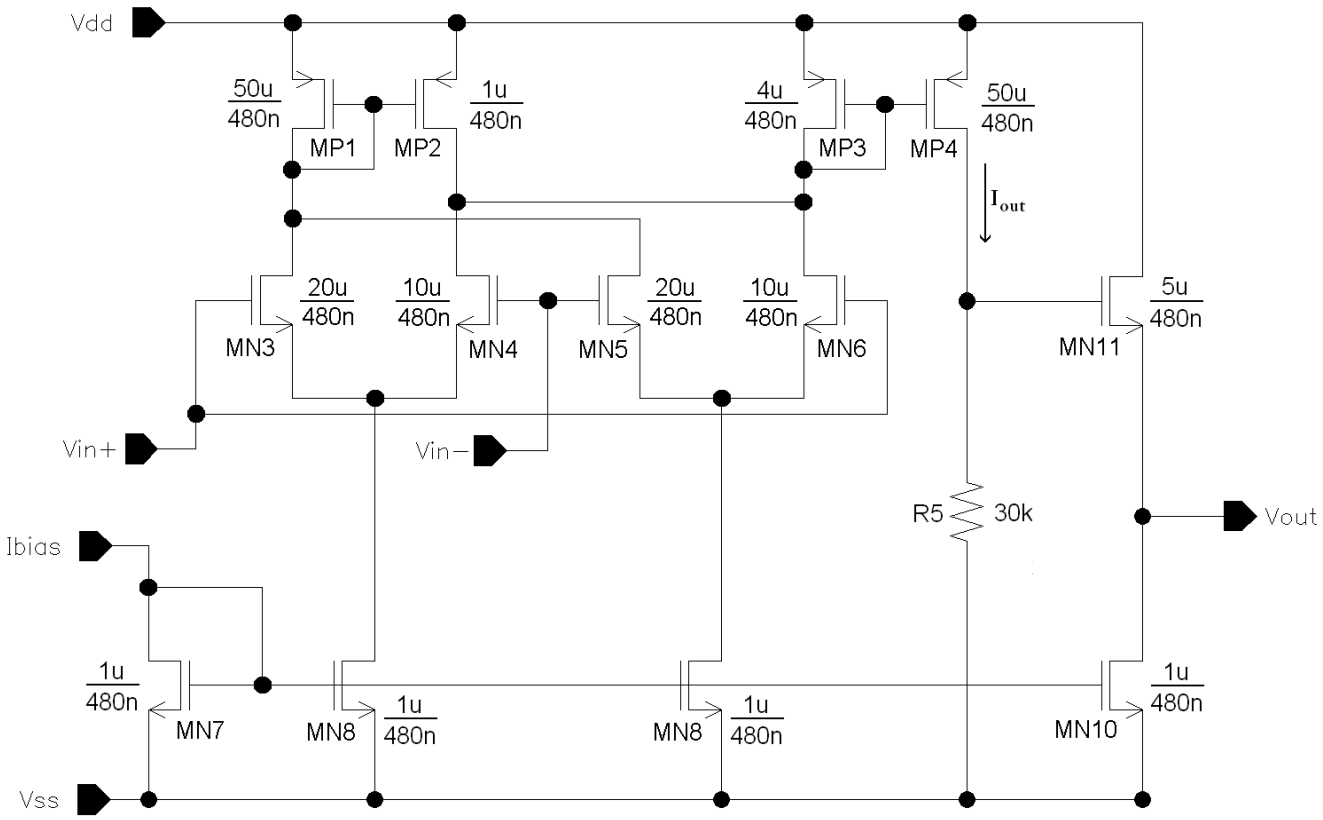

Figure 5.6: Level detector schematic.

dedicated low-pass filter would normally be required to provide this average value, but since rectification doubles the frequency of the input signal, the finite bandwidth of the level detector effectively acts as a low-pass filter such that the level detector output is equal to the average value of the rectified input signal. MN11 provides a level shift so that the level detector DC output voltage properly biases the next stage. Each level detector consumes $120\,\mu A$ of current.

5.3.3 Differential Amplifier

The differential amplifier is implemented using a two-stage op-amp architecture, shown in Fig. 5.7. The amplifier performance specifications are summarized in Table 5.1. The differential amplifier has high gain in order to achieve low gain error (see Eq. (5.33)). The amplifier is compensated using the pole splitting method. The phase margin is lower than the typical 65° where maximal flatness is achieved, but the amplifier will never be used

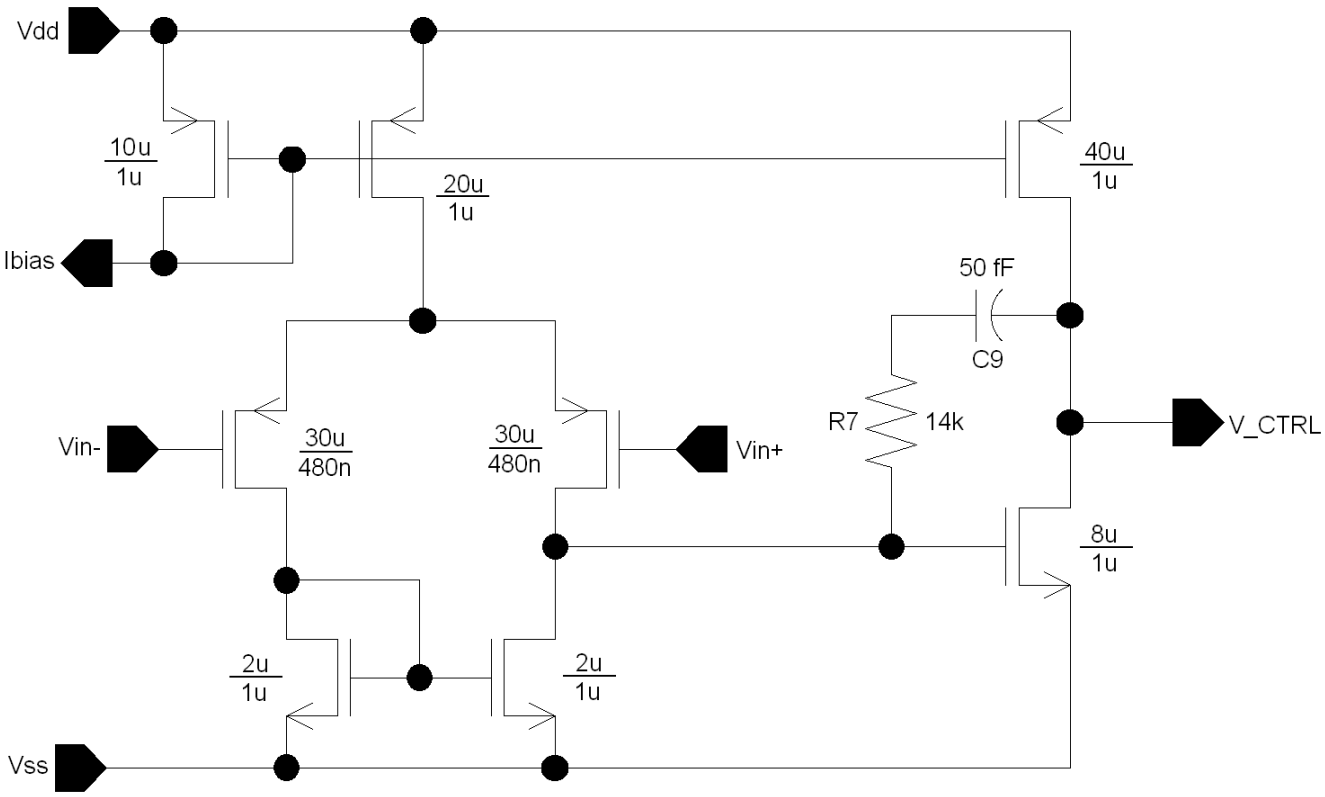

Figure 5.7: Differential amplifier schematic.

Table 5.1: Differential amplifier specs

Power Supply (V)	3.0
Total Current (μA)	70
DC Gain (dB)	84
Unity Gain (MHz)	355
Phase Margin (degrees)	28

in the worst-case unity gain configuration. The amplifier has at least 72° phase margin over the operating frequency range. No output buffer is used as the amplifier will drive a small capacitive load.

5.3.4 System Circuit

The complete system schematic is shown in Fig. 5.8. To maintain cleanliness in the schematic, only the components that require commentary have been labeled. The circuit

is fully differential and consumes 310 μA of current. The differential input signals are labeled V_{in+} and V_{in-}. The differential outputs, V_{out+} and V_{out-}, are taken at the MOS-implemented RC-CR filters in the first stage. R1-R4 are present to bias the inputs to the level detectors, with C6-C8 acting as AC coupling capacitors between the RC-CR filters and level detectors. This biasing scheme allows the drain-source DC voltages of devices MN1-MN4 to be zero. This ensures that the devices are operating in the deep triode region by satisfying the requirement that $V_{DS} \ll 2(V_{GS} - V_{TH})$.

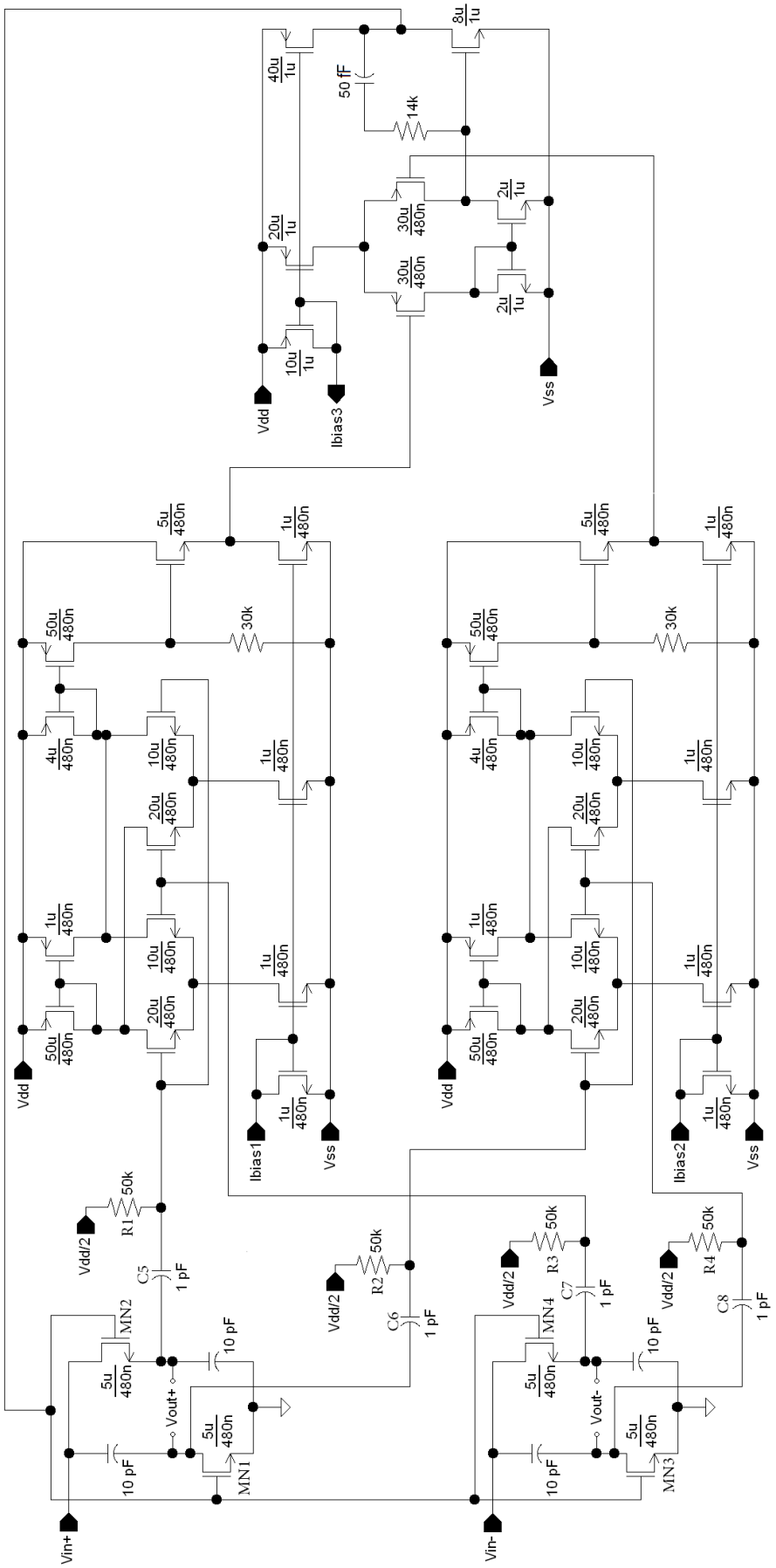

Figure 5.8: System schematic.

Chapter 6

Simulation Results

6.1 Results

The system operates over a bandwidth of 16 MHz, centered at an IF of 35 MHz. The choice of IF will be discussed in the next section. The IRR can be calculated using simulated values of phase and gain error according to the following equation [15, 13],

$$IRR_{dB} \approx 10\,log\frac{4}{(\Delta\theta)^2 + (\Delta G)^2} \tag{6.1}$$

where ΔG is the gain error and $\Delta\theta$ is the quadrature mismatch measured in radians. Table 6.1 summarizes system performance over temperature at nominal process.

Table 6.1: IRR performance (nominal process)

27°C

	27 MHz	31 MHz	35 MHz	39 MHz	43 MHz
ΔG	0.0039	0.0029	0.0014	0.0006	0.0018
$\Delta\theta$ (degrees)	0.03	0.23	0.32	0.34	0.32
IRR (dB)	54.12	52.12	50.82	50.51	50.65

0°C

ΔG	0.0050	0.0039	0.0027	0.0015	0.0003
$\Delta\theta$ (degrees)	0.27	0.13	0.29	0.35	0.35
IRR (dB)	49.32	52.93	50.85	50.05	50.29

70°C

ΔG	0.0024	0.0011	0.0020	0.0039	0.0073
$\Delta\theta$ (degrees)	0.16	0.29	0.3	0.3	0.25
IRR (dB)	54.67	51.73	50.80	49.91	47.38

The results show an average IRR of about 50 dB, which is a very good figure. The gain error is less than 1% in all cases. As predicted in Section 5.3.1, a small phase error is present. The equations developed in Section 5.2.3 show that when mismatch is present in some form, a phase error will likely result. Although the transistors and capacitors are all matched in simulation, the phase error can be explained by observing in Fig. 5.8 that the two MOS devices in each RC-CR filter have the same gate voltages but unequal small-signal source voltages. This time-varying inequality of source voltages will cause a mismatch in the MOS channel resistances, resulting in a phase error. Additionally, the channel resistance is also a weak function of the drain-source voltage. The source voltage inequality has already been noted, but the instantaneous values of the small-signal drain voltages are also unequal due to the phase difference across those two nodes. This likely contributes an additional small amount to the phase error.

20 mV peak-to-peak differential input signals were used in the transient simulations. As expected, the phase error increases as the small-signal input voltage increases, which degrades the IRR. If the typical signal voltage at the IF stage in a particular system were higher than what this image-reject system could accommodate, then adjustments or additional circuitry would be required. The conversion gain of the quadrature mixers preceding the IF stage could possibly be lowered, or the mixer output could simply be attenuated. Alternatively, if the system did not have a high IRR requirement, a larger input signal could be used at the expense of IRR performance.

Since constant amplitude response is achieved only at the pole frequency, the output also has a 3 dB drop relative to the input. This is a relatively small attenuation by itself and would probably not require make-up gain. If additional gain is necessary for any of the preceding reasons, this could possibly be achieved through the programmable-gain amplifier that typically follows the IF stage (see Fig. 3.2).

As noted in Ch. 5, the circuit requires good matching to guarantee good performance. One set of 4 MOS devices and one set of 4 capacitors must be matched. This is similar to the matching requirement for a one-stage polyphase filter. One of the primary strengths of this circuit is that it does not require high precision. So long as the components are well-matched, the absolute value of the component parameters can shift due to process

variations or temperature effects, and the feedback network will compensate to maintain good performance. IRR performance over process and temperature is summarized in Table 6.2. The results show that the system does in fact maintain an average IRR of 50 dB over process and temperature.

Table 6.2: IRR performance over process and temperature

Fast-Fast, 27°C

	27 MHz	31 MHz	35 MHz	39 MHz	43 MHz
ΔG	0.0046	0.0037	0.0024	0.0007	0.0005
$\Delta\theta$ (degrees)	0.18	0.18	0.31	0.34	0.34
IRR (dB)	51.13	52.46	50.65	50.39	50.57

Fast-Fast, 0°C

ΔG	0.0032	0.0019	0.0010	0.0021	0.0038
$\Delta\theta$ (degrees)	0.08	0.27	0.32	0.32	0.29
IRR (dB)	55.16	51.96	50.95	50.60	50.07

Fast-Fast, 70°C

ΔG	0.0053	0.0047	0.0036	0.0024	0.0013
$\Delta\theta$ (degrees)	0.48	0.04	0.26	0.34	0.36
IRR (dB)	46.10	52.60	50.89	49.92	49.87

Slow-Slow, 27°C

ΔG	0.0030	0.0021	0.0009	0.0007	0.0032
$\Delta\theta$ (degrees)	0.08	0.27	0.33	0.32	0.29
IRR (dB)	55.63	51.77	50.72	51.01	50.47

Slow-Slow, 0°C

ΔG	0.0016	0.0021	0.0038	0.0061	0.0110
$\Delta\theta$ (degrees)	0.22	0.30	0.30	0.27	0.20
IRR (dB)	53.85	50.99	49.80	48.28	44.78

Slow-Slow, 70°C

ΔG	0.0041	0.0032	0.0020	0.0007	0.0010
$\Delta\theta$ (degrees)	0.11	0.20	0.32	0.34	0.33
IRR (dB)	52.90	52.42	50.57	50.49	50.70

6.2 Comparison

This section compares the IRR performance of this work to publications of other analog image-reject systems. The image-reject system in [22] achieves an IRR of 58 dB across a 10 MHz channel. This is a superior IRR figure, although the bandwidth is smaller than that of this work. The authors note that the RC product in a polyphase stage can vary by as much as ±25%. To account for these process variations and ensure the 10 MHz bandwidth, the number of polyphase filter stages was increased to perform the image rejection across a nominal bandwidth of about 15 MHz (10 MHz ±25%). The feedback network in the system of this work reduces the need to "over-design" in this manner in order to overcome process variations, which reduces layout area. The design in [22] requires matching accuracy of 0.1% for all polyphase stages to guarantee that the system will achieve its targeted IRR of 60 dB. Since component variance is inversely proportional to layout area, large area resistors and capacitors were used in order to achieve good matching.

The receiver in [22] uses the double-quadrature approach, which has the IF mixer inputs in quadrature phase in addition to the mixer LO inputs. The system has four IF mixers, two IF stages, and seven total stages of polyphase filters. This is a relatively large and complex system, whereas the circuit of this work is comparatively much smaller and simpler. The motivation for using a double-quadrature receiver is that quadrature matching of the polyphase filters need only be 3% in order to achieve an IRR of 60 dB, whereas a single-quadrature receiver requires 0.1% quadrature matching for the same performance (not to be confused with the 0.1% *component* matching discussed in the preceding paragraph).

The system of [22] has 191 pF of total capacitance compared to 40 pF in this work. This translates to a substantial decrease in layout area, although it must be noted that the system of this work would require additional capacitance to match the 10 MHz IF of [22]. One of the major drawbacks of polyphase filters is significant attenuation. The signal in [22] suffers a 25 dB loss through the five-stage polyphase filter path and requires two interstage amplifiers to compensate. The filter in this work attenuates by only 3 dB, but the filter stage can only accept signals with small voltage swings.

The work in [23] uses a similar double-quadrature system to achieve an IRR of 58 dB over an 8 MHz bandwidth. Large area components were used to achieve good matching, as

in [22], as well as designing for an excessively large nominal bandwidth to ensure the target bandwidth over RC process variations. No mention is made of signal attenuation through the four-stage polyphase path. 32 pF of total capacitance is used. Table 6.3 provides a performance summary of the systems compared in this section.

Table 6.3: Comparison of image-reject systems

	IF	bandwidth	IRR	power	capacitance
this work	35 MHz	16 MHz	50 dB	0.93 mW	40 pF
[22]	10 MHz	10 MHz	58 dB	>62.7 mW	191 pF
[23]	36 MHz	8 MHz	58 dB	11 mW	32 pF

As no layout area information is available for [22] or this work, total capacitance is used to give insight into circuit size since capacitors typically dominate the layout area. The power consumption listed for [22] is only for the interstage amplifiers and does not include the four IF mixers. Since [23] makes no mention of the well-known attenuation problem of polyphase filters, it is fair to assume that one or more amplification stages may be necessary, as in [22], which would increase power consumption.

The image-reject systems of [22] and [23] both make use of double-quadrature mixers to relax the quadrature matching requirement. As a result, a high IRR is achieved at the cost of complexity and power consumption. Additionally, the nominal bandwidth of the systems must be increased to counter process variations. This is done by increasing the number of polyphase stages, which increases layout area and signal attenuation. The advantages of the image-reject system of this work are simplicity, reduced power consumption, and reduced sensitivity to process variations. This last point results in reduced layout area by eliminating the need to over-design in order to counter process variations. The disadvantage is the limitation on input voltage swing.

6.3 Application

The circuit can be used to perform image rejection using the Hartley method in an 802.11a low IF receiver. An 802.11a system requires 16 MHz of bandwidth, which is

satisfied by this system. The ideal IF for an 802.11a receiver is 10 MHz, which places the entire range of image frequencies within the bandwidth that is regulated by the 802.11a standard. This ensures that the image signal will be below a certain power level, making the required IRR more predictable. With an IF of 35 MHz, 65% of the image band falls within the 802.11a regulated bandwidth. The remaining portion of the image band would need to be investigated by the system designer to see what regional standard the spectrum is regulated by. An image rejection of at least -32 dBc is desirable [13].

35 MHz was chosen as the IF in order to reduce the size of the RC-CR filter capacitors. As the required pole frequency decreases, the RC product must increase. If C remains fixed and R is increased to achieve a lower pole frequency, ΔR (defined in Eq. (5.17)) increases, which causes ΔV_{CTRL} to increase as well (see Eq. (5.18)). As discussed in Section 5.3.1, a large ΔV_{CTRL} is undesirable because it increases the phase error. A lower IF can nonetheless be used by increasing the size of the filter capacitors and adjusting the widths of the MOS devices in the RC-CR filter in order place ΔV_{CTRL} in the desired location.

Although the circuit of this work is intended for wideband applications, it could still find use in narrowband applications because of its reduced sensitivity to process variations. Traditional RC-CR filters are only used in narrowband applications since they cannot be cascaded to provide wideband image rejection in the same way that polyphase filters can. Thus, buffering the bandwidth with additional filter stages to combat process variations, as in [22] and [23], is not possible. Process variations in the RC product might unacceptably degrade the IRR of an RC-CR filter by shifting the pole frequency too far from the IF. By replacing a traditional narrowband RC-CR filter with the circuit of this work, a greater manufacturing yield and more consistent performance could be achieved at the expense of added power consumption and layout space.

Since the circuit of this work provides a control signal that is proportional to the input frequency, it could also be used in frequency detection applications. The typical method of analog frequency detection requires a PLL, which is a feedback system consisting of a phase/frequency detector, charge-pump, and VCO. Each one of these by itself can be complicated and difficult to properly design. The circuit of this work performs frequency detection in a significantly simpler system.

Chapter 7

Conclusion

A wideband, precision quadrature phase shifter was designed which was shown to have sufficiently low phase and gain error to achieve 50 dB of image rejection over a 16 MHz bandwidth. The circuit operates by using an RC-CR filter in a feedback loop which adjusts the pole frequency of the filter to match the frequency of the input signal. The circuit gives comparable performance to other similar systems, but with less power and reduced sensitivity to process variations. Such a system can be used to perform image rejection in an 802.11a low IF receiver using the Hartley method. This system could also improve performance and yield in receivers employing a traditional narrowband RC-CR filter because of the reduced process variation sensitivity.

7.1 Suggestions for Future Research

IRR performance could be improved with a better VCR. Two major shortcomings of the use of single-device MOS transistors as the VCRs in the system of Fig. 5.4 are the presence of two control terminals and the requirement that $V_{DS} \ll 2(V_{GS} - V_{TH})$. These problems limit the accuracy of the circuit and preclude large voltage swings at the input. A wide-swing CMOS VCR with a single control port implemented in the system of Fig. 5.4 would yield greater accuracy and versatility.

Another application for this circuit is the generation of quadrature VCO (QVCO) signals. If the CMOS circuit blocks were optimized to operate at RF frequencies, such a circuit could use the signal generated from a VCO to produce a precise quadrature counterpart. QVCO signals are more difficult to produce at RF frequencies, but the feedback of the system in Fig. 5.4 desensitizes the quadrature matching to process and temperature variations. An on-chip RC time constant in a polyphase filter may vary by as much as $\pm 25\%$

[22]. Good matching of RC-CR filter components would still be required, but the circuit could maintain accuracy while allowing the absolute value of the matched components to vary.

As noted in Sec. 6.3, the circuit of this work could also be used in frequency detection applications. Additional research could be done to determine how well it performs in this regard compared to traditional methods of frequency detection.

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Appendix A

Constant Amplitude Response with Mismatched Components

This appendix provides a proof that the system of Fig. 5.4 will still drive the output to constant amplitude response when the RC-CR filter components are mismatched.

A.1 Proof

The output voltages of the low-pass and high-pass branches of the RC-CR filter are first defined as

$$V_{LP} = \frac{1}{\sqrt{1 + (\omega C_{LP} R_{LP})^2}} \cdot V_{in} \tag{A.1}$$

and

$$V_{HP} = \frac{\omega C_{HP} R_{HP}}{\sqrt{1 + (\omega C_{HP} R_{HP})^2}} \cdot V_{in} \tag{A.2}$$

where C_{LP} and R_{LP} are the low-pass filter components, and C_{HP} and R_{HP} are the high-pass filter components. If constant amplitude response was achieved, this would occur at the frequency where Eqs. (A.1) and (A.2) intersect. Solving for this frequency gives

$$\omega = \frac{1}{\sqrt{R_{LP} R_{HP} C_{LP} C_{HP}}}. \tag{A.3}$$

The values of C_{LP} and C_{HP} are fixed, but the values of R_{LP} and R_{HP} are both variably controlled by the feedback network through a single control signal, V_{CTRL}. Solving Eq. (A.3) for R_{LP} and R_{HP} gives

$$R_{LP} = \frac{1}{\omega^2 R_{HP} C_{LP} C_{HP}} \tag{A.4}$$

and

$$R_{HP} = \frac{1}{\omega^2 R_{LP} C_{LP} C_{HP}}. \tag{A.5}$$

The resistors in the low-pass and high-pass filter branches must be equal to Eqs. (A.4) and (A.5), respectively, in order to achieve constant amplitude response. The question is whether or not the feedback network is capable of simultaneously satisfying both of these equations with a single control signal. From Eq. (5.3), the VCR equations are now redefined as

$$R_{LP} = \frac{R_{o-LP}}{V_{CTRL}} \tag{A.6}$$

and

$$R_{HP} = \frac{R_{o-HP}}{V_{CTRL}} \tag{A.7}$$

where R_{o-LP} and R_{o-HP} are the VCR constants for the low-pass and high-pass filter VCRs. Solving for V_{CTRL} and equating Eqs. (A.6) and (A.7) gives

$$\frac{R_{o-LP}}{R_{LP}} = \frac{R_{o-HP}}{R_{HP}}. \tag{A.8}$$

This relationship defines the values of R_{LP} and R_{HP} that are possible when both VCRs are controlled by a single control voltage. If this relationship can be used to simultaneously satisfy Eqs. (A.4) and (A.5), then the system can achieve constant amplitude response. Solving Eq. (A.8) for R_{LP},

$$R_{LP} = \frac{R_{o-LP}R_{HP}}{R_{o-HP}}. \tag{A.9}$$

Substituting Eq. (A.9) into Eq. (A.4),

$$\frac{R_{o-LP}R_{HP}}{R_{o-HP}} = \frac{1}{\omega^2 R_{HP}C_{LP}C_{HP}}. \tag{A.10}$$

Rearranging terms and substituting Eq. (A.9) into Eq. (A.10) gives

$$R_{HP} = \frac{R_{o-HP}}{R_{o-LP}} \frac{1}{\omega^2 R_{HP}C_{LP}C_{HP}} = \frac{1}{\omega^2 R_{LP}C_{LP}C_{HP}}. \tag{A.11}$$

Equation (A.11) is equal to Eq. (A.5), so R_{HP} is capable of reaching its desired value. Repeating the procedure in Eqs. (A.9) through (A.11) for R_{LP},

$$R_{HP} = \frac{R_{o-HP}R_{LP}}{R_{o-LP}}. \tag{A.12}$$

Substituting Eq. (A.12) into Eq. (A.5),

$$\frac{R_{o-HP}R_{LP}}{R_{o-LP}} = \frac{1}{\omega^2 R_{LP}C_{LP}C_{HP}}. \tag{A.13}$$

Rearranging terms and substituting Eq. (A.12) into Eq. (A.13) gives

$$R_{LP} = \frac{R_{o-LP}}{R_{o-HP}} \frac{1}{\omega^2 R_{LP}C_{LP}C_{HP}} = \frac{1}{\omega^2 R_{HP}C_{LP}C_{HP}} \tag{A.14}$$

which is equal to Eq. (A.4). Since Eqs. (A.4) and (A.5) can be simultaneously satisfied with a single control voltage, constant amplitude response can indeed be achieved when the RC-CR filter components are mismatched.