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A Survey of Pattern Classifier Research

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I. Introduction

This paper is a survey of research on pattern classifier. In particular, it emphasizes on the different types of pattern classifiers and their performance factors. Pattern classifiers use the algorithms of pattern recognition to classify various input classes into their respective categories. Recently many algorithms for pattern classifiers have been proposed. However no study of the normalized performance of pattern classifier has been done. Based on the implementation methods, in general there are three types of pattern classifiers: I.C. based, optical based, and software based using general-purpose computers. Advantages, disadvantages, and performance factors of each classifiers is discussed in this survey. Based on the presented facts, we can create benchmarks and normalized performance for pattern classifiers. Our future research will focus on building a pattern classifier in accordance with the normalized performance standard.

II. Pattern Classifier

A. I.C. Based Pattern Classifier

This section presents the current research of pattern classifier based on the technology of integrated circuits. The classification is very time consuming when the number of template vectors in the classification system is large. According to the demanding computation involved with the classification, the idea of direct hardware implementation using parallel VLSI architecture is proposed for high speed real time applications. There are a number of advantages to use the technique of integrated circuits to build pattern classifier.

A.1 Pattern classifier proposed by Masa and et al.

P. Masa, K. Hoen, and H. Wallinga [1], [2]discussed a pattern classifier using CMOS neural network integrated circuit. This circuit is designed for very high speed applications. As is known, it is a very challenging task to realize the inner product operation for neural networks in hardware. This paper proposes a method to combine the analog computing technique and the digital weight storage in the parallel architecture of the pattern classifier. The chip implements a fully connected feed forward neural network with 70 inputs, 6 hidden layer neurons, and one output neuron. This single chip pattern classifier can classify as high as 70 dimensional vectors within 20 nanoseconds, performing 20G multiply-and-

add operations per second. The circuit occupies $10 * 9mm^2$ silicon area with 1.5um CMOS process and dissipates only 1W at 5V supply. This circuit demonstrated the advantages of analog computing in real-time pattern classification. Table 1 shows more details about the specifications of the chip discussed.

TABLE I

Chip Specifications

Total processing delay	20 nanoseconds
Computation speed	20G multiplication and additions per second
Equivalent input bandwidth	4000 Mbytes/second
Number/resolution of synapses	426,5 bits (4 bits + sign)
Synapse size	$400 * 70um^2$
No. of transistors	40,000
PGA package	144 pins
Chip size	$10mm * 9mm$(1.5 DLM CMOS, ES2, EUROCHIP)
On-chip static RAM	3750 bits
Power dissipation	$<$ 1W

Dr. Masa wrote, "Analog VLSI offers compact, high speed but moderate precision analog computing. With a standard CMOS process up to tens of thousands of synapses can be integrated on a single chip resulting up to ten-thousand fold parallelism in the computing. This parallelism can not be achieved with digital technique, because the inner product computing requires too large chip area." Dr. Masa made his point in the paper "70 inputs, 20 nanosecond pattern classifier" by demonstrating the high speed pattern classification.

A.2 Pattern classifier proposed by Shibata and et al.

T. Yamasaki and T. Shibata [3], [4]developed an analog CMOS pattern classifier circuit based on a robust image representation algorithm called projected principal-edge distribution (PPED). With the use of the floating-gate MOS technology, the flexible pattern matching operation is made tunable by altering the sharpness of the similarity evaluation

as well as the peak position and the peak height. The test chip was made in a 0.6um CMOS process with the supply of 4V and successfully applied to the simple handwritten pattern recognition. The PPED image representation algorithm is developed to reduce the data dimensionality by mapping a 2-D image to a feature vector while preserving the essential features in the original image. Input image which consists of 64∗64 pixels are converted to 64 dimension feature vectors. A problem resulted from the present test circuits are only for 16 dimension vectors. The experiments reduced the number of elements by merging each set of four neighboring elements into one without seeing significant performance degradation. The classifier chip contains 15 vector matching circuits. Each element matching circuit occupies the area of 150um∗110um in the pyramid-type and 170um∗ 180um in the plateau type for eight levels of functional form variation. However, more than half of the area is occupied by capacitors. An increased area-efficient layout would be possible by employing the advanced capacitor technologies. In the circuit, the external D/A converters in the measurement setup limit the time required to write template vectors. The writing time needed was 10-100us in the handwritten recognition experiment. In contrast, the time for winner searching depends on the speed of the ramp-down voltage, which can be less than 200ns claimed by Shibata and et al.

B. Optical Based Pattern Classifier

Optical computation employs the advantages of optics in processing speed, parallelism, and interconnection. Many research [5], [6], [7] have heavily concentrated on optical character recognition (OCR) of printed texts. There is also research on other optical pattern classifier. To achieve better performance, suitable input /output devices such as SLMs (spatial light modulators) and detectors are necessary for the optical pattern classifier.

C. Software Based Pattern Classifier Using General Purpose Computer

Pattern classifiers based on software are computationally very expensive. It is impractical to build real-time response processing system by software so far.

III. Normalized Performance Benchmarks

Pattern Classifiers are important in many areas that include defense, medicine, business, and etc. We create benchmarks and normalized performance for pattern classifiers based on more collected aspects of different types of classifiers.

IV. Future Research

Our future research will focus on building a pattern classifier in accordance with the normalized performance benchmarks that we create.

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