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A Pixel Scale Digital-to-Analog Converter Array for Liquid Crystal on VLSI Displays

Gregory P. Nordin
nordin@byu.edu

S. T. Kowel

J. H. Kulick

R. G. Lindquist

P. J. Nasiatka

See next page for additional authors

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under the condition that $[(w_{p-m},\cdots,w_{p-1}),q] \in \eta[(x_{p-m},\cdots,x_{p-1}),r_3] \times \eta(\theta,r_4)$. But this condition is met because $b < r_4$ and $|w_n - x_n| \le K|\sum_{k=1}^{m} b_k(w_{n-k}-x_{n-k})| + |q_n|, n \ge 0$ with $w_n = x_n$ for $n = -m,\cdots,-1$. This completes the proof of the theorem.

Comments: Very direct modifications of the proof establish a corresponding theorem for digital filter models of the form

$$w_n = f\left(\sum_{k=1}^{m} b_k w_{n-k} + \sum_{k=0}^{m} a_k u_{n-k} + q_n\right), \quad n \ge 0 \qquad (10)$$

which are sometimes used. For this case, one obtains the following.

Theorem 2: Assume that conditions i)–iv) are satisfied. Suppose that for each $[u,(x_{-m},\cdots,x_{-1})] \in S(\beta) \times C$ we generate $x \in S$ according to

$$x_n = f\left(\sum_{k=1}^{m} b_k x_{n-k} + \sum_{k=0}^{m} a_k u_{n-k}\right), \quad n \ge 0$$

and that for each $[u,(x_{-m},\cdots,x_{-1})] \in S(\beta) \times C$ there is a nonnegative integer l such that $|\sum_{k=1}^{m} b_k x_{n-k} + \sum_{k=0}^{m} a_k u_{n-k}| < 1$ for $n \ge l$. Then there is a nonnegative integer p and a $b > 0$ such that $(\sum_{k=1}^{m} b_k w_{n-k} + \sum_{k=0}^{m} a_k u_{n-k} + q_n)$ of (10) satisfies

$$\left|\sum_{k=1}^{m} b_k w_{n-k} + \sum_{k=0}^{m} a_k u_{n-k} + q_n\right| < 1, \quad n \ge p$$

for any $q_0, q_1, \cdots$ with $|q_n| \le b$ $(n \ge 0)$, any $u \in S(\beta)$, and any $(w_{-m},\cdots,w_{-1}) \in C$.

The ideas used in the proof of Theorem 1 can be extended to obtain a corresponding theorem for a much more general class of finite-precision systems. In particular, a result along the lines of Theorem 1 can be given for systems governed by a state equation that takes into account several nonlinearities.[3]

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[3]The related problem of bounding the amplitude or norm of limit cycles under the (typically tacit) assumption of separation has been studied by several writers. Recent results, including a comparison of bounds by different writers, can be found in [8].

A Pixel Scale Digital to Analog Converter Array for Liquid Crystal on VLSI Displays

Axel Thomsen, Robert G. Lindquist, Jeffrey H. Kulick, Patrick J. Nasiatka, Gregory P. Nordin, and Stephen T. Kowel

***Abstract*—A pixel scale digital to analog converter and driver for liquid crystal (LC) cells is presented. The circuit is a compact CMOS logic gate that sums pulse density modulation (pdm) signals. Low pass filtering of the pdm signal is done by the LC material. The circuit is suitable to implement large arrays of converters as, for example, in display applications. It is applicable in LC on silicon displays where gray scale data are stored and converted at each pixel site. Advantages over the commonly used active matrix technology include the removal of all analog circuitry, no need for refresh, reduced interconnect complexity, no capacitive loading of analog lines, and the ability to build larger scale or smart displays that combine memory, processing, and drive circuitry. Experimental results from a CMOS implementation are presented.**

I. INTRODUCTION

The integration of liquid crystalline materials with silicon integrated circuits [1]–[3] offers the opportunity to create a new generation of displays in which smart display elements are integrated with video memory and processors for decompression of visual information or scene generation [3]. Such a display could consist of a single IC, a multichip module, or a wafer depending on size and number of pixels. The surface of the silicon is planarized, patterned with electrodes, and covered with a film of liquid crystals (LC's). Each electrode has a via connection to the underlying VLSI drive circuitry as shown in Fig. 1. It depicts a pixel element currently under investigation for a 3-D diffractive display based on the previously reported partial pixel architecture [4].

In such displays, a number of unique requirements exist for the drive electronics. Currently, data to be displayed are computed and stored external from the display, for example, on a video card. The data are transferred to the display serially. Thus, a serial scanning scheme to set the pixel gray scale voltages is suitable. The active matrix scheme that uses a single global digital to analog converter and analog dynamic memory is an example. The smart display technology described above changes the storage location and data availability. The data to be displayed is stored locally in digital form and is not generated in sequential order. Thus, a local data conversion and driving scheme is more suitable, especially for high resolution or large (wafer scale) area displays. Unlike for the global driving scheme, where capacitive loading, scanning, and update rates have to be considered, the main design issue for a local circuit is the layout size. Since state of the art displays require more than thousand pixels per row or column, and die size is limited, only a small layout makes this approach feasible for a display.

We present a complete digital to analog converter and driver solution that is sufficiently compact to be integrated at each pixel site of a VLSI-based LC display. The individual element is compact, easy to design, and suitable for large arrays. We verify the operation by driving high resolution LC diffraction gratings. We analyze the layout area requirements in current and advanced CMOS technology. In addition, we illustrate how these cells can provide compensation for threshold and nonlinearity effects in the LC's.

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The authors are with the Department of Electrical and Computer Engineering, University of Alabama in Huntsville, Huntsville, AL 35899 USA.

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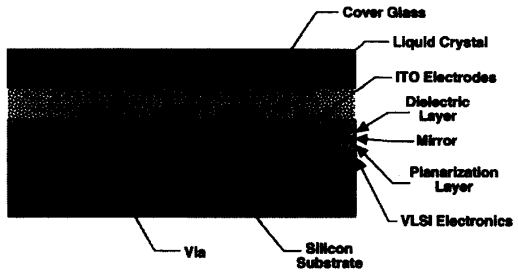


Fig. 1. Schematic of a LC on VLSI display.

II. Review

Liquid crystalline material is well established in flat panel display technology. Some of its electrooptic properties that had to be considered or were exploited in the design of the driver and converter circuit will be reviewed.

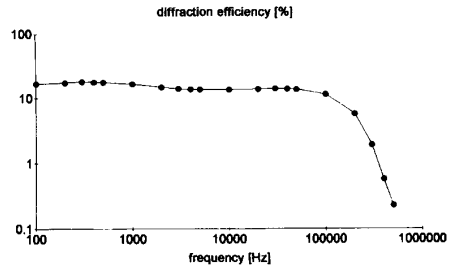
In an oscillating electric field above a minimum frequency, the rotation of the LC's is proportional to the root-mean-square (rms) value of the field and thus proportional to the rms voltage. This relationship holds above a cutoff frequency given by the inverse of the relaxation time of the LC. For the given geometry, LC alignment and LC material, this frequency is about 200 Hz. At lower frequencies, the crystal rotation starts to follow the instantaneous value. At higher frequencies above 100 kHz, the rms response of the LC's rolls off (see Fig. 2(a)), possibly due to the *RC* effects in the electrode geometry. Note that Fig. 2(a) does not show the frequency response of LC rotation, but of the resulting effect, the diffraction efficiency of a LC grating. For frequencies below the cutoff at 200 Hz, the measured diffraction efficiency is reduced, and flickering of the diffracted light is visible.

Whether the response is measured as transmissivity as in traditional displays or as diffraction efficiency as in the grating cell, the response is typically a nonlinear function of the rms voltage. Measurements in this paper were performed on a diffractive element [4]. The diffraction efficiency is given as the ratio of the power of the first order diffracted light to the power of the incident beam. The measured diffraction efficiency from the structure under test does not respond linearly to the rms value of the drive voltage. Threshold effects of the LC material and optical geometry considerations lead to an overall nonlinear response of diffraction efficiency versus rms drive voltage (see Fig. 2(b)).

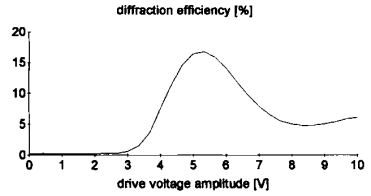
Finally, the LC material must not have a prolonged exposure to dc voltage because migration of impurities damages the material. Therefore, the average applied voltage must be zero.

The current state of the art in flat panel display driver technology uses the active matrix scheme [6]. At every pixel location is a storage capacitor and a sampling switch. The storage capacitor holds an analog gray scale value that drives the LC pixel, while the sampling switch is closed like an analog dynamic memory. The capacitor is recharged periodically from a global digital to analog converter. This system has been successfully implemented for LC on VLSI [1] using only binary values. An advantage of this technique is the minimal circuit size at each pixel. Its disadvantages for a smart display are the following.

1) A large interconnect network is required to retrieve digital data and send out analog data to each pixel location.
2) A constant refresh is required, even where pixel data do not change.



(a)



(b)

Fig. 2. Measured response of LC gratings. (a) Diffraction efficiency versus driver frequency. (b) Diffraction efficiency versus rms voltage of drive signal based on amplitude variation.

3) An array size limitation is given by the drive capability of the analog buffers.
4) The high voltages that may be required to achieve good contrast ratio in liquid crystalline material have to be routed and switched by many transistors.
5) For an IC fully covered with pixels, the large global drive circuitry presents a problem in floor planning.

An array of digital to analog converters with a voltage output can be built in several ways. Common approaches in VLSI technology are based on either resistors or capacitors. However, to achieve proper scaling and reasonable device parameters, a converter based on these devices would have a large layout area [7]. A design alternative is the use of pulse density modulation (pdm). The pdm based digital to analog converters are suitable for short channel VLSI technology. They are used successfully for high resolution audio applications [8].

III. Circuit Design

The core of the converter driver cell is a single AOI gate that realizes the logic equations

$$Z_0 = -c(p_0 d_0 + p_1 d_1 \cdots + p_n d_n)$$
$$Z_1 = c(p_0 d_0 + p_1 d_1 \cdots + p_n d_n)$$

where Z_0 and Z_1 are the outputs, the p_i are the globally generated pdm signals, d_i the data in local memory, and c the carrier signal. The drive voltage is the differential voltage between Z_0 and Z_1. In the simplest linear case, the pdm signals are nonoverlapping with a duty cycle D of $D(p_n) = 2^{-n}$. Fig. 3 illustrates the operation with an example for a duty cycle of 62.5%. The data and the master pdm signals are multiplied, then summed in the OR gate, resulting in a waveform with the duty cycle that corresponds to the input data. The carrier signal c is twice the highest bit frequency with 50% duty cycle. It is required so that the resulting differential output has zero average value. For every pulse where Z_0 is positive with respect to Z_1, there

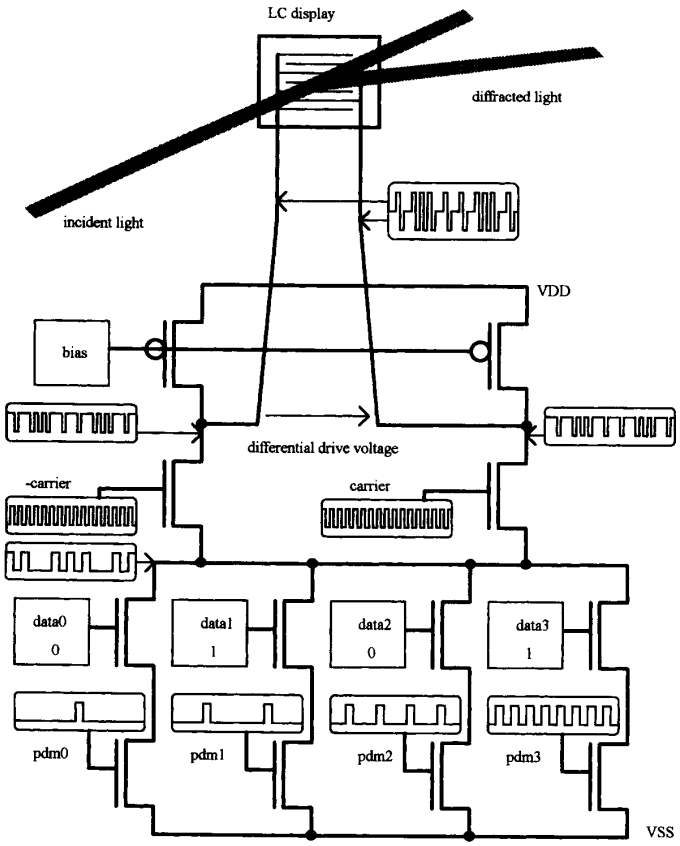


Fig. 3. Circuit diagram of the digital to analog converter cell. Illustration of the operation with a data input of 1010 and 62.5% duty cycle output.

is a pulse of similar length where Z_1 is positive with respect to Z_0. The load resistor that is needed in this single gate DAC was chosen as a p-channel load device that is externally biased. This option provides the smallest layout area without reducing the voltage swing.

The signal can have a frequency content that is limited on the upper end by the roll-off in response of the LC above 100 kHz and on the lower end by the low pass filter cutoff given by the LC at around 200 Hz. This ratio of $f_{\max}/f_{\min}$ allows for more than 256 levels or 8 b of gray scale. The settling time requirements for the circuit are thus easy to meet using minimum size devices and small bias currents. Compared to most analog design tasks, this is a very simple, robust circuit to implement.

Due to the inherent low pass filter property of the liquid crystalline materials, no electronic low pass filtering of the pdm signal is required, thus leading to a simple system. A set of globally generated master pdm signals is needed, but their distribution requires only n lines for 2^n gray levels. These digital signals are easy to buffer and restore after transmission over long distances.

An integral part of the cell layout is the memory structure. By integration of the memory with the converter, layout area can be minimized. The interconnect and thus the required contacts and wire spacings are significantly reduced in an integrated layout. An analysis of the converter layout based on the 6-transistor SRAM cell [9] shows that in a 4-b cell, only 20% of the area is taken up by the converter/driver. For the 8-b case, 90% of the cell layout area is memory. Several memory implementation options are available: static memory was chosen because a frequent refresh of the data could not be guaranteed in the application under consideration [3]. A more compact alternative is dynamic memory (DRAM). For experimental DRAM processes, cell sizes of 0.6 μm $\times$ 1.2 μm per bit have been reported [11]. It depends on the application which memory alternative should be used. If a sufficient update rate can be assumed or refresh amplifiers are implemented, DRAM appears most advantageous for the most compact layout.

Several enhancements to the basic circuit are possible: Fig. 2(b) shows a nonlinear relationship between drive voltage and diffraction efficiency. For a display application, a linear relationship between input code and diffraction efficiency is desired. To compensate for these nonlinearities in the LC response, various adjustments to the pdm signals can be made. Overlap of the master pdm signals can create nonlinear relationships of input data and output duty cycles. Fig. 4 shows the pulse sequences and the resulting nonlinear response of duty cycle versus memory data (octal). The example illustrates how threshold and saturation effects can be overcome. Overlap of the pulses creates this nonlinear relationship of input code and output duty cycle.

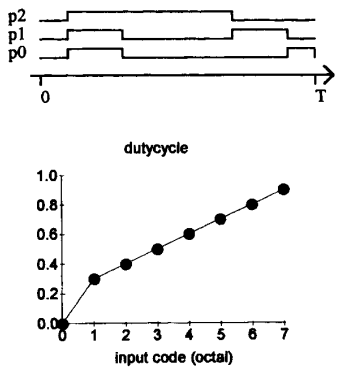


Fig. 4. Example of modified pdm waveforms to overcome threshold and saturation effects: waveforms (top), duty cycle versus input data (bottom).

IV. Results

The operation of the driving circuit with and without a LC cell has been verified. The logic function of the gate was tested. Then the differential output was attached to the two electrodes of a LC grating. The carrier frequency was 16 kHz, the fundamental frequency of the pdm signal was 1 kHz. For a square wave with amplitude A and duty cycle D the rms voltage V_{rms} is given by

$$V_{\text{rms}} = A \times D^{0.5}.$$

Fig. 5 shows how the data word applied to the logic gate relates to the measured diffraction efficiency for various power supply voltages. As expected the responses are scaled segments of the curve shown in Fig. 2(b). For example, the peak of the curve in Fig. 2(b) is near 5 V rms, which corresponds to 100% duty cycle at 5 V or approximately 56.25% or 9/16 at 6.6-V amplitude. Since the peak response is at 5 V rms, the operation with 5-V power supply yielded the most useful characteristics and best resolution for a display. It offers the widest range of input data with nonzero response and monotonically increasing diffraction efficiency. It is apparent that the resolution of the system could be improved by utilizing the technique explained above. Especially for the lower drive voltages, the LC threshold reduces the number of input codes with nonzero output. Threshold compensation, linearization, and, for larger supply voltages, limitation of the maximum duty cycle will greatly improve the number of useful input codes and thus the resolution of the display.

The main goal of this paper is to demonstrate the feasibility of local digital to analog conversion for display applications. The most critical factor is the circuit size. The layout was done under MOSIS scalable CMOS rules. The IC was fabricated in 2-μm technology. The cell size for 4 b of static memory and the converter/driver is 40 $\times$ 200 lambda (scalable length unit), which for the 2-μm technology used corresponds to 40 μm $\times$ 200 μm.

The conservative layout rules used apply to 0.8-μm CMOS technology too. The layout size per converter is 20 μm $\times$ 100 μm. An eight bit version would require approximately 20 μm $\times$ 180 μm. In a 0.5-μm technology, these sizes would shrink to approximately 10 μm $\times$ 50 μm (4 b), or 10 μm $\times$ 90 μm (8 b). The use of DRAM promises significant area savings. Advanced DRAM processing can dramatically reduce the layout area dedicated to the converter/driver. With reported memory cell sizes of 0.6 μm $\times$ 1.2 μm per bit in 0.25-μm technology [10], [11], an 8-b memory and digital to analog converter could be laid out in an estimated 2.4 μm $\times$ 15 μm area. The smaller the conversion and drive circuitry, the more processing circuitry can be integrated on chip, or more resolution can be achieved. For the specific application under consideration [3], which requires static memory and an estimated pixel size of 20 μm $\times$ 100 μm, an implementation of a 4-b cell in 0.5-μm CMOS technology leaves 75% of the chip area for a processor. An 8-b cell would require almost 50% of the pixel area.

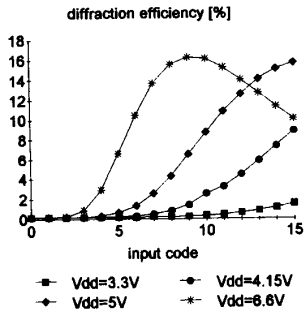


Fig. 5. Diffraction efficiency versus input code for linear pdm driving scheme.

The most suitable technology though must offer sufficient drive voltage for the LC rotation, so that an optimum technology choice may be a small feature size digital technology with high voltage (10 V) transistor option.

V. Conclusion

A highly compact pixel scale digital to analog converter and driver for smart LC on silicon displays has been presented. Its functionality has been verified. The pdm drive techniques can take advantage of LC properties and are easy to implement in silicon. The layout area for a 4-b device with static ram is 40 μm $\times$ 200 μm in 2-μm CMOS technology, so that a circuit size of 10 μm $\times$ 50 μm is expected for implementation in 0.5-μm technology. This makes it feasible to integrate a large array of converters on a single IC with sufficient space for other circuitry. This technology can enable the integration of displays, memory, and processors for decompression or scene generation in a single unit.

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