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Design and Realization of a Single Stage Sigma-Delta ADC With Low Oversampling Ratio

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DESIGN AND REALIZATION OF A SINGLE STAGE SIGMA-DELTA ADC WITH LOW OVERSAMPLING RATIO

by

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GRADUATE COMMITTEE APPROVAL

of a dissertation submitted by

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This dissertation has been read by each member of the following graduate committee and by majority vote has been found to be satisfactory.

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ABSTRACT

DESIGN AND REALIZATION OF A SINGLE STAGE SIGMA-DELTA ADC WITH LOW OVERSAMPLING RATIO

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Department of Electrical Engineering

Doctor of Philosophy

Due to the rapid growth of the communication market, a large amount of research is in process toward a high speed and high resolution sigma-delta A/D converter. This dissertation focuses on the design of a single-stage sigma-delta A/D converter with very low oversampling ratio for the wireless application. An architecture for a multibit single-stage delta-sigma A/D converter with two-step quantization is proposed. Both the MSB and LSB signals produced by the two-step quantization are fed back simultaneously to all integrator stages, making it suitable for low oversampling ratios. The two-step ADC avoids the problem that the complexity of an internal flash ADC increases exponentially with each added bit. A segmented architecture with coarse/fine DEM and DAC is proposed to reduce the complexity of DEM and DAC due to the large internal quantizer. The consequence of the segmentation, mismatch between coarse and fine DACs can be

noise-shaped by using a digital requantization (REQ) algorithm. A second-order single-stage sigma-delta A/D converter with 8-bit two-step inner quantization is proposed in this dissertation, which employs the feed-forward branches to reduce the integrator output swing. The proposed modulator is implemented with TSMC 0.25 μm mixed-signal process, using the switched-capacitor circuit. The measured system achieves the dynamic range of 70 dB under an oversampling ratio of 16 with the REQ algorithm reducing the noise floor in the signal bandwidth by 20 dB.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1 Introduction

Data converters including analog-to-digital converters (ADC) and digital-to-analog converters (DAC) are the essential link between the real analog world and the digital world [1]. ADCs convert the analog signal to a digital counterpart, which is then processed in the digital domain while DACs convert the digital codes back into the analog signals. Data converters are always in demand with the rapid development of computing and digital signal processing. For example, electronic devices such as compact disc players, digital cameras, telephones, modems, and high-definition television (HDTV) require a high resolution and/or high speed converter to interface to the analog world [2,3].

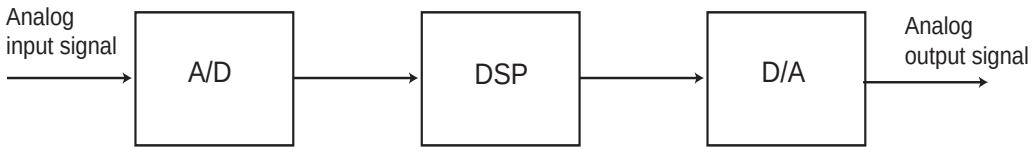

Figure 1.1 Typical Digital Signal Processing System

Figure 1.1 shows a simple block diagram of a typical signal processing system. To take advantage of the powerful digital signal processors (DSP), all input analog signals are digitalized using ADCs. After converting to digital signals, the output of the

ADC is then processed by DSP and finally converted back to analog signals through DACs.

There are two main types of ADCs, Nyquist-rate converters and oversampling converters [4]. Nyquist-rate converters are used in high-speed applications, such as video and radar signal processing, as they generate a series of output values in which each value has a one-to-one correspondence with a signal input value. However, the precision of analog components in current semiconductor processes limits the resolution of Nyquist-rate converters. Oversampling converters, on the other hand, find application in lower or medium speed applications such as digital audio and asymmetrical digital subscriber line(ADSL), as they convert a large number of analog input signal samples to their corresponding digital representations. As a result of taking more input signal samples, the oversamped converters can achieve high-resolution without using high precision analog components, making them easier to implement in modern submicron processes.

This thesis is concerned with a practical realization of an oversampled A/D converter. Section 1.1 discusses the Nyquist-rate converters while Section 1.2 is concerned with oversampled converters. Finally, an overview of this thesis is in Section 1.3.

1.1 Nyquist-rate ADC

Nyquist-rate ADCs sample the analog input signal at the Nyquist-rate $f_s=2f_b$, where f_b is the highest frequency component of the input signal. If the input signal is not bandlimited, an anti-aliasing filter must be used before the converter to prevent aliasing. Figure 1.2 shows the spectrum of the sampled input signal. A typical frequency response

of the anti-aliasing filter is shown in Figure 1.3. To ensure that the filtered signal does not contain any frequency components above $f_s/2$ [5], the anti-aliasing filter must have a very narrow transition band, which is not easy to realize.

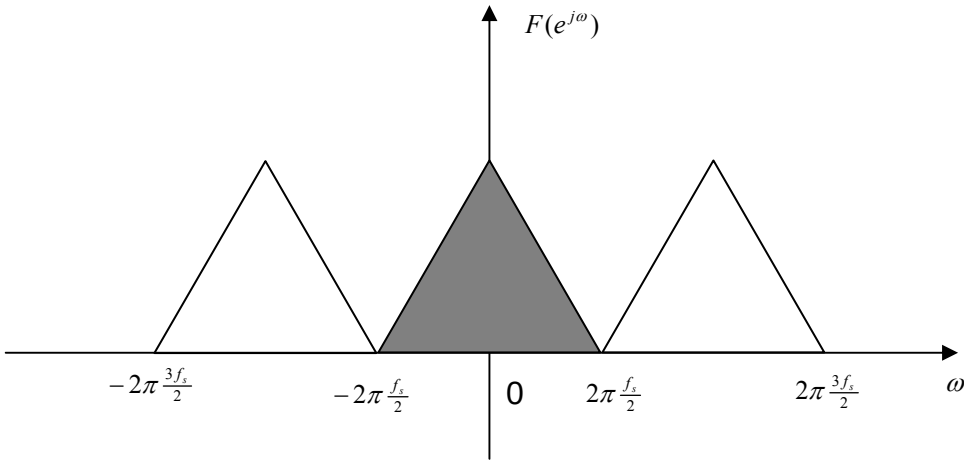

Figure 1.2 Spectrum of input signal

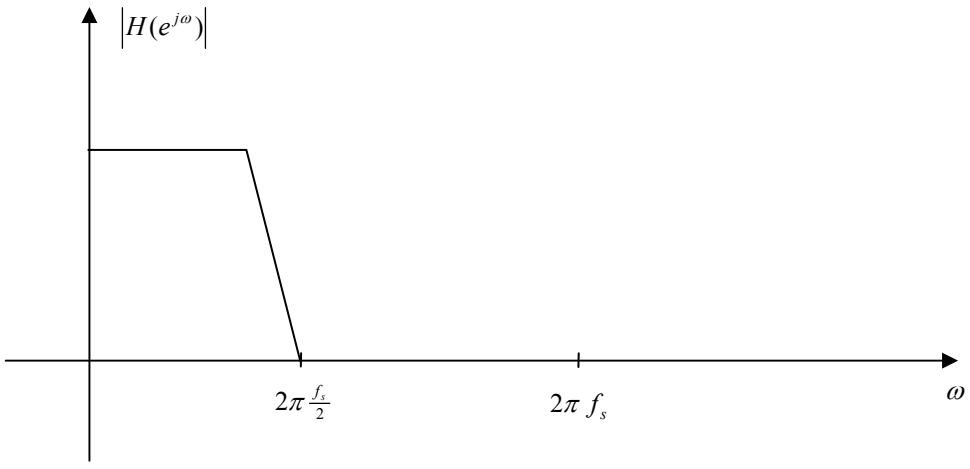

Figure 1.3 Anti-aliasing filter for nyquist-rate ADC

In the Nyquist-rate ADC, the relationship between input voltage (V_{in}), the reference voltage (V_{ref}) and the digitized results (b_0 - b_N) can be represented by

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_n 2^{-N}) = V_{in} + E_q \tag{1.1}$$

and the range of E_q , the quantization error caused by the converter is

$$-\frac{1}{2}V_{LSB} \le E_q < \frac{1}{2}V_{LSB} \tag{1.2}$$

where V_{LSB} is defined to be

$$V_{LSB} = \frac{V_{ref}}{2^N}. \tag{1.3}$$

Since there is a range of valid input values that produce the same digital output code, this signal ambiguity causes the quantization error, E_q for all A/D converters even ideal converters.

Equation (1.2) shows that the difference between the input signal and the output signal is only the quantization noise E_q. So a linear model with a simple additive noise source shown in Fig. 1.4 can be used to model the converter.

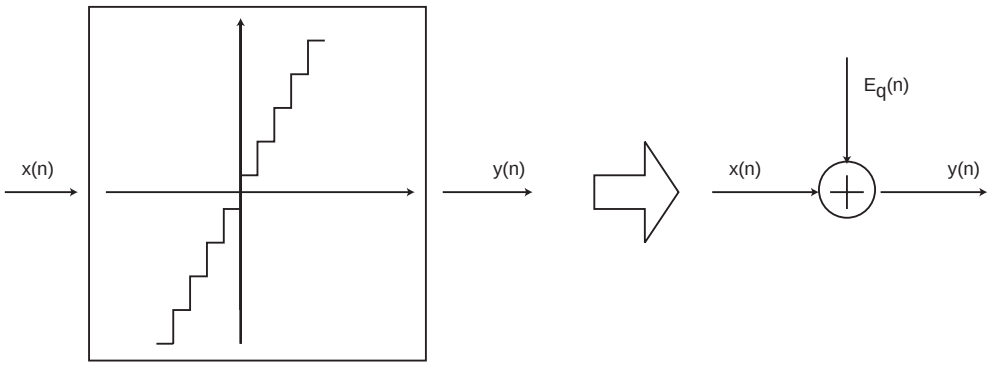

Figure 1.4 Linear model of the nyquist-rate ADC.

To gain an understanding of the properties of the quantization noise signal, E_q, a ramp signal from 0 to V_{ref} is assumed to be the input of the converter. Figure 1.5 is the sawtooth waveform of the quantization noise, E_q. Note that the quantization error, E_q is limited to LSB/2 and –LSB/2 and its average value is zero.

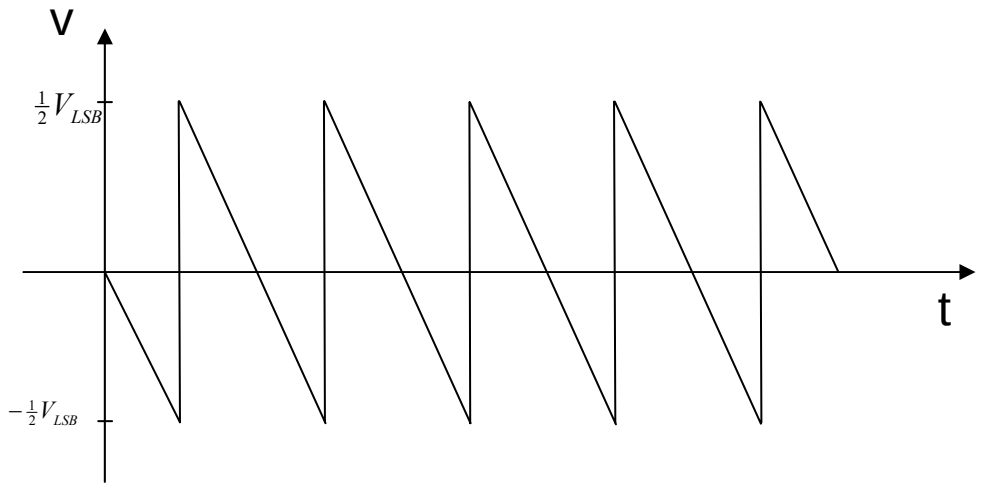

Figure 1.5 Sawtooth waveform of the quantization noise

For an arbitrary input to the converter, the quantization noise will not have a sawtooth waveform. However, we can assume that the input signal changes rapidly such that the quantization error, E_q, is a random variable uniformly distributed between $-\frac{1}{2}V_{LSB}$ and $-\frac{1}{2}V_{LSB}$ [4]. So the probability density function for such signal will be a constant value, as shown in Figure 1.6.

The power of the quantization noise error can be found as

$$P_E = \int_{-\infty}^{\infty} x^2 f(x)dx = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LsB}/2} x^2 dx = \frac{V_{LSB}^2}{12}. \qquad (1.4)$$

The above suggests that given an input signal waveform, a formula can be derived to get the best possible signal-to-noise ratio (SNR) for a given number of bits in an ideal ADC.

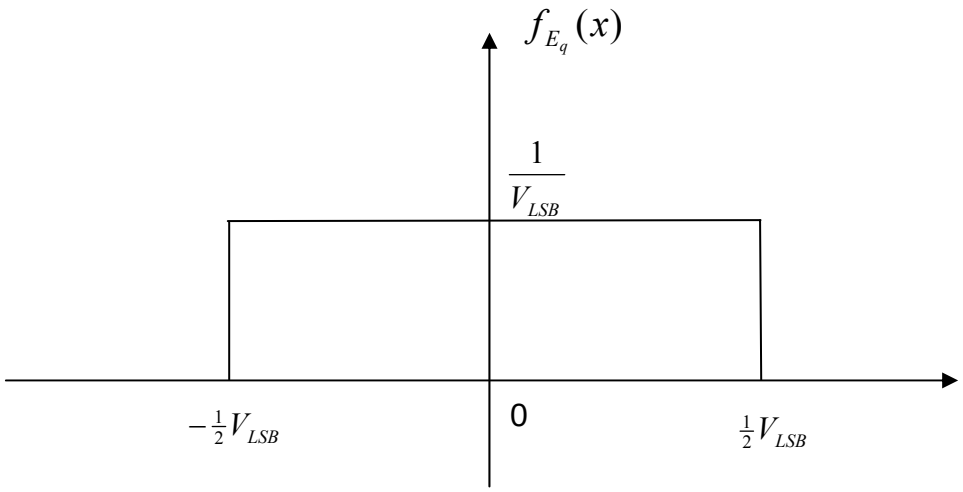

Figure 1.6 Assumed probability density function for the quantization error E_q

Because most ADC are tested by inputting a pure sinusoidal signal, a common SNR formula of the converters with a sinusoidal input can be derived as

$$SNR = 10\log\frac{P_S}{P_E} = 10\log\frac{V_{ref}^2/2}{V_{LSB}^2/12} = 10\log\left(\frac{3}{2}2^{2N}\right) = 6.02N + 1.76\,. \qquad (1.5)$$

Equation (1.5) reveals that each additional bit increases the SNR of the converter by 6 dB. Thus for a Nyquist rate converter to achieve a SNR of 98 dB(or 16bits) requires a 16-bit quantizer. This requirement is beyond the practical achievable accuracy for untrimmed monolithic circuits, since matching of one part in 65535 (0.0015%) element matching is required. As will be demonstrated, the methods employed in sigma-delta

modulation allow much higher SNRs to be achieved without high precision element matching.

1.2 Oversampled Converters

The previous section outlines the basic relationships between the number of bits of the converter and SNR for the Nyquist-rate converters. Although increasing the converter bits can reduce the power of the quantization error, the implementation imperfections such as component mismatches limit the SNR of Nyquist-rate converters.

To achieve high-resolution without requiring high precision analog components, oversampling techniques are often used. This relies on three techniques: oversampling of the input signal, quantization error shaping and digital filtering. The general topology of a sigma-delta ADC is shown in Figure 1.7. The core circuit of the ADC is a sigma-delta modulator, which acts as a high pass filter to filter the quantization error in the signal bandwidth. Because of the oversampling that makes the signal bandwidth much smaller than half of the sampling frequency, a digital decimation filter can be used to downsample and filter the modulated signal to the Nyquist bandwidth. A summary of the signal spectrum inside the sigma-delta ADC showing the spectrum change after anti-aliasing filtering, noise shaping, and digital filtering is also in Figure 1.7.

That the anti-aliasing filter in Figure 1.7 has a much wider transition band than that of Nyquist-rate converters in Figure 1.3 because the sampling frequency in the oversampled converters is much higher than the input signal bandwidth. Thus the design of the anti-aliasing filter for the oversampled converters becomes much easier.

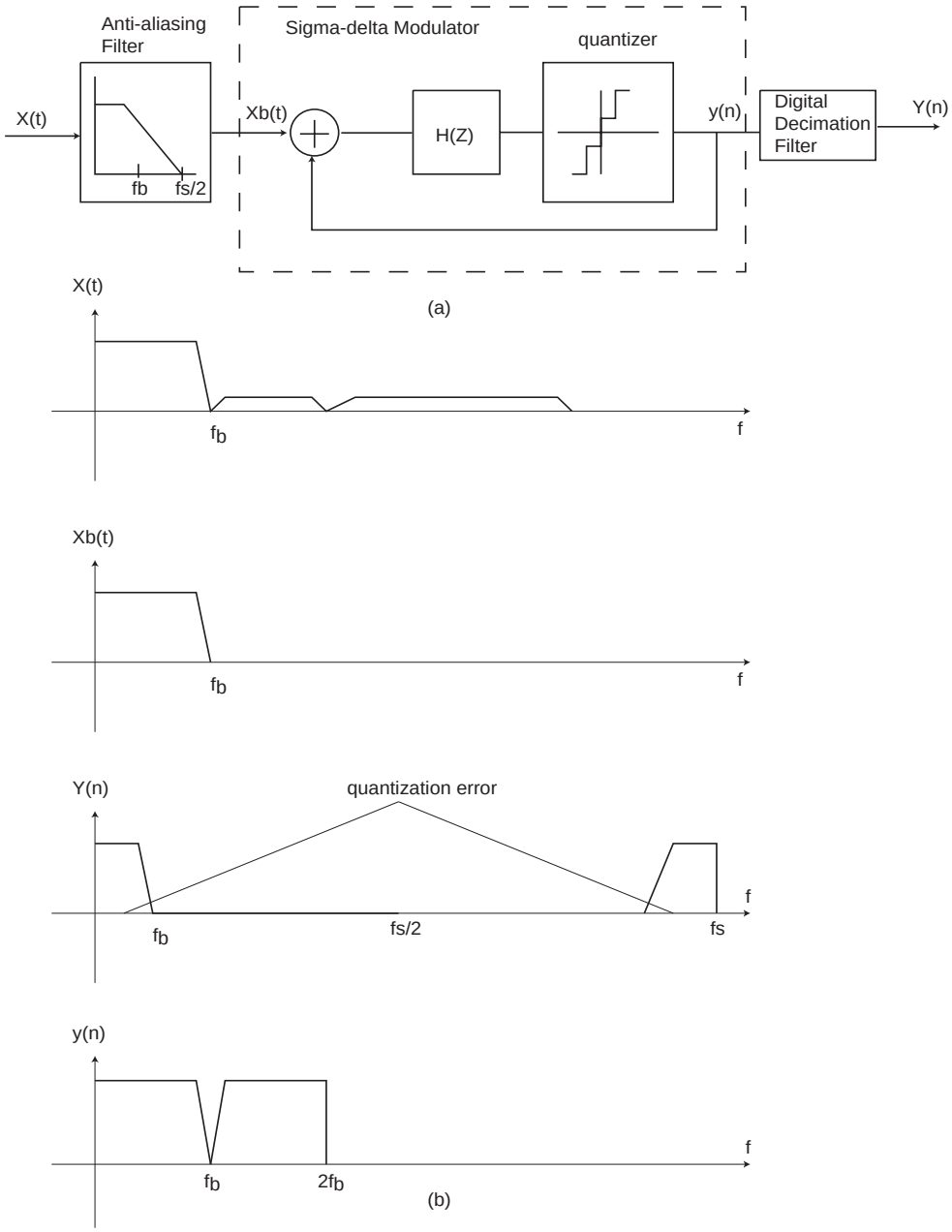

Figure 1.7 Sigma-delta ADC overview (a) block diagram (b) spectrum content

Even without noise shaping, oversampling can also help to increase the resolution of the ADC because it spreads the power of the quantization error over the sampling

bandwidth. To see the effect of oversampling on the SNR, we first define the oversampling ratio, OSR, as

$$OSR = \frac{f_s / 2}{f_b} = \frac{f_s}{2 f_b} \tag{1.6}$$

where f_s is the sampling frequency and f_b is the highest signal frequency. Because the quantization error is equally distributed over the sampling bandwidth without the noise shaping, an oversampling ratio of M means that the power of the quantization error in the signal band width is reduced by M. Thus the SNR of the ADC will increase M times and can be expressed as

$$SNR = 10 \log\left(\frac{3}{2} 2^{2N} OSR \right) = 10 \log(OSR) + 6.02N + 1.76 . \tag{1.7}$$

The above equation shows that 1-bit improvement in SNR requires a factor of four increase in OSR. To improve SNR by 4 bits, the OSR needs to be 256. This exponential relationship quickly reaches a practical implementation limit due to the speed of the quantizer. So the improvement of ADC resolution simply by increasing the oversampling alone is somewhat limited.

Further improvement in the resolution of the oversampled converter can be obtained using the sigma-delta modulator of Figure 1.7 so that the majority of the quantization error is moved out of the signal bandwidth. To characterize the performance of the sigma-delta modulator, both signal and noise transfer functions are developed.

The basic transfer function for the sigma-delta modulator can be easily developed using the linear model in Figure 1.8 where the quantizer error is modeled as an additive noise source similar to that shown in Fig. 1.4 and H(z) is the transfer function of the integrator. The feedback modulator is a linear, time-invariant system allowing

superposition for analysis of the input signal transfer function and the quantization noise transfer function.

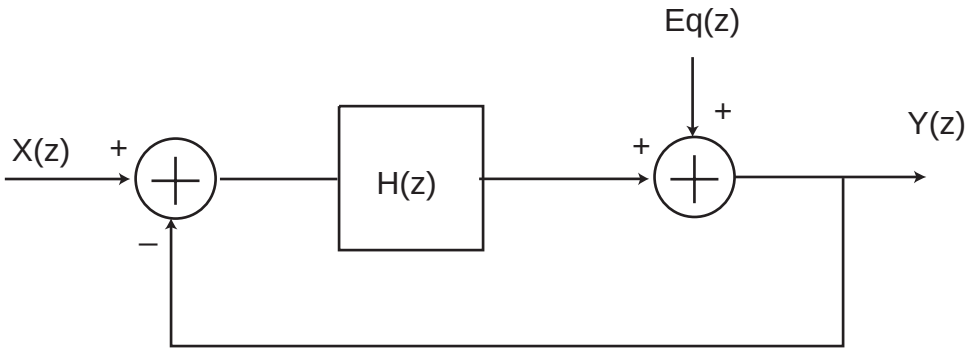

Figure 1.8 Signal Flow of the Sigma-Delta modulator

Assuming that the quantization noise is zero, the output signal, Y(z) can be determined as

$$(X(z)-Y(z))H(z)=Y(z). \tag{1.8}$$

Simplifying 1.8 leads to the signal transfer function that is

$$S_{TF}(z)=\frac{Y(z)}{X(z)}=\frac{H(z)}{1+H(z)}. \tag{1.9}$$

By assuming that the input signal is zero, in the same way, one can get the noise transfer function that is

$$N_{TF}(z)=\frac{Y(z)}{E_q(z)}=\frac{E_q(z)}{1+H(z)}. \tag{1.10}$$

Using superposition, the system output is the combination of the signal and noise transfer function, which can be written as

$$Y(z)=S_{TF}(z)X(z)+N_{TF}(z)E_q(z)=\frac{H(z)X(z)+E_q(z)}{1+H(z)}. \tag{1.11}$$

For first-order noise shaping when $H(z) = z^{-1}/(1-z^{-1})$, the modulator output is

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E_q(z). \tag{1.12}$$

We can see that the signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator. An analysis of the first-order sigma-delta modulator reveals that the quantization noise is given by [2]

$$P_E = \left(\frac{V_{LSB}^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{V_{LSB}^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3. \tag{1.13}$$

So the SNR of the sigma-delta ADC with first order noise shaping is

$$SNR = 10\log\left(\frac{P_s}{P_E}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{3}{\pi^2}(OSR)^3\right). \tag{1.14}$$

From the above equation, one can find that doubling the OSR gives an SNR improvement for a first-order modulator of 9 dB. However, for the system without noise shaping, the SNR improvement is only 3 dB.

The SNR expression for the oversampling sigma-delta A/D converter reveals a high resolution A/D converter can be obtained by oversampling the input signal and is not limited by the precision of the analog components.

1.3 Research Contributions

Several original contributions are made and documented in this dissertation to allow the inner quantization with a large number of bits in a single-stage ΣΔ modulator. Additionally, an experimental prototype has been fabricated with the TSMC 0.25um mixed-signal process to verify the design of a single stage ΣΔ modulator with 8-bit two-

step inner quantization. This section gives a brief summary and a detailed description of the contributions that will appear in the corresponding chapters.

1. *Two-step quantization.* Two-step inner quantization using traditional, power-efficient switched-capacitor circuits has been developed in a single-stage mulibit ΣΔ modulator by incorporating half-delay integrators, careful two-step ADC timing, and other architectural changes. The two-step quantization avoids the problem that the complexity of an internal flash ADC increases exponentially with each added bit. Because both the MSB and LSB signals produced by the two-step quantization are fed back simultaneously to all integrator stages, it is made suitable for low oversampling ratios. This part of research found in chapter 3 has been published in two conference papers [6,7].
2. *Segmented architecture with coarse/fine DAC and DEM*. A segmented architecture with coarse/fine Dynamic Element Matching (DEM) and DAC has been proposed to reduce the complexity of DEM and DAC due to the internal quantization with large number of bits. The consequence of the segmentation, mismatch between coarse and fine DACs can be noise-shaped by using a digital requantization (REQ) algorithm. A theoretic analysis of the REQ algorithm has been conducted to obtain the upper limit of the gain mismatch between coarse and fine DACs. Both behavior simulation and the circuit implementation demonstrated the effectiveness of the REQ algorithm. This part of research found in chapter 3 has been accepted in a journal paper [8].

3. *A new architecture of the ΣΔ modulator.* A new architecture of the second-order ΣΔ modulator illustrated in chapter 4 has been developed. This architecture uses the 8-bit two-step ADC for the inner quantization, achieving high resolution with a very low oversampling ratio. Two feed-forward branches are used to reduce the output swing of the integrators, therefore greatly relaxing the requirement on the DC gain of the opamp inside the integrators. A theoretic analysis of the feed-forward branches was performed to find the best gain of the branches.

4. *First reported ΣΔ modulator with 8-bit inner quantization*. An experimental prototype with the implementation of a single-stage ΣΔ modulator with 8-bit inner quantization has been fabricated with the TSMC 0.25um mixed-signal process. Chapter 5 describes the VLSI implementation of this prototype chip. It is the first reported single-stage ΣΔ modulator with 8-bit inner quantization. The REQ algorithm implemented in the system helped to decrease the noise floor in the signal band by 20 dB. The measured system achieved the dynamic range of 70 dB with an oversampling ratio of 16.

5. *A static adder circuit.* A static circuit with only switches and capacitors was developed to realize a short delay adder before the inner quantization. By adding two extra capacitors to the frond-end of the fully differential comparators, the short delay adder becomes the integral part of the flash quantizer, which firstly adds two signals together and then quantizes their sum. The static circuit adder has less power and chip area than that

implemented with the switched-capacitor circuit. The details of this circuit can be found in chapter 5.

1.4 Dissertation Outline

Conventionally, sigma-delta ADCs are used for low frequency applications due to the limit of the sampling frequency. One method of extending the signal bandwidth of a sigma-delta ADC is to appropriately trade internal quantization with oversampling ratio. This dissertation explores the possible benefits of applying the inner quantization with a large number of bits to a single stage sigma-delta modulator to reduce the oversampling ratio (OSR). Problems arising from this approach will be discussed in this dissertation. A prototype chip with 8-bit inner quantization was fabricated to demonstrate the performance of this approach. The dissertation is organized as follows.

In Chapter 2, the basics of the sigma-delta modulator are reviewed and several architectures are discussed along with their advantages and limitations.

In Chapter 3, the system architecture of a single-stage sigma-delta ADC with 8-bit two-step quantization is presented. Two problems encountered during the system design, the complexity of the quantizer and DACs are addressed and their respective solutions are presented.

In Chapter 4, the results of the behavior simulation are presented to determine the critical parameters of all sub-circuits of the system.

In Chapter 5, the detailed VLSI implementation of the system with the TSMC 0.25um mixed-signal process is presented with an emphasis on the switched-capacitor

integrator. The optimization of the circuit performance and the design of the digital circuit are also included.

In Chapter 6, the experimental prototype and the measurement results are presented along with the discussion of the key performance issues.

In Chapter 7, the contributions of the thesis are presented and further improvements of this project are proposed.

2 Sigma Delta ADC Fundamentals

The basic concept for the sigma-delta ADC is using the feedback to improve the effective resolution of a coarse inner quantizer. An early description of this concept was given in a patent by Culter [9]. His idea was to take a measurement of the quantization error in one sample and subtract it from the next input sample by using a delta modulator. Sigma-delta modulation employing noise shaping was proposed by Inose, Yasuda, and Murakami in 1962 [10] who added the loop filter to the frond end of a delta modulator and then move it inside the loop. Since the system contained a delta modulator and an integrator, it was named a delta-sigma modulator, where the "sigma" denoted the summation performed by the integrator. However, this technique was not widely used until the mid-1980s, because the use of a sigma-delta ADC required a digital decimation filter to digitally filter the high frequency noise, which was not realistic to build. With the development of VLSI technology, from mid-1980s, the sigma-delta converters have gradually become an area of great interest.

Based on the architecture, there are three types of sigma-delta modulators: single-stage modulators, cascade modulators and multibit modulators. Each type of modulator has both advantages and disadvantages. The following sections will provide an overview of these three types of modulators and compare their advantages and disadvantages.

2.1 Single Stage Modulators

A single loop sigma-delta modulator is the most straightforward architecture. Like the example of the first-order sigma-delta modulator in chapter 1, more integrators can be added to the feed-forward path of the modulator to increase the noise shaping order. Figure 2.1 shows the diagram of a second-order single-stage sigma-delta modulator. Compared with the first-order modulator, it has two integrators in the feed forward paths, which integrate the difference between the feed forward signal and the feedback signal from the output.

Let the gains of two integrators: a1, a2 equal 0.5 and 2 respectively, the signal and noise transfer function of the second-order modulator are given by

$$STF(z) = z^{-2} \tag{2.1}$$

and

$$NTF(z) = (1 - z^{-1})^2 . \tag{2.2}$$

The above equations show that the signal component at the output of the second-order modulator is simply a two clock cycle delay of the input signal while the noise component gets the second-order noise shaping.

From the noise transfer function of equation (2.2), one can also obtain the expression of SNR for a second-order modulator. The magnitude of the noise transfer function can be shown to be

$$\left|N_{TF}(f)\right| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{2.3}$$

leading to a quantization noise power over the signal bandwidth of

$$P_E = \frac{V_{LSB}^2 \pi^4}{60}\left(\frac{1}{OSR}\right)^5 . \tag{2.4}$$

Again assuming the input of the converter is the full scale sinusoidal signal, the maximum SNR for the second-order modulator becomes

$$SNR = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]. \tag{2.5}$$

We see here that doubling the OSR improves the SNR for the second-order modulator by 15 dB while for the first-order modulator the improvement is only 9 dB.

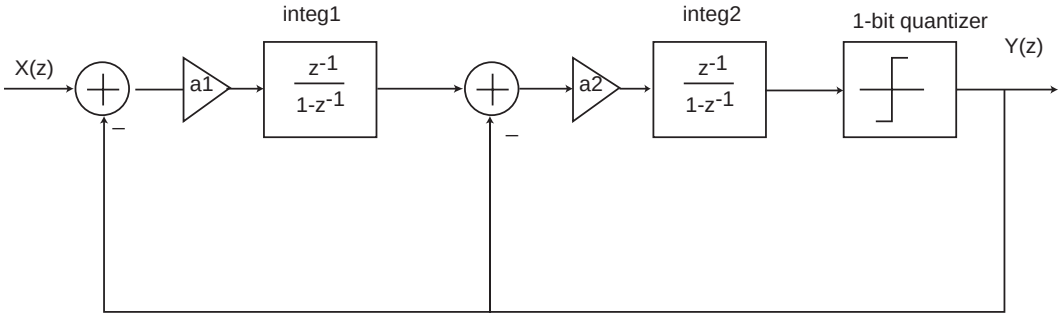

Figure 2.1 Block diagram of a second-order single-stage sigma-delta modulator

One can increase the modulator beyond second-order by including more integrators in the feed forward path as shown in Figure 2.2 where L integrators are used. Since the noise transfer function of an L-order modulator is

$$N_{TF}(z) = (1 - z^{-1})^L, \tag{2.6}$$

in the same way, one can get the maximum SNR for the L-th order modulator, which can be written as

$$SNR = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{(2L+1)}{\pi^{2L}}(OSR)^{2L+1}\right]. \tag{2.7}$$

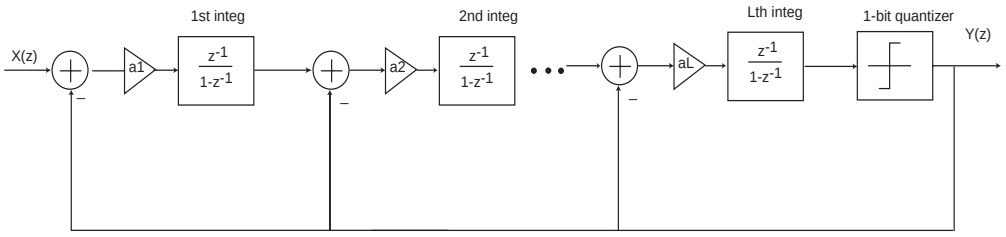

Figure 2.2 Block diagram of an Lth-order single-stage sigma-delta modulator

Although, it is convenient to use a high-order modulator to achieve high-order noise shaping, the high order (order >2) single-stage modulator has a problem in that the system becomes unstable due to the overload of the quantizer caused by the high gain of the noise transfer function. There are several different approaches to solve the problem of the instability while maintaining high-order noise shaping.

One approach to obtain a stable high-order single loop modulator is to scale down the gain coefficient of each integrator stage so that the highest gain of the noise transfer function can be controlled below 2 [11-14]. When the integrator gain is down-scaled, the modulator noise shaping is degraded from the standard shape form of $(1-z^{-1})^L$. As a result, a bigger OSR is needed to get the SNR predicted by equation (2.7). A systematic analysis of the tradeoff between the performance and integrator coefficients can be found in [3].

The other two approaches are either using cascade architecture or applying the multi-bit inner quantization to get the high-order noise shaping, which will be discussed in the following section.

2.2 Cascade Modulators

In cascade modulators, the combination of a first-order or second-order sigma-delta modulator is used to obtain higher-order noise shaping. Because each stage only has a 1st or 2nd order noise shaping, the whole system has no instability problem.

The quantization noise from each stage is fed as input into the following stage and the output of each stage is digitally filtered and a single output is obtained as the sum of the filter outputs. Proper selection of the filter stages results in cancellation of the quantization noise of each stage except the last. The final stage quantization noise is shaped to the order of the overall modulator, which is the sum of the order of every stage.

Figure 2.3 shows an example of cascade architecture, where a second-order modulator is followed by a first-order modulator. The quantization error of the first modulator stage is fed to the input of a second modulator. The signal transfer function and noise transfer function of the two modulators can be respectively written as:

$$Y1(z) = z^{-2}X(z) + (1-z^{-1})^2 Q1(z) \tag{2.8}$$

and

$$Y2(z) = z^{-1}Q1(z) + (1-z^{-1})Q2(z). \tag{2.9}$$

The digital outputs of two sigma-delta modulator stages, $Y1(z)$ and $Y2(z)$ are then processed with one clock cycle delay unit and second order differentiator unit respectively and finally pass through a subtractor to form the output of the system $Y(z)$. This output can be calculated as

$$Y(z) = z^{-1}Y1(z) - (1-z^{-1})^2 Y2(z) = z^{-3}X(z) - (1-z^{-1})^3 Q2(z). \tag{2.10}$$

Equation (2.10) indicates that a third-order noise shaping can be obtained by combining a second-order and a first-order modulator in cascade. Since no single stage is greater than 2nd order, the whole system achieving 3rd order noise shaping is stable.

This cascade approach can be extended to a higher-order simply by adding more first-order or second-order stages. For example, fourth-order noise shaping can be obtained by using two second-order stages (2-2 architecture).

Besides achieving high-order noise shaping without the problem of instability, the cascade architecture has another advantage over its single stage counterparts. For most single-stage modulator, the inner quantization is only 1-bit due to the nonlinearity of multibit DAC, which will be discussed in the next section. However, in cascade modulators, the multibit quantizer and DAC can be used in the last stage to increase the system resolution because the nonlinear errors of DACs are shaped by the sigma-delta modulator in the previous stage [16-19]. An example of a cascade modulator with multibit quanitzer can be found in [20].

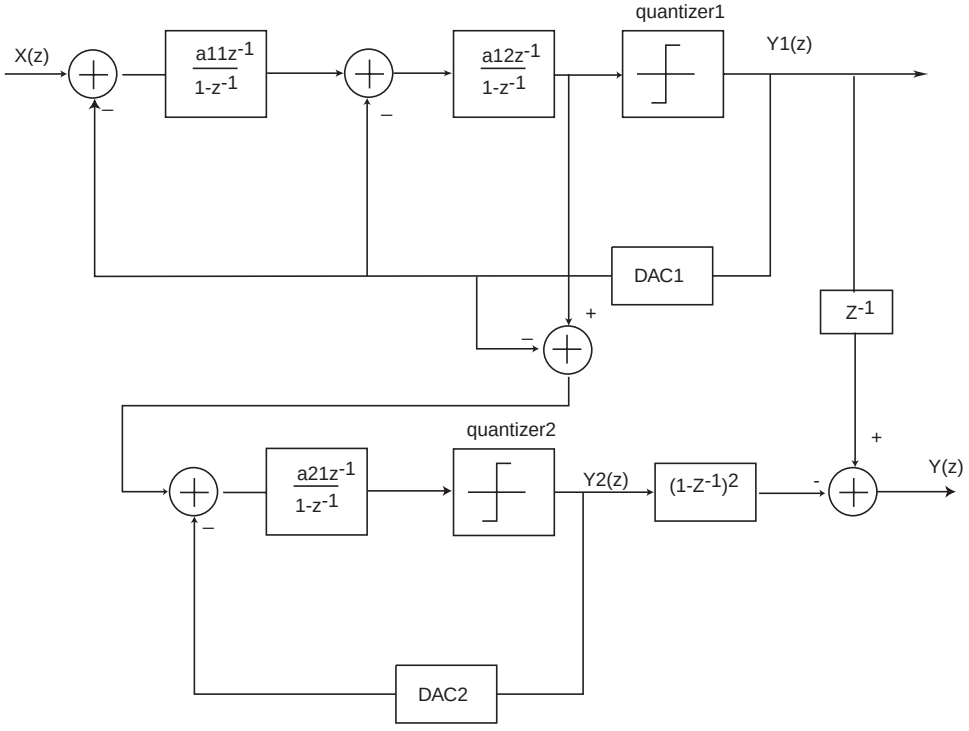

Figure 2.3 Block diagram of a third-order modulator in a cascade architecture

In cascade architecture, the limit on the increase of the noise shaping order is set by matching requirements. If the gains between the analog and digital paths do not match, the quantization noise in different single loops can not be cancelled effectively, and the quantization noise will leak through to the modulator output. As the order of the noise shaping in the cascade is increased, the constraints on this mismatch become more severe.

2.3 Multibit Modulators

One-bit noise shaping modulators have achieved popularity for use in integrated circuit data converters largely due to the fact that they employ 1-bit internal DAC that does not require precision component matching. However, as shown in equation 2.1, the resolution that a 1-bit sigma-delta modulator can achieve at a given oversampling ratio is limited. Although the achievable resolution increases with increasing single-stage order, these improvements rapidly diminish because of the problem of instability.

The primary advantage of multibit modulators is that the power of the quantization noise decreases dramatically and the SNR increases by 6 dB for each additional bit. Therefore, we can increase the overall resolution of any oversampled data converter without increasing the oversampling ratio, simply by increasing the number of levels in the internal data converters. This performance improvement in reducing the oversampling ratio while maintaining the resolution can be a significant advantage in high speed and high resolution application. The use of the multibit inner quantizers also facilitates the design of high-order single-stage modulators because the multibit quantizer is less likely to be overloaded than a 1-bit quantizer.

A big disadvantage of multibit modulators is that the multibit DAC inside the feedback path loses the excellent linearity as found in the one-bit DAC. Since the linearity of an oversampling converter is no better than the linearity of the DAC, the undesirable nonlinearity of the DAC directly limits the performance of the system [21, 22]. As the smallest component mismatch that can be achieved is on the order of 0.1-0.5% in an inexpensive CMOS IC fabrication process, the harmonic created by multibit modulators can approach -60 dB relative to the full-scale fundamental.

To deal with the nonlinarity problem of a multibit DAC, several circuit techniques from electronic trimming to digital corrections have been proposed. Because the digital correction technique called dynamic element matching (DEM) is the most popular method, the following section will focus on the introduction of the DEM method.

DEM is designed to convert a DC error into a wide-bandwidth noise by choosing different elements to represent a digital input code K at different times. In short, the DEM technique does not eliminate errors but spreads the power of errors over a wide-bandwidth. Four possible approaches are listed below to implement the DEM technique.

- Random Dynamic Averaging (RDA)
- Data Weighted Averaging (DWA)
- Individual Level Averaging (ILA)
- Clock Level Averaging (CLA)

For practical purposes, ILA and DWA are performed for the matching of the DAC. Figure 2.4 shows an example where DEM is used in the system. Before the feedback signal is fed to the DAC, the DEM block controls the elements to be chosen for the DAC operation.

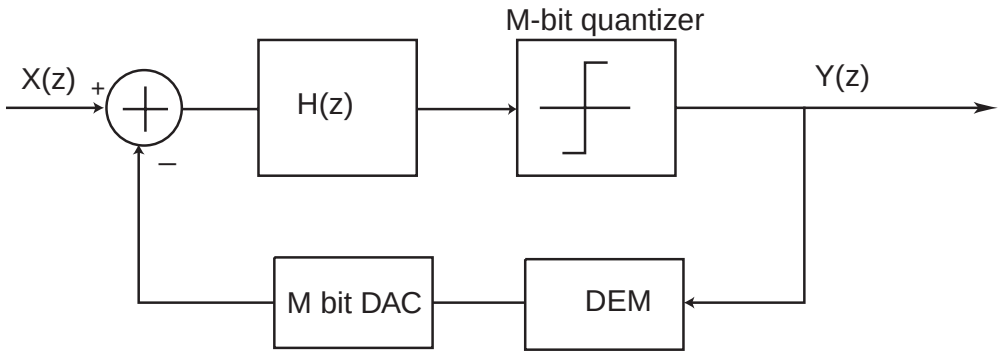

Figure 2.4 A multibit sigma-delta modulator with dynamic element matching(DEM)

The goal of the individual level averaging algorithm is to improve the SNR in the signal band while avoiding the generation of tones. The basic idea of individual level averaging is to guarantee that each element is used with equal probability for each digital input code [23, 24]. In order to use this algorithm, each output level has its own pointer to remember the position of the last elements. For a certain digital input code, the ILA block first finds the pointer for the input. Once the pointer is known, the Rotation block will select a certain number of elements starting from the pointer. For example, a 4-bit DAC has 15 elements. If the input code is 4, the ILA block first finds a pointer associated with the input code 4. If that pointer is 2, the rotation block then selects the elements numbered from 3 to 7 and updates the pointer from 2 to 6. Figure 2.5 shows the diagram of the ILA block. In summary, the ILA algorithm decides which elements are used for a specific digital code each time in such way that each element is equally used no matter what the input code is.

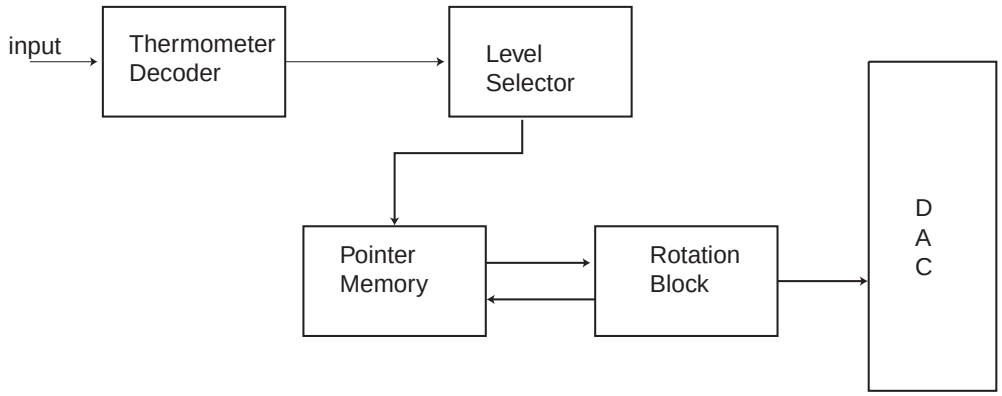

Figure 2.5 Block diagram of the individual level averaging (ILA) block

Although the ILA can remove most harmonics of the DAC nonlinearity and spread out the noise widely in the Nyquist band, it increases the design complexity in the digital circuit due to the needs of storing the pointers for all the different quantization levels. The data weighted averaging (DWA) method, in contrast is much simpler than ILA only requiring one pointer for all the quantization levels.

Unlike ILA, DWA modulates the nonlinearity error around the subharmoinics of the sampling clock frequency by making the mismatch noise a periodic signal instead of making the mismatch noise white [25, 26, 27]. This method keeps track of the last element used in the previous code, and uses the next group of elements sequentially. Figure 2.6 demonstrates how the DWA algorithm works in a 4-bit DAC with fifteen unit elements. For the first input code of "2", the algorithm chooses the first two unit elements if the initial pointer position is 0. Then it would choose the elements from 3 to 5 and elements from 6 to 10 for two consecutive input codes, "3" and "5". Finally it would choose the last five elements and the first element for last input code of "6". The pointer in the DWA block always points to the position of the last elements used in the previous code.

Although the DWA method can not remove the harmonic distortion of the DAC as well as the ILA method, it modulates the nonlinarity of the DAC, moving the harmonic distortion out of the signal bandwidth, which can be removed by the digital filter in the following stage.

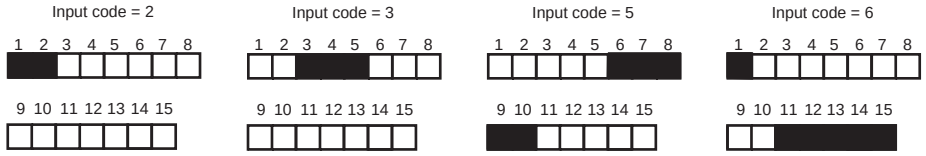

Figure 2.6 Graphical Explanation of DEM Operation

The block diagram of the DWA method can be found in Figure 2.7 where the binary input signal controls the update of the pointer while the thermometer code of the input determine which elements are chosen based on the position of the pointer. Instead of having pointers for every quantization level as illustrated in the ILA block, the DWA block only has one pointer updated with the input digital code, thus greatly reducing the complexity of the digital circuit.

2.4 Conclusion

The tradeoffs involved in achieving high resolution in sigma-delta ADCs usually lead to low internal quantization levels and high oversampling rates. However, in order to achieve both high resolution and high speed, the oversampling ratio (OSR) must be reduced, which requires an increase in the noise shaping order or the inner quantization levels.

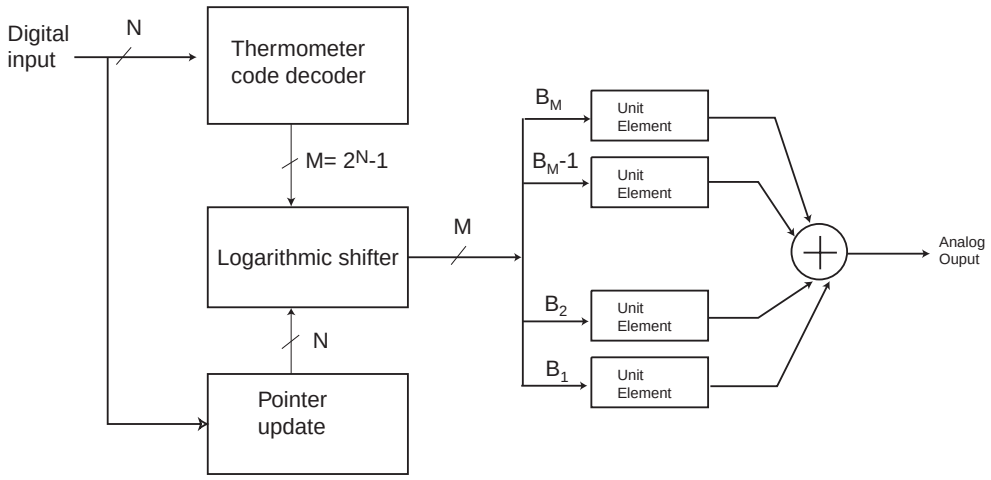

Figure 2.7 Block diagram of the data weighted averaging (DWA) method

New DEM algorithms make it possible to use multibit inner quantization inside the single-stage sigma-delta modulator in spite of the nonlinearity of the analog DAC. However, there is a limit on increasing the quantization levels of the multibit sigma-delta modulator. The limit is imposed by the exponential increase of the complexity of the DAC, DEM, and inner quantizer with each additional bit of internal quantization. To further push the limit of the quantization bits of the inner quantizer, the next chapter will discuss a new system architecture, which solves the problem of the exponential increase in the complexity.

3 Inner Quantization with Large Number of Bits

3.1 Introduction

The multibit delta-sigma modulator has become a popular architecture for implementing high-resolution ADCs for digital communications [28][29]. Due to the introduction of efficient dynamic element matching (DEM) techniques [23], single-stage multibit modulators have also gained interest. They offer a potentially low-power solution because of their relative insensitivity to integrator inaccuracies.

Most single-stage multibit modulators use a low number of bits (six or less) for internal quantization [28,30]. Each additional quantizer bit improves overall SNR by 6 dB and also improves modulator stability, which permits more aggressive noise shaping. However, power dissipation quickly becomes unmanageable because of the exponential increase in complexity of the internal flash ADC, the DEM circuitry, and the capacitive DACs. Figure 3.1 shows the schematic of a flash ADC in which 2^N-1 comparators are needed to distinguish 2^N quantization levels. So for the 8-bit flash ADC, the total number of the comparators is 255.

The two-step flash quantizer architecture can potentially solve this problem, but the latency of a two-step system normally causes modulator instability. Some attempts at solving this problem have been made, but with limited success. Lindfors [46] proposes an

architecture with two-step quantization in which the coarse quantization noise can be removed by using digital noise cancellation. Another attempt at internal multi-step quantization is proposed in [30]. However, both methods need digital filtering and recombination to cancel coarse ADC quantization noise, which again are subject to noise leakage and the nonidealities of analog circuits.

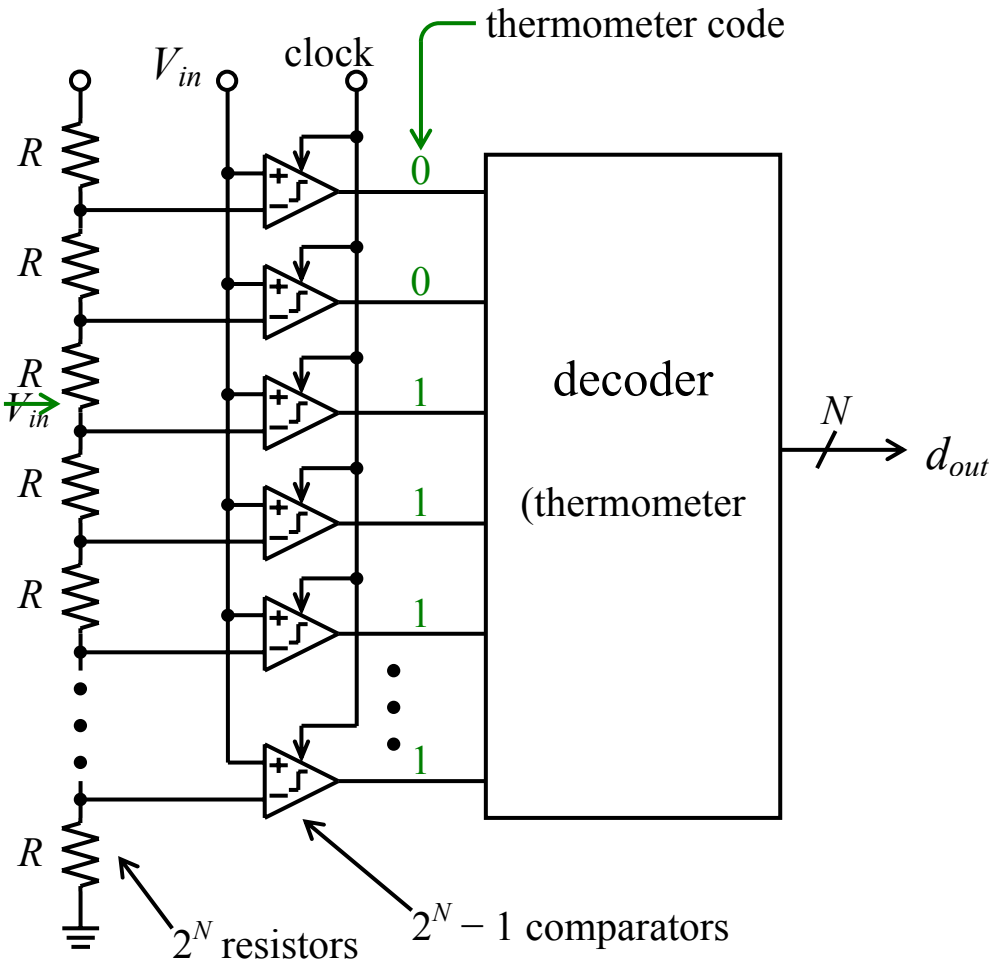

Figure 3.1 Block diagram of the flash ADC

To solve this problem, new single-stage modulator architecture with two-step quantization is described. The effectiveness of the two-step quantization is not restricted by quantization noise leakage. A segmented DEM/DAC system with digital requantization is proposed to accommodate the high level of quantization achieved with two-step coarse/fine quantizers. The mismatch between two segmented DACs can be filtered by using a noise-shaped requantization.

3.2 Two-step Quantization

Performing two-step quantization within a single-stage modulator is challenging because only one-half clock cycle quantizer delay is permitted for stability reasons. Figure 3.2 shows a diagram of the quantizer (ADC block) and last integrator of a typical single-stage multibit sigma-delta ADC. The system is controlled by two non-overlapping clocks P1 and P2, shown in Figure 3.3. The parasitic-insensitive integrator of Figure 3.2 samples the input when P1 is high and updates its output (V_a of Figs. 3.1 and 3.2) when P2 is high. Figure 3.3 shows the total processing time, $t_a + t_b + t_c$, allowed for both quantizer and dynamic element matching (DEM) block. t_b corresponds to the pulse width of the clock P1, while t_a and t_c represent the "dead zones," when both P1 and P2 are low. DEM outputs d_j must assume their logical values before the next integration phase, or before the end of time t_c. With little more than half a clock cycle to accomplish A/D conversion and DEM, it appears that only a flash quantizer can be used in the traditional multibit modulator architecture.

The proposed architecture permits two-step A/D conversion by employing the following two techniques. First, the conversion time of a two-step quantizer is

compressed by utilizing the dead zone between the two non-overlapping clocks. Second, half-delay integrator stages are used to permit additional delay in the feedback path to all integrators except the last.

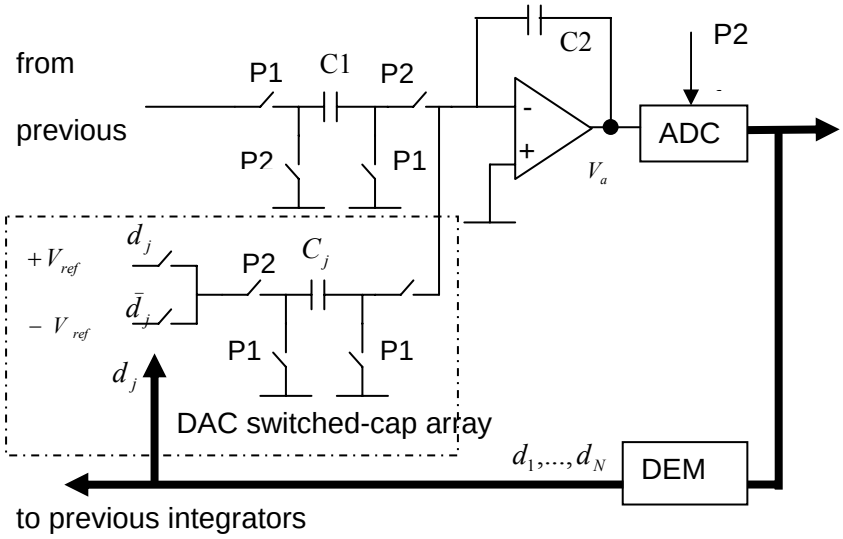

Figure 3.2 Block diagram of the quantizer and last integrator in a typical single-stage multibit sigma-delta modulator

By using the special timing, the overall delay of a two-step quantizer can be compressed to half a clock cycle. Figure 3.4 shows a diagram of a two-step quantizer, where the two-step operations have been allocated to time slots t_a, t_b and t_c corresponding to Figure 3.3. At the beginning of time t_a, the last integrator has just finished integrating and is driving ADC1, the coarse flash ADC. At the falling edge of clock P2, the latches of ADC1 begin to regenerate, and at the end of t_a, the conversion is complete. During t_b when P1 is high, the op-amp based DAC and subtractor, similar in appearance to the DAC/integrator stage of Figure 3.2, has time to settle. At the beginning of time slot t_c, the output of the subtractor is available and ADC2, the fine flash ADC, is strobed as P1

falls. If the fine flash latches can regenerate during t_c, both coarse and fine bits are available at the beginning of P2 for the integrator of Figure 3.2.

Although the conversion time of the comparator is much longer than the dead zone(t_a, t_b), the time required for the preamplifier in the comparator is overlapped with the settling time of either the last integrator or subtractor, resulting in no additional delay in the signal path. So the only extra delay imposed by the comparators is the regeneration time of the latch. Circuit simulation of the two-stage regenerative latch in [31] shows that the latch settling time in 0.18-um CMOS technology is under 1 ns. Thus for typical clock rates, the dead zone requirement does not reduce significantly the settling time of the two-step ADC subtractor or the last integrator. The pulse width t_b is determined by the speed of the subtractor, which is restrained by the power budget. However, the subractor does not require high settling accuracy because its errors are noise-shaped by the modulator.

For the flash quantizer inside a common ΣΔ modulator, comparator offsets usually need to be less than 0.5 LSB. However, the simulation result in Fig. 3.4 shows that the maximum allowable offset of the fine ADC is 0.25 LSB doubling the precision of the coarse ADC.

Because of capacitor mismatch, DAC noise will seriously degrade the system performance if it is not shaped by DEM. To allow processing time for DEM, additional delay can be added in the feedback path if half-delay integrators are used as shown in Figure 3.6. Half-delay integrators sample on one clock phase and update their outputs on the next, with the following stage sampling this output at the end of the update phase. The

half-clock delay added to the feedback path makes it possible to apply DEM to shape the first-stage DAC noise digitally.

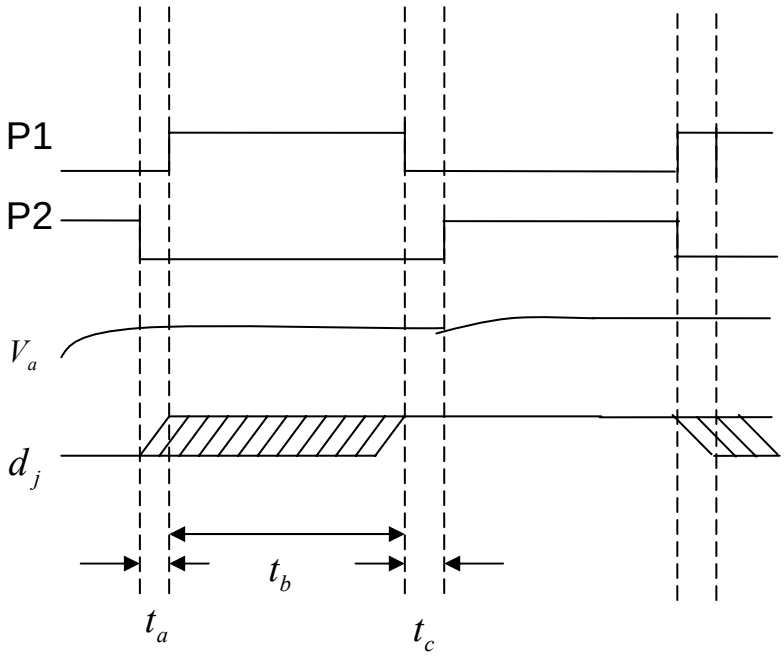

Figure 3.3 Timing diagram for Figure 3.2

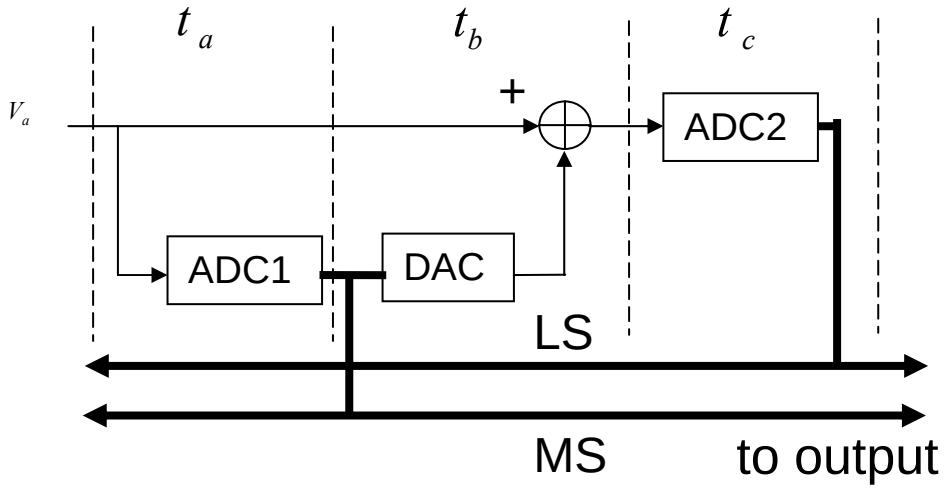

Figure 3.4 Two-step quantizer with time slot allocation

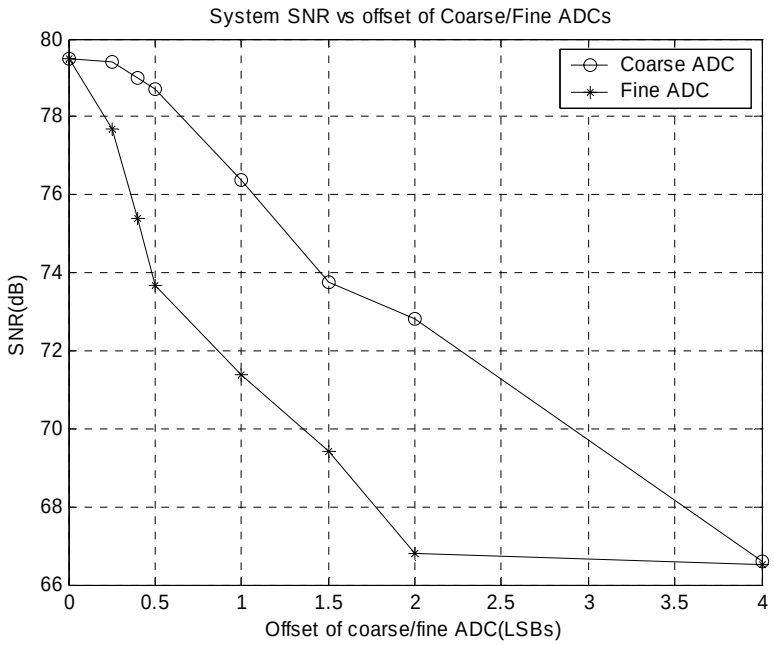

Figure 3.5 The system SNR in a second-order ΣΔ modulator versus the offset of coarse/fine ADCs inside an eight bit two-step quantizer

Even though two half-delay integrators are applied in the system of Figure 3.6, it has the same form of signal/noise transfer function as a standard second-order modulator because both the two-step ADC and the DEM block have half a clock delay.

Since the feedback loop of the last integrator only allows for one clock cycle delay, the DEM has to be removed from the loop. Although the DAC mismatch noise at the input of the last integrator is not digitally shaped, the gain of previous integrators shapes its spectrum, preventing it from dominating in-band noise.

3.3 Noise Shaped Requantization

Similar to using two-step quantization to reduce the number of comparators in the flash ADC, one can use the segmented DACs(coarse/fine DACs) to greatly reduce the

number of unit elements in the DAC, as illustrated in Figure 3.7. Due to the mismatch of the analog components, this segmented architecture is subject to the leakage of the coarse quantization noise.

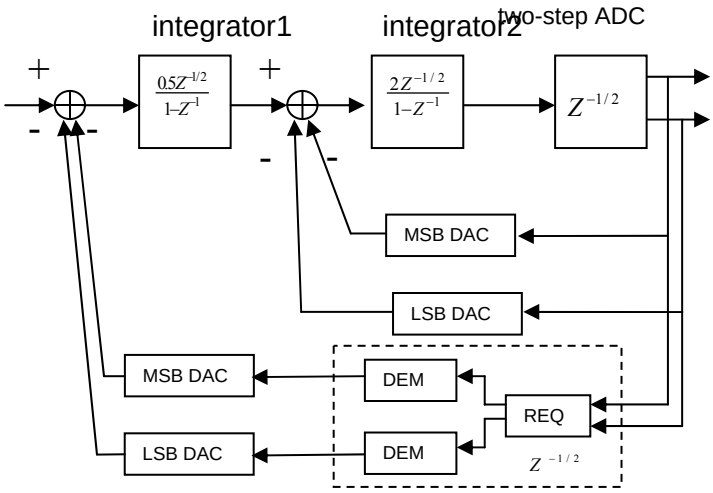

Figure 3.6 Example 2nd-order sigma-delta modulator with two-step quantizer

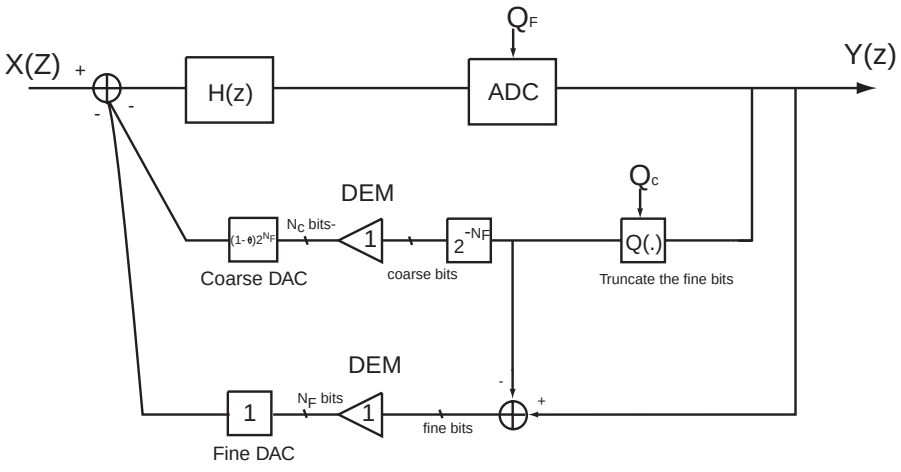

Figure 3.7 Block diagram of ΣΔ ADC with the segmented DAC

In order to reduce the leakage coarse quantization noise, a noise-shaped requantization (REQ) method is introduced here. This method was originally proposed in [32] for a ΣΔ DAC, however, in this chapter this concept is extended to ΣΔ ADCs.

In Figure 3.7, N_C and N_F are the number of coarse and fine bits respectively and Q_C and Q_F are the coarse and fine quantization noise respectively. To obtain the coarse bits from the digital output, all the fine bits are truncated after passing a simple digital quantizer, introducing the coarse quantization noise to the feedback loop. This high level of noise should be cancelled when coarse and fine DACs are summed at the input of the modulator. The output of the quantizer is then divided by 2^{NF} to represent the binary right shift by N_F; this is because the coarse output is the N_C most significant bits of an N-bit digital output. To compensate for this binary right shift, the gain of the coarse DAC should be 2^{NF} times that of the fine DAC. However, any mismatch between coarse and fine DAC will change this fixed ratio from its ideal value, noted as gain mismatch error, 1-θ in Figure 3.7. Although the mismatch noise inside each individual DAC can be filtered by two independent DEM circuits shown in Figure 3.7, part of the coarse quantization noise caused by the DAC gain mismatch directly leaks into the system output with no noise shaping, as will be shown below.

It can be found from the output of system, which is given by

$$Y(z) = \frac{X(z)H(z)}{1+(1-\theta)H(z)} + \frac{Q_F}{1+(1-\theta)H(z)} + \frac{\theta Q_C H(z)}{1+(1-\theta)H(z)} \quad (3.1)$$

The last term in equation 3.1 is the leakage component, which vanishes as $\theta \rightarrow 0$. To prevent the leakage noise from dominating the output, the power of the leakage noise should be less than that of the fine quantization noise. This relation can be expressed as:

$$P_{Q_C} < P_{Q_F} \tag{3.2}$$

where P_{QC} and P_{QF} represent the power of the coarse leakage noise and fine quantization noise respectively. Since the coarse leakage noise has no noise shaping and fine quantization noise gets second-order noise shaping in a typical second-order ΣΔ modulator, their powers are given as:

$$P_{Q_C} = \frac{\theta^2 2^{-2N_C}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{2f_0}{f_s} \tag{3.3}$$

and

$$P_{Q_F} = \int_{-f_0}^{f_0} \frac{2^{-2(N_c+N_F)}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{1}{f_s} \left[2\sin(\tfrac{\pi f}{f_s})\right]^4 df \,. \tag{3.4}$$

where V_{ref} stands for the reference voltage of the inner quantizer and $N_{C,}$ N_F is the number of coarse and fine quantization bits respectively. f_0 is the highest signal frequency and f_s is the sampling clock rate.

Combining equation (3.2)-(3.4), one can get the condition for the coarse quantization noise leakage in a second-order ΣΔ modulator, which is given by

$$\frac{\theta^2 2^{-2N_C}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{2f_0}{f_s} < \int_{-f_0}^{f_0} \frac{2^{-2(N_C+N_F)}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{1}{f_s} \left[2\sin(\tfrac{\pi f}{f_s})\right]^4 df \,. \tag{3.5}$$

Assuming that the signal band is much lower than half of the sampling frequency, we may approximate equation (3.5) by

$$\frac{\theta^2 2^{-2N_C}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{2f_0}{f_s} < \int_{-f_0}^{f_0} \frac{2^{-2(N_C+N_F)}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{1}{f_s} \left(\frac{2\pi f}{f_s}\right)^4 df = \frac{2^{-2(N_C+N_F)}}{60} \mathrm{V}_{\mathrm{ref}}^2 \pi^4 \left(\frac{2f_0}{f_s}\right)^5 \,. \tag{3.6}$$

Simplifying equation (3.6) leads to

$$\theta < \frac{2^{-N_F}}{\sqrt{5}}\pi^2\left(\frac{2f_0}{f_s}\right)^2 = \frac{2^{-N_F}}{\sqrt{5}}\pi^2\left(\frac{1}{\mathrm{OSR}}\right)^2. \tag{3.7}$$

From equation 3.7, one can see that even for a moderate oversampling ratio of 16, the maximum allowable gain mismatch between the coarse and fine DAC in a second order ΣΔ modulator with 4+4 inner quantizer is 0.1%, which is not easy to achieve.

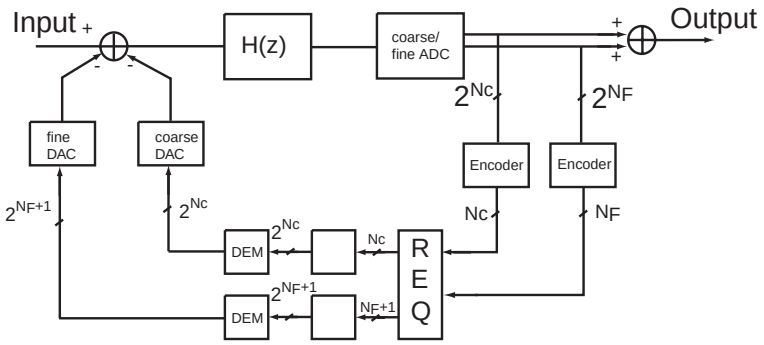

Figure 3.8 Block diagram of ΣΔ ADC with a first-order requantization block

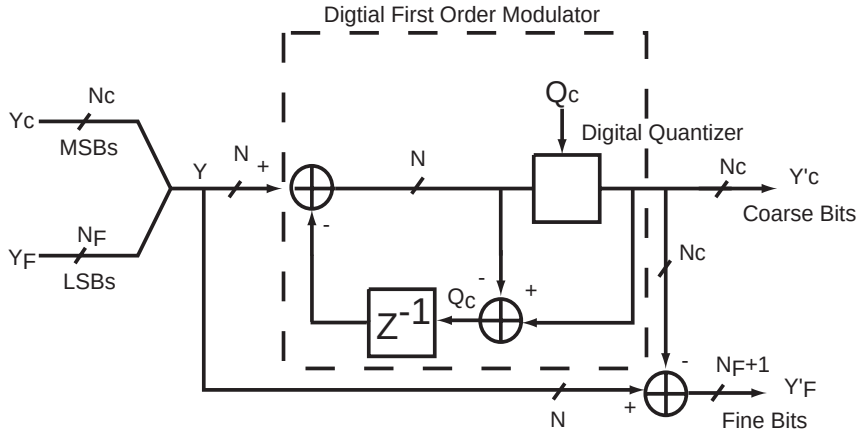

Figure 3.9 Expanded View of REQ Block

In a ΣΔ ADC with two-step quantization, the MSB and LSB signals can be combined and requantized using a first-order digital ΣΔ modulator as shown in Fig. 3.7 and Figure 3.9. Referring to Figure 3.8, the digital coarse and fine signals from the quantizer are first concatenated to form an N-bit signal. This signal is then requantizd to N_C bits using a digital first-order modulator. The coarse signal is then subtracted from the original N-bit signal to form a new fine signal with N_F+1 bits. After requantization, the new coarse and fine signals are:

$$Y_C^{'}(z) = Y(z) + Q_C(1 - z^{-1}) \tag{3.8}$$

and

$$Y_F^{'}(z) = -Q_C(1 - z^{-1}). \tag{3.9}$$

Signals $Y_C^{'}$ and $Y_F^{'}$ then pass through the independent DEM blocks and DACs and are summed at the input of the modulator. The effectiveness of the REQ block can be seen in Figure 3.10 where inside the REQ block the coarse quantization noise gets first-order noise shaping before passing to the next stage. When the new coarse and fine signals are summed at the input of the modulator, the leakage noise component due to the DAC gain mismatch gets first-order noise shaping. This is manifested in the expression of the system output, which is given by

$$Y(z) = \frac{X(z)H(z)}{1 + (1-\theta)H(z)} + \frac{Q_F}{1 + (1-\theta)H(z)} + \frac{\theta Q_C(1 - z^{-1})H(z)}{1 + (1-\theta)H(z)}. \tag{3.10}$$

The last term of equation (3.10) is the leakage coarse quantization noise with first-order noise shaping.

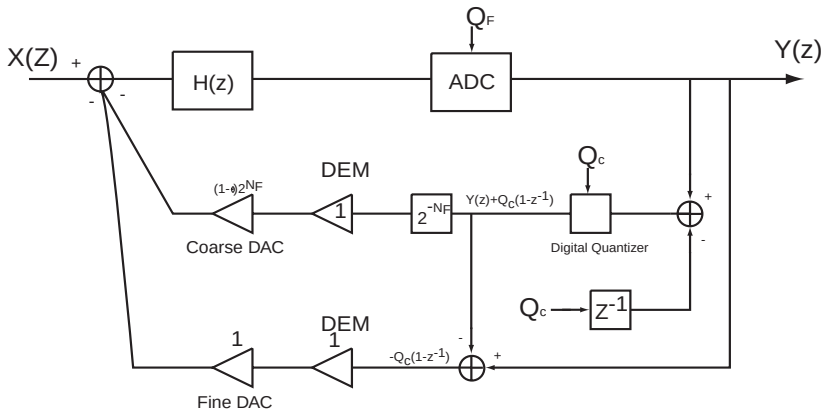

Figure 3.10 The signal flow graph of a ΣΔ ADC with a first-order requantization block

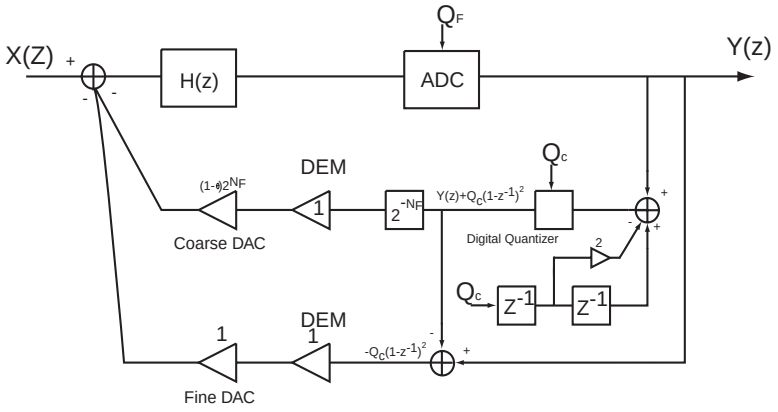

Figure 3.11 The signal flow graph of a ΣΔ ADC with a second-order requantization block

The above first-order requantization can be extended to high-order at the expense of the complexity of fine DAC and DEM. Figure 3.11 shows the signal flow graph of a ΣΔ ADC with a second-order requantization block where coarse quantization noise gets second-order noise shaping. The system output in Figure 3.11 can be written as

$$Y(z) = \frac{X(z)H(z)}{1+(1-\theta)H(z)} + \frac{\mathrm{Q_F}}{1+(1-\theta)H(z)} + \frac{\theta Q_C (1-z^{-1})^2 H(z)}{1+(1-\theta)H(z)} \quad . \tag{3.11}$$

Although the leakage coarse quantization noise can be greatly suppressed by using second-order requantization, the complexity of the fine DEM and DAC increases four times.

Since the leakage coarse quantization noise is shaped by the REQ block, the stringent requirement on the DAC gain mismatch can be greatly relaxed. As shown in equation (3.2), the power of leakage coarse quantization noise should be less than that of fine quantization noise. And their relative powers in a second-order ΣΔ modulator with a first-order requantization are found to be

$$P_{Q_C} = \int_{-f_0}^{f_0} \frac{\theta^2 2^{-2N_C}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{1}{f_s} \left(2 \sin \tfrac{\pi f}{f_s}\right)^2 df \tag{3.12}$$

and

$$P_{Q_F} = \int_{-f_0}^{f_0} \frac{2^{-2(N_c+N_F)}}{12} \mathrm{V}_{\mathrm{ref}}^2 \frac{1}{f_s} \left(2 \sin \tfrac{\pi f}{f_s}\right)^4 df \,. \tag{3.13}$$

Combining equation 3.2, 3.12 and 3.13 and assuming $f_0 << f_s$, the new condition for the DAC gain mismatch can be written as

$$\theta < 2^{-N_F} \pi \sqrt{\frac{3}{5}} \left(\frac{1}{\mathrm{OSR}}\right). \tag{3.14}$$

For an OSR of 16 and fine bits N_F of 4, the maximum allowable DAC gain mismatch is 0.95%, which is nearly ten times bigger than that without noise shaping.

The effectiveness of the REQ block can also be seen in the behavioral simulation results shown in Figure 3.12 and Figure 3.13. By comparing the spectrum and SNR of a second-order ΣΔ modulator with the same DAC gain mismatch and different order noise shaping of REQ, the simulation shows that the REQ block can greatly lower the quantization noise floor and increase the system SNR especially in the case of high oversampling ratio.

Although the REQ method can greatly relax the stringent requirement on gain mismatch between coarse and fine DAC, it contains several minor drawbacks. As the REQ order increases, more additional bits are needed for the fine DAC and DEM because the signal range of the new fine bits increases exponentially with the noise shaping order. Another potential drawback is a slight reduction in the input signal range due to the possible overflow of the REQ circuitry. This is because the REQ circuitry uses a fixed-point number to represent the signal. For the second-order system simulated, no overflow occurs if the input is limited to 90% of full scale.

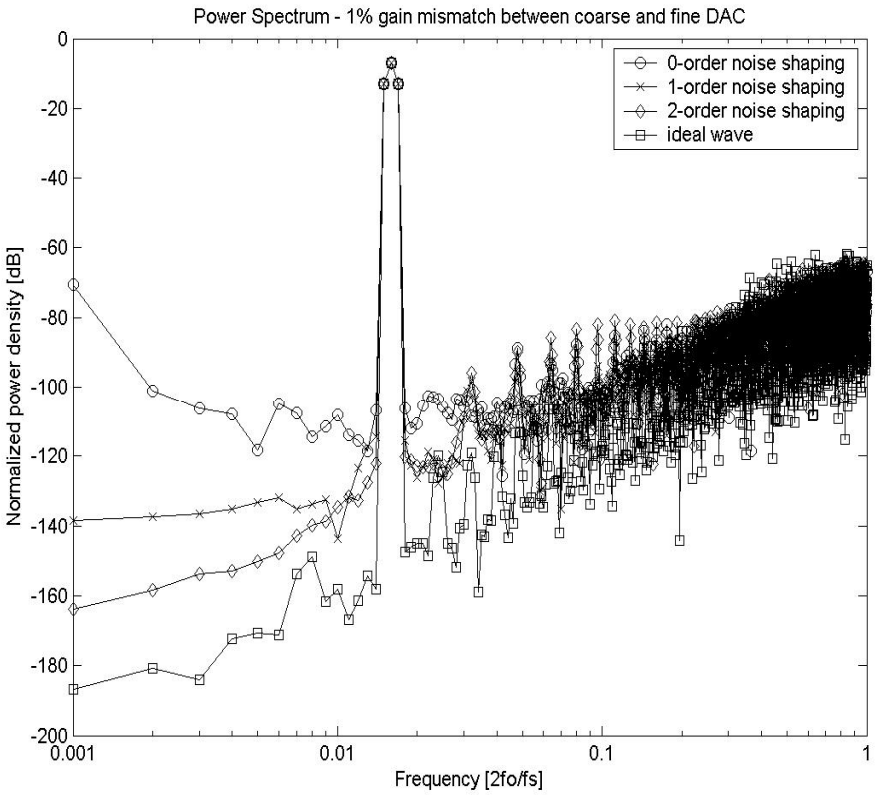

Figure 3.12 The simulated spectrums with different REQ orders in a second-order ΣΔ modulator with 4+4 bit two-step quantization.

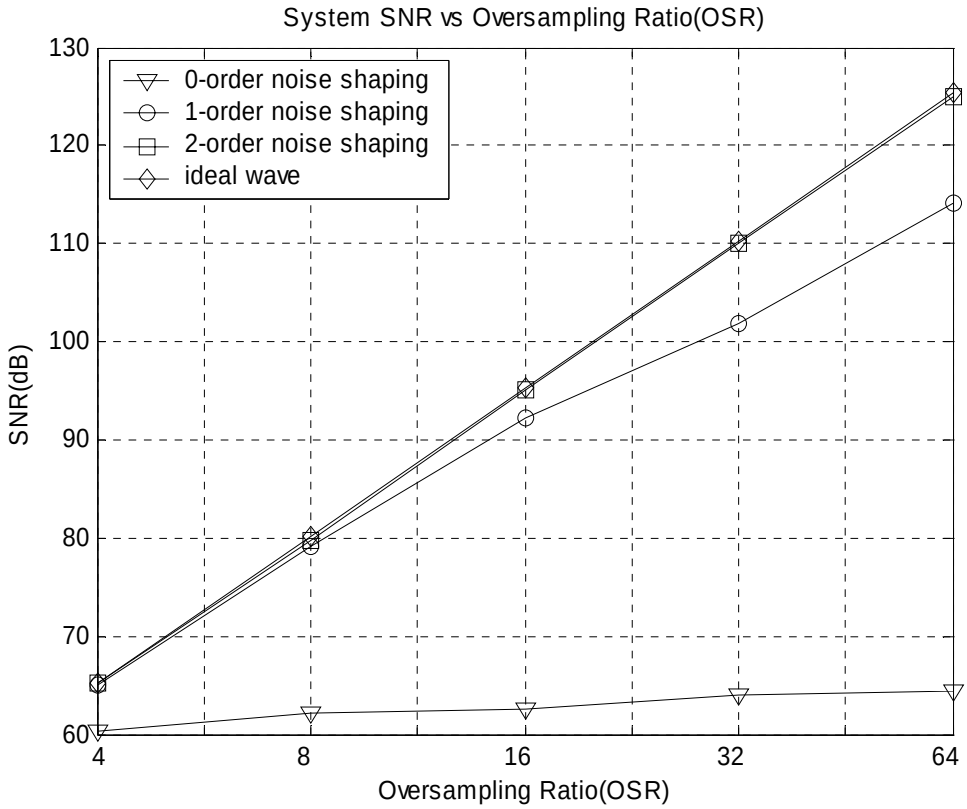

Figure 3.13 The simulated system SNR versus oversampling ratio under different REQ orders

3.4 Conclusion

The exponential increase in the complexity of the flash ADC, DEM and DAC circuitry with each added quantizer bit limits the internal resolution of a single-stage multibit ΣΔ modulator. Two techniques have been proposed to resolve this dilemma. By incorporating half-delay integrators, careful two-step ADC timing, and other architectural changes, two-step quantization becomes feasible in a single-stage multibit ΣΔ modulator using traditional, power-efficient switched-capacitor circuits. Coarse/fine segmentation combined with an REQ block allows for larger internal quantization without the

exponential increase in complexity of DEM and DAC circuitry, while still maintaining performance close to the alternative non-segmented system.

Although the two-step inner quantization with a moderate number of bits increases the complexity of the digital circuitry, this burden can be substantially reduced as CMOS technologies continue to scale.

4 Architecture and Behavior Simulation

In general, there are three primary degrees of freedom associated with the architecture selection for sigma-delta modulators: oversampling ratio, noise shaping order, and inner quantization bits. For the high-speed and high resolution sigma-delta modulator, the oversampling ratio must fall below the range of 64-512 typically used in low and medium speed oversampling converters [28, 30]. To offset the resolution loss caused by the decreased oversampling ratio, either noise shaping order or inner quantization bits must increase.

Although cascade architectures can easily increase noise shaping without the problem of instability, they are subject to noise leakage and the nonidealities of analog circuits. So increasing the inner quantization bits becomes a reasonable alternative to realize a high speed and high resolution modulator even though this introduces nonlinearity due to the multibit DAC.

Chapter 3 shows that it is possible to build a single-stage modulator with a large inner quanitzer (above 6 bits) so that the oversampling ratio can be reduced to 8 or 16. To demonstrate that the novel architecture in chapter 3 can achieve high resolution (SNR > 70 dB) with very low oversampling ratio, a proposed high-speed, high resolution single-stage sigma-delta modulator with 8-bit inner quantization is implemented in the TSMC 0.25um mixed-signal process. The following section will introduce the architecture of the

proposed modulator and show how to find the critical design parameter using the behavior simulation.

4.1 System Architecture

The proposed system architecture shown in Figure 4.1 extends the example of the second-order single-stage architecture in Figure 3.6. Based on two techniques discussed in chapter 3, a special 8-bit two-step ADC with only half a clock delay is chosen as the inner quantizer for the system. To reduce the complexity of DEM and the DAC, a segmented structure with 4-bit coarse and fine DACs associated with coarse and fine DEMs are also used in the system. Finally, to reduce the leakage of the coarse quantization noise caused by the mismatch between coarse and fine DAC, a digital noise shaping block called the requantization block is used in the feedback path of the system.

Due to the delay restraint of the feedback loop associated with the last integrator, only the coarse bits for the coarse DAC of the last integrator pass through a DEM block and the fine bits go directly the fine DAC. Since any nonlinearities from the DAC of the second integrator can be shaped by the gain of the first integrator, the elimination of DEM for the fine DAC of the last integrator does not degrade the performance of the system.

Compared with the typical second-order single-stage sigma-delta modulator, the proposed system in Figure 4.1 has two additional feed-forward paths. Although these two feed-forward paths do not change the noise transfer function, they help to reduce the output swing of two integrators. Because the large output swing of integrators requires very high opamp gain, which is not easy to achieve in the submicron process, the

proposed feed-forward paths help to alleviate the stringent requirement on the opamp gain even though they increase complexity of the system.

To better illustrate the functionality of the feed forward path, a linear approximation of the system is shown in Figure 4.2 (a), wherein the quantizer is modeled by signal-independent additive error sources and half a clock cycle delay, while the integrators are represented by their transfer function in the z-domain and the total delay of the digital feedback blocks, DEM/REQ is half clock cycle. $E(z)$ represents the quantization noise caused by the 8-bit two-step ADC. Note that node A and B are the output of the first and second integrators respectively.

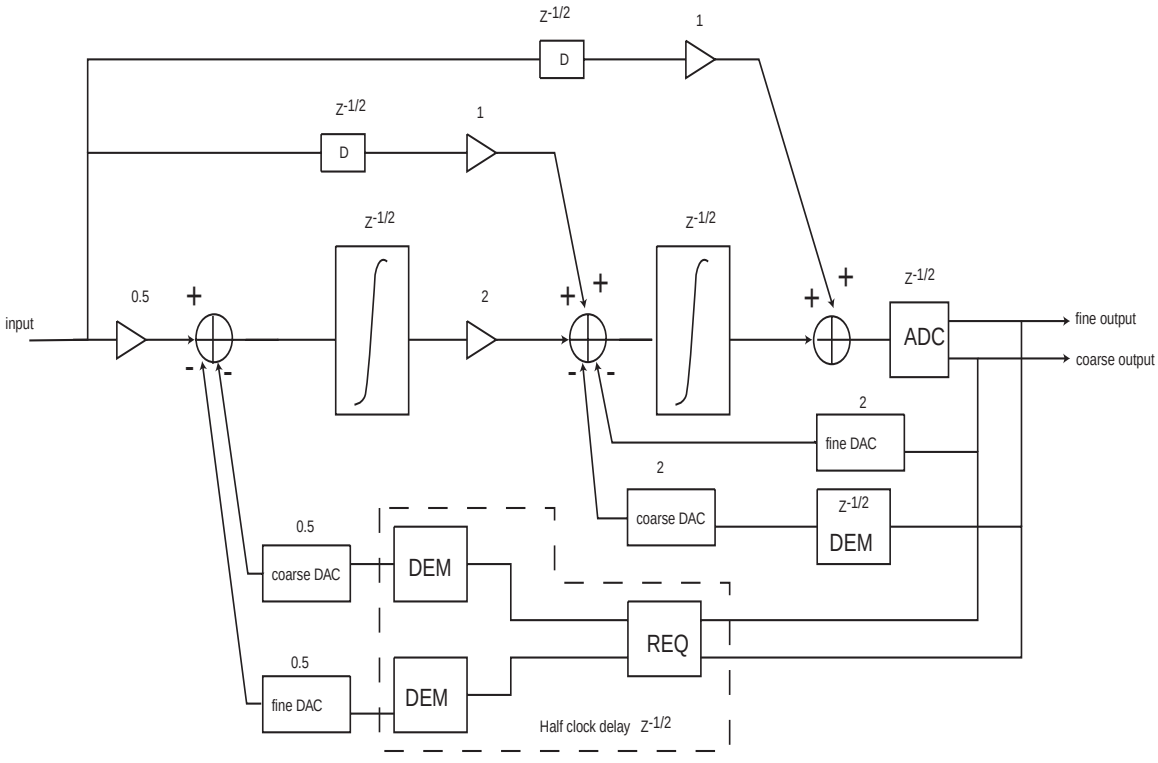

Figure 4.1 Block diagram of the system

From the linearized model of Figure 4.2 (a), the signal component of the first integrator output, A(z) is

$$A(z) = (0.5z^{-1/2} + 0.5z^{-3/2} - z^{-5/2})X(z). \quad (4.1)$$

In the same way, one can get the signal component of the second integrator output, B(z), which can be expressed as

$$B(z) = (z^{-1} - z^{-5/2})X(z). \quad (4.2)$$

Because in oversampling converters, the sampling clock frequency is much higher than the bandwidth of the input signal, $z^{-1/2}X(z)$, $z^{-3/2}X(z)$ and $z^{-5/2}X(z)$ are very close. So the signal components in node A and B as illustrated equation 4.1-2 will be very small. Although the outputs of both integrators also include the components of quantization noise, this can be ignored because an 8-bit inner quantizer is used in the system.

By comparison, Figure 4.2 (b) is a linear model of the second modulator without a feed forward path. In the same way one can calculate the signal components in the outputs of the two integrators in Figure 4.2 (b). The expression for the signal components in both nodes are

$$A' = (0.5z^{-1/2} + 0.5z^{-3/2})X(z) \quad (4.3)$$

and

$$B' = z^{-1}X(z). \quad (4.4)$$

Equations (4.3)-(4.4) demonstrate that the amplitudes of the signal components in the outputs of the integrators are very close to that of the input signal if no feed forward paths are used. As will be shown in the following sections, the small amplitude of the integrator outputs facilitates the circuit design of the integrators.

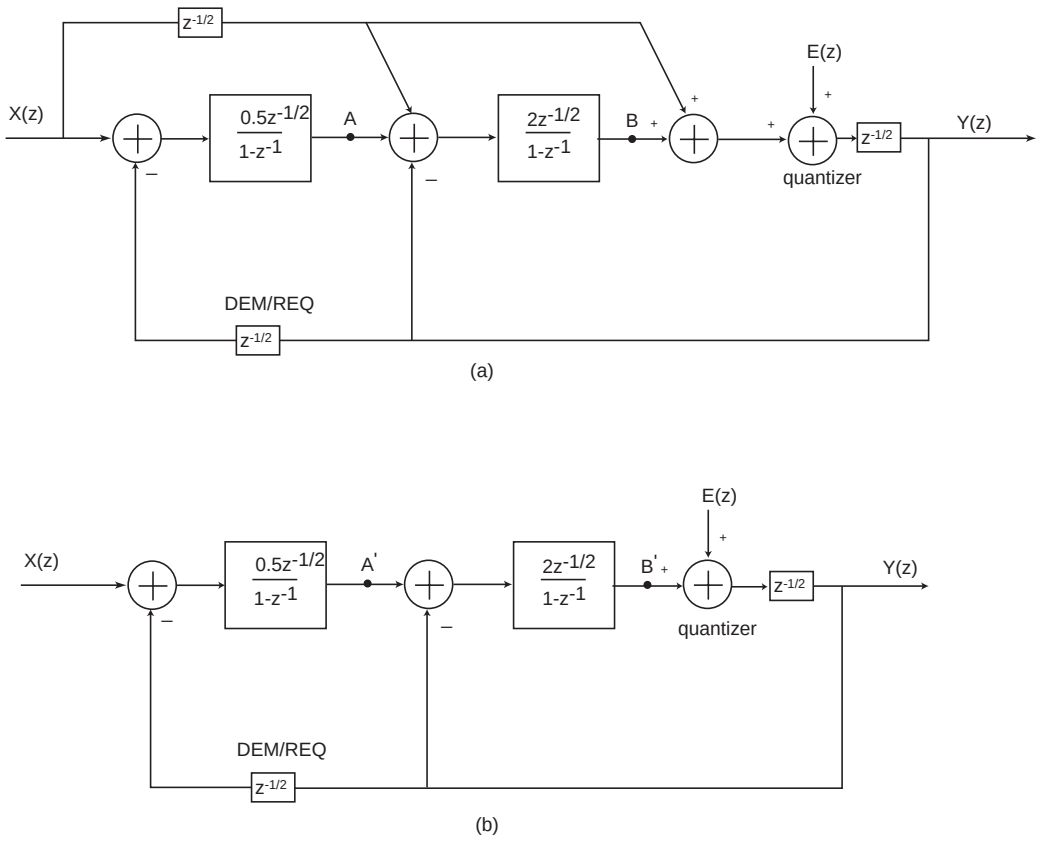

Figure 4.2 Linear model of the systems. (a) proposed system (b) proposed system without two feed forward paths

4.2 Matlab Simulations

The proposed system including the building blocks of the integrators, adder, DACs, and two-step ADC is simulated by Matlab to determine the design parameters for each block. All building blocks are built using the Matlab codes, including both ideal models and nonideal models. In the system simulation, only one building block uses the non-ideal model to characterize the nonideality of that block and all other blocks use the ideal model. In this way, the relationships between the system SNR and the non-ideality of blocks can be established and the best design parameters of the blocks are then obtained from the relation.

In the simulation, the sampling frequency is 40 MHz with an oversampling ratio (OSR) of 8. The input signal frequency is 39 kHz with amplitude of -2 dB FS. The output power spectral density is calculated by 8192 points with Hanning-windowed FFT. Under ideal conditions, the SNR of the proposed system has 2 dB less than the typical second-system with the full scale sinusoid input. The SNR of the system with all ideal building blocks is around 80 dB for the oversampling ratio of 8.

4.3 Effects of Nonidealities

The proposed sigma-delta modulator is implemented by switched capacitor circuits. The nonidealities of the switched capacitor circuits can degrade the system performance. The main error sources come from the sampling network and operational amplifier. These nonidealities can cause a change in the transfer functions of the signal and quantization noise (STF(z) and NTF(z), respectively), and degrade the modulator performance. They can be analyzed and simulated with the behavioral model in Matlab. The following subsections will explain the non-ideal effects and show how to get the best circuit design parameters.

4.3.1 Finite DC Gain of Integrators

At DC, where z=1, the ideal transfer function of the integrator assumes that its gain at DC is infinite. However, in the real circuit, the actual DC gain of the integrator is limited by circuit constraints especially the DC gain of the opamp inside it. When including the DC gain of the integrator, the transfer function of noninverting SC integrator becomes [33]

$$H(z) = \frac{C_1/C_2}{(1+\frac{1}{A_0}+\frac{C_1/C_2}{A_0})z-(1+\frac{1}{A_0})} = \frac{(1+\beta)z^{-1}}{1-(1+\alpha)z^{-1}} \tag{4.5}$$

where A_0 is the DC gain of the opamp and C_1 , C_2 are the sampling and integrating capacitors respectively. The gain error, β represents the error of the integrator gain and the phase error, α represents the pole error of the transfer function. They can be obtained as

$$\alpha = -\frac{\frac{C_1/C_2}{A_0}}{1+\frac{1}{A_0}+\frac{C_1/C_2}{A_0}} \tag{4.6}$$

and

$$\beta = -\frac{1+A_0+C_1/C_2(1-A_0)}{1+A_0+C_1/C_2} \quad . \tag{4.7}$$

The phase error proves to be the dominant error of the finite gain of the opamp because it changes the noise shaping of the modulator particularly at low frequencies. The new noise transfer function caused by the finite dc gain of opamp can be derived as

$$NTF(z) = \frac{(1-z^{-1})^2}{1-\alpha\, z^{-1}} - \frac{\alpha(1-z^{-1})z^{-1}}{1-\alpha\, z^{-1}} \quad . \tag{4.8}$$

The second term in Equation 4.8 shows that the phase error, α, adds first order shaping noise to the system while the first term indicates the creation of a small pole in the second order noise shaping function. Due to the introduction of the first order noise transfer function, the phase error α causes leakage of noise shaping at low frequency.

Because the oversampling ratio of the system is rather small and the signal bandwidth is not restricted to very low frequency, the noise leakage at low frequency

does not cause significant performance degradation of the system. The results of behavior simulation show the effects of the finite DC gain on the system.

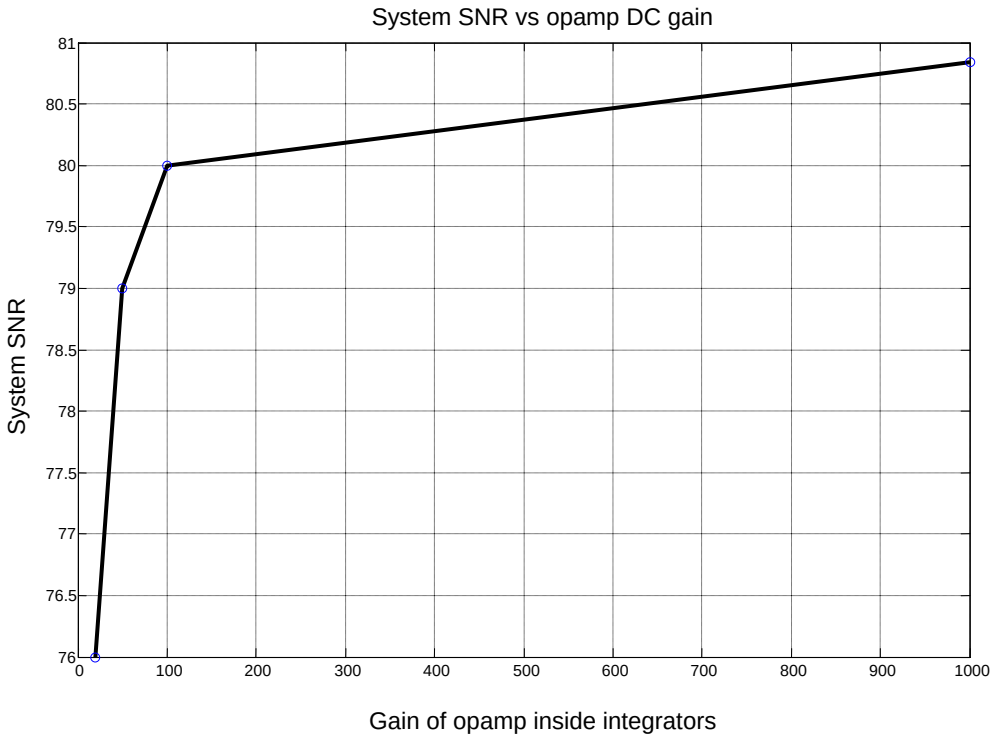

Figure 4.3 System SNR versus the dc gain of opamp

Figure 4.3 shows that to obtain the near ideal SNR, the DC gain of the opamp only needs to be over 200. Although the harmonic distortion caused by the nonlinearity of dc gain over the output range of the opamp requires a much higher DC gain than 200, the two feed-forward branches discussed in the last section greatly reduce the output swing of the two integrators, therefore relaxing the requirement of high DC gain. The behavior simulation shows that harmonic distortion caused by the nonlinearity of dc gain

can be less than 90 dB of the signal component if the gain of the opamp is greater than 60 dB.

4.3.2 Finite GBW and Slew Rate

The finite gain-bandwidth (GBW) and the slew rate of the amplifier can also cause incomplete or inaccurate charge transfer to the output of the integrator. If there is no slew rate limiting, the output of a SC (switched capacitor) integrator is

$$V_o(t) = V_o(nT - T) + V_s(1 - e^{-t/\tau}) \tag{4.9}$$

assuming the opamp only has one pole [34]. Because equation 4.5 only shows the output in the integrating phase and τ is the time constant of the integrator denoted as $1/(2\pi GWB)$. The maximum slope of the output curve occurs when t=0 and can be calculated as

$$\left.\frac{dV_o(t)}{dt}\right|_{\max} = \frac{V_s}{\tau} \tag{4.10}$$

where V_s is the step size of the integrator. If the slew rate of the opamp is greater than the maximum slope calculated from equation 4.10, no slew rate limitation occurs and the output is given by equation 4.9. However, if slew rate is less than the maximum slope, the output of the integrator can be determined as [35]

$$t \le t_0 \qquad V_o(t) = V_o(nT - T) + SR \cdot t \tag{4.11}$$

and

$$t > t_0 \qquad V_o(t) = V_o(t) + (V_s - SR \cdot t_0)(1 - e^{-\frac{t - t_0}{\tau}}) \tag{4.12}$$

where t_0 is found to be

$$t_0 = \frac{V_s}{SR} - \tau \quad . \tag{4.13}$$

Equation 4.11 shows that the small slew rate of the opamp can cause the nonlinear settling of the integrator output if t_0 is greater than half a clock cycle. Also the system simulation demonstrates that nonlinear settling error can cause very serious harmonic distortions at the output, which greatly degrades the system performance. So the slew of the opamp must be high enough to avoid the nonlinear settling of the output. In the proposed system, the slew rate of the opamp does not need to be very high because 8-bit inner quantization are used, which greatly reduces Vs, the step size of the integrator. The behavior simulation shows that the slew rate can be as small as 64V/us.

Even without the limitation of the slew rate, the integrators are still subject to the incomplete settling errors caused by the finite GBW of the opamp. Because the settling error of the opamp is linear, it only causes a gain error of the integrator similar to the capacitor mismatch of the integrator. To investigate the effects of gain error on the system SNR, a behavior model is used to model the gain error of the integrator. Figure 4.4 shows the relationship between the system SNR and the gain error of the integrators. Because the gain error only raises the noise floor of the system and has no harmonic distortion, the requirement on the gain error of the integrators can be very relaxed.

4.3.3 Capacitor Mismatch of DACs

To avoid the problem of exponential increase in the number of the unit capacitors, two DACs inside the feedback path of the modulators have to be constructed with two-parts—coarse/fine DACs. This reduces the number of unit capacitors from 255 in the nonsegmented structure to only 30 in the segmented structure for a typical 8-bit DAC because two four bit coarse and fine DACs need only 15 unit capacitors.

To reduce the mismatch of each individual DAC, DEM block is used to shift the digital input codes of the DAC, moving the DAC noise out of the signal band. Since the DEM can not completely remove the mismatch of the DAC from the signal band, it is still necessary to know the limits of DAC mismatch.

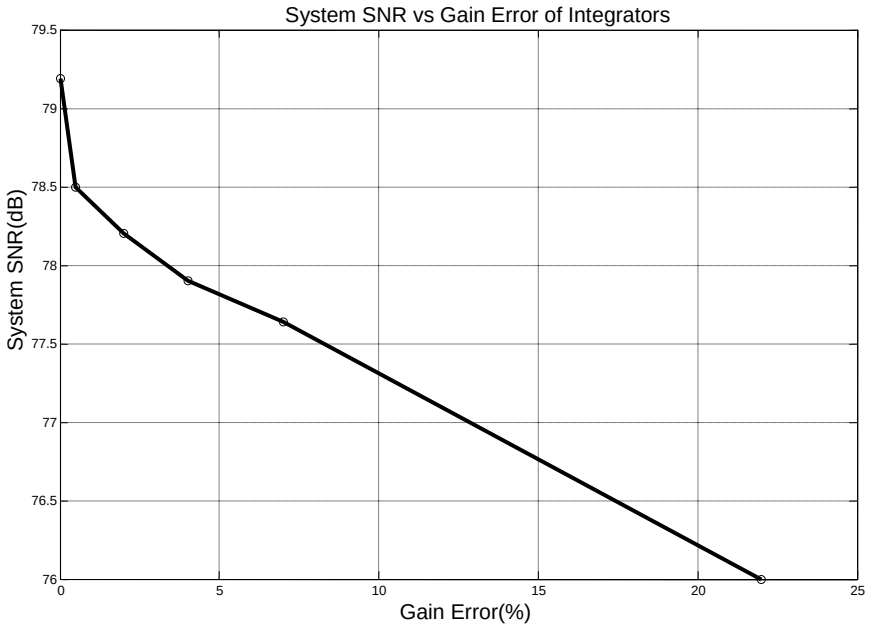

Figure 4.4 System SNR versus gain error of the integrators

In the proposed system, two different reference voltages are used for the coarse and fine DACs to achieve a fixed gain ratio between them. Based on the design requirements, the ratio of the reference between coarse and fine DAC is 4:1. However, in the real circuit, this ratio is subject to many kinds of distortion and might deviate from its ideal value. Thus it is important to know the limit of this ratio variance. The following section will discuss the effects of the DAC match on the system and give the upper limit

of the capacitor mismatch in the different DAC. The upper limit of the reference mismatch will be discussed in the last subsection.

4.3.3.1 Mismatch of coarse/fine DAC for the first integrator

Although the DAC mismatch noises from both coarse and fine DACs of the first integrator directly leak into the system output without any noise shaping, the digital correction block, DEM, can move this DAC noise to high frequency, relaxing the requirement on the mismatch of the coarse and fine DAC. A behavior model of Matlab, in which the DAC mismatch noise is modeled as a white Gaussian noise source, is used to get the upper limit of the mismatch for the coarse and fine DACs. Since the coarse DAC contributes to the major part of the total DAC output, it needs to be more accurate than the fine DAC does. The results of the behavior simulation shown in Figure 4.5 and Figure 4.6 indicate that the maximum allowable mismatch of the coarse DAC is 0.4%, five times smaller than that of the fine DAC.

4.3.3.2 Mismatch of Coarse/Fine DAC for the Second Integrator

Unlike DACs in the first integrator, the mismatch noises of DACs in the second integrator are shaped with the first order due to the gain of the first integrator. So the mismatch requirements of DACs in second integrator are less stringent than those in the first integrator.

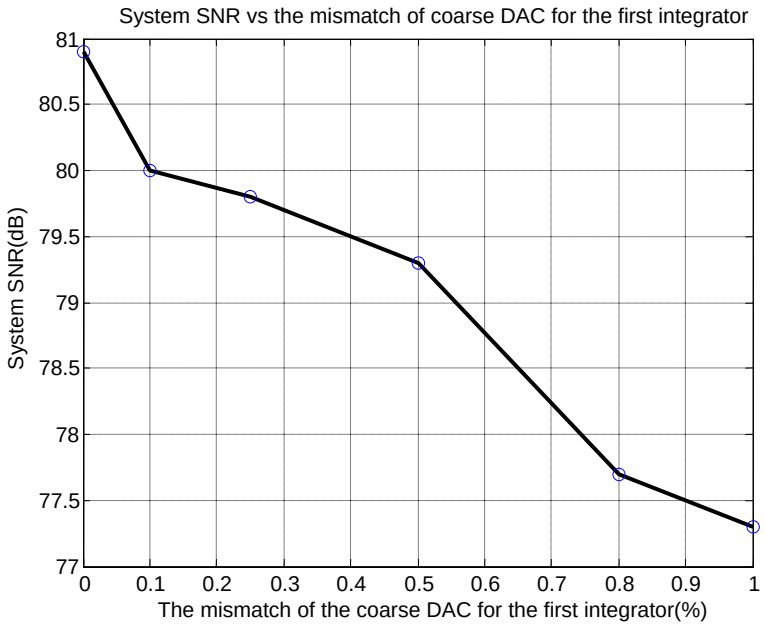

Figure 4.5 System SNR vs mismatch of coarse DAC for the first integrator

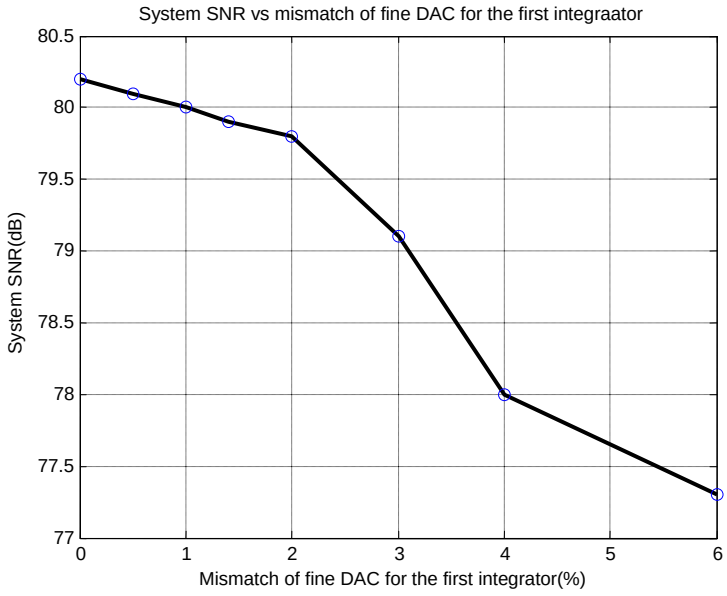

Figure 4.6 System SNR vs mismatch of fine DAC for the first integrator

4.3.3.3 Mismatch of Coarse/Fine DAC for the Second Integrator

Unlike DACs in the first integrator, the mismatch noises of DACs in the second integrator are shaped with the first order due to the gain of the first integrator. So the mismatch requirements of DACs in second integrator are less stringent than those in the first integrator.

However, because no half a clock delay is permitted along the feedback path of the second integrator, the DEM/REQ block, which causes half a clock delay in the signal path, must be removed from the feedback loop. Due to the elimination of the REQ block, coarse and fine bits generated from the two-step ADC go directly to the coarse and fine DACs in the second integrator. Along the feedback path of the coarse bits, a DEM block with half a clock delay can be added to reduce the mismatch of coarse DAC because coarse bits are generated half a clock earlier than fine bits. Since the fine DAC in the second integrator has no digital noise shaping, its maximum allowable mismatch could be even smaller than that of the fine DAC in the first integrator, which can be shown in Figure 4.8. In Figure 4.8, the maximum mismatch is only 1.4%, in contrast with 2% in Figure 4.6. By comparison, the maximum mismatch of the coarse DAC for the second integrator shown in Figure 4.7 is 0.8%, while the mismatch requirement in Figure 4.5 is 0.6%.

4.3.3.4 Mismatch of the Reference Voltage for DACs

To get the correct gain ratio between coarse and fine DACs, the coarse reference voltage providing charging current to the coarse DAC needs to be exactly four times bigger than the fine reference voltage connecting to the fine DAC.

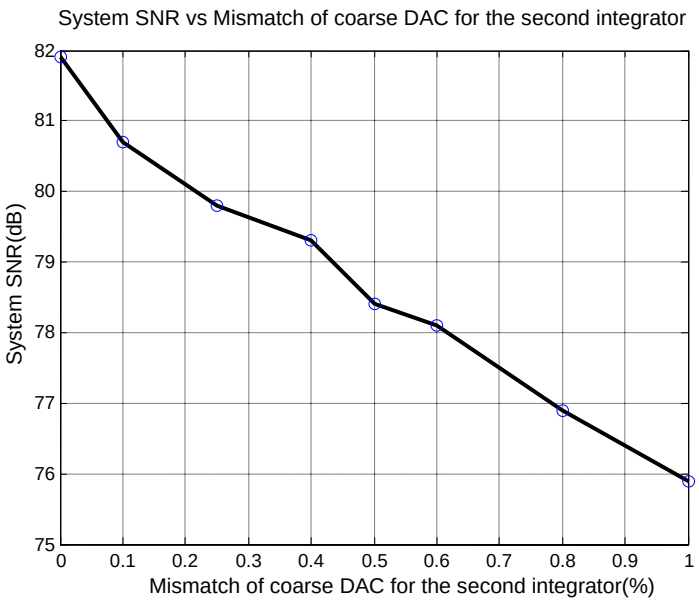

Figure 4.7 System SNR vs mismatch of coarse DAC for the second integrator

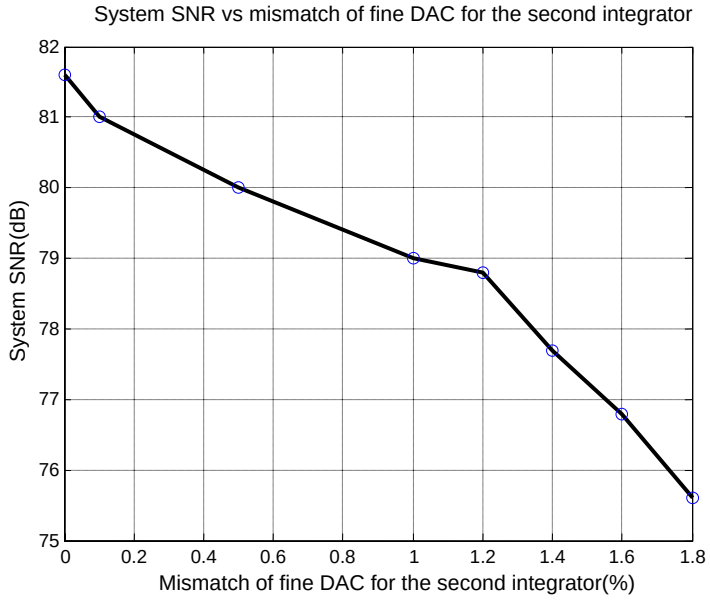

Figure 4.8 System SNR vs mismatch of coarse DAC for the second integrator

However, in the real circuit, the reference voltage is not immune to the various noise sources, resulting in a deviation of their ideal ratio. As a result of the introduction of REQ block, the coarse quantization leakage noise caused by the ratio error of the reference can be filtered digitally with first-order noise shaping. Therefore the simulation results in Figure 4.9 reveal that the reference ratio error can be as high as one percent without substantially degrading the system SNR.

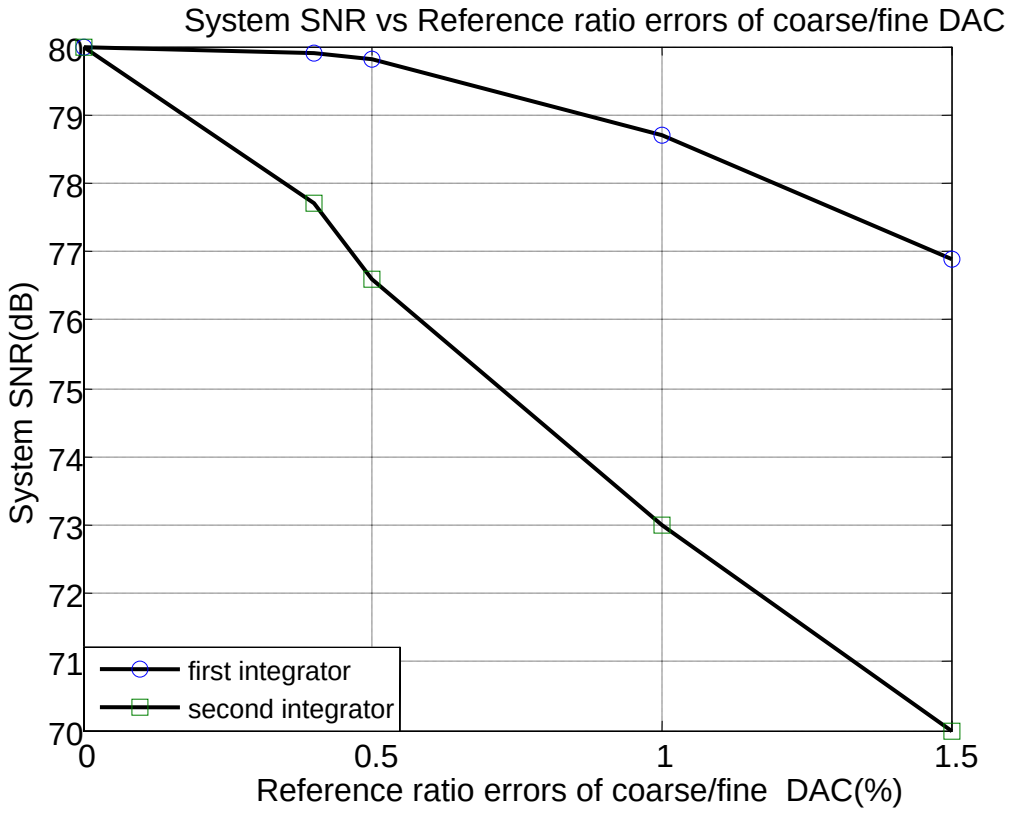

Figure 4.9 System SNR vs Reference ratio errors of coarse/fine DAC

Although the REQ block only applies to DACs of the first integrator due to the delay limitation, the gain of the first integrator helps to filter the coarse quantization

leakage noise caused by the reference error. Due to the gain of the second integrator, the coarse quantization leakage noise in the second integrator is still greater than that in the first integrator. So the reference requirement on the DAC of the second integrator should be more stringent than that of the first integrator, as indicated in Figure 4.9. From Figure 4.9, one can find that the maximum allowable reference error for the DAC of the second integrator is 0.5% compared with 1% for the DAC of the first integrator.

4.3.4 Offsets of Two-Step Quantizer

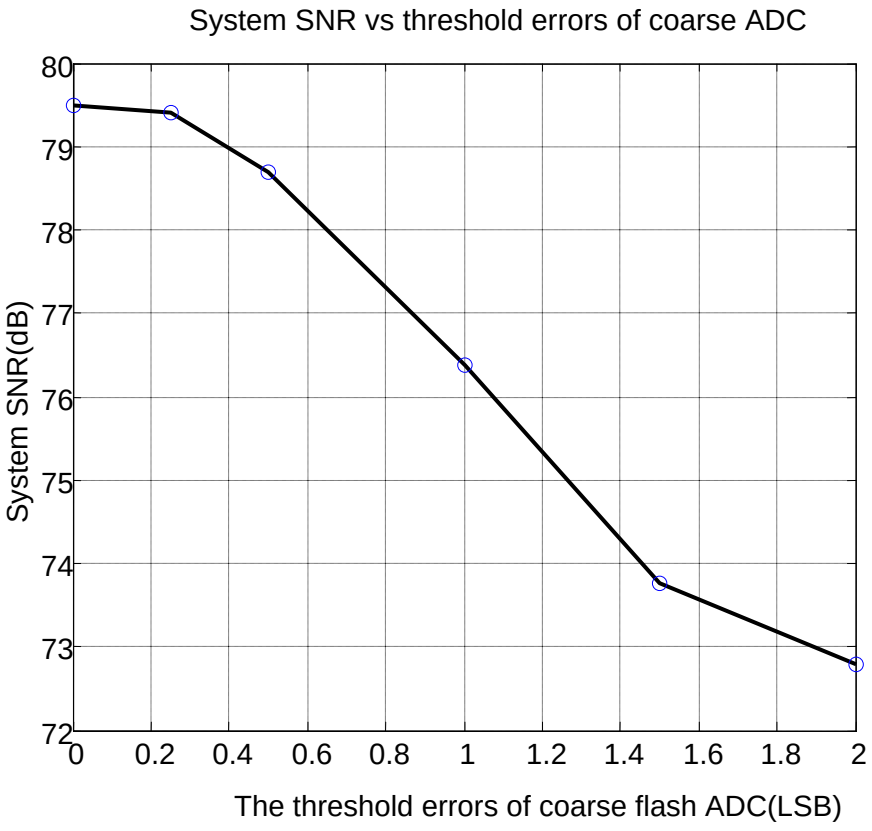

Figure 4.10 System SNR vs Offset Error of Coarse ADC

An eight-bit two-step ADC is employed as an inner quantizer to increase the system SNR at low oversampling ratio. Even though the non-ideality of the two-step ADC can be filtered by the modulator, it is necessary to know the exact upper limits on the offsets of two-step ADC.

4.3.4.1 Offsets of Coarse Flash ADC

The coarse flash ADC measures the amplitude of the input analog signal and outputs the digital code associated with it. Unlike the common two-step ADC, there is no digital correction block to correct the coarse bits. So the coarse flash needs to have the same accuracy as the two-step does. This means that maximum offsets of the coarse ADC must be within one half LSB of the two-step ADC, which can be proved in the behavior simulation of Figure 4.10. As shown in Figure 4.10, the system still maintains the near ideal SNR, less than one dB drop from the ideal value when the offsets are within half LSB.

4.3.4.2 Offsets of Fine Flash ADC

Because the coarse ADC measures the input analog signal directly, one error of certain threshold only affects the signal near that threshold. However, for the fine ADC, a certain error of threshold may affect the signal in the sixteen different ranges. Therefore, the threshold errors of the fine flash ADC have a large effect on the ADC output than that of coarse ADC. The result of the behavior simulation shown in Figure 4.11 verifies the validation of the above hypothesis. From Figure 4.10 and Figure 4.11, one can find that at the same offset error level, for example 0.5 LSB, the system SNR drops 4 dB for the offset error of the fine ADC compared with 2 dB SNR drop relating to the coarse ADC.

4.3.5 Thermal Noise and Clock Jitter

In addition to the circuit limitations, thermal noise is an important factor to determine the ADC resolution. The thermal noise is caused by thermally induced random fluctuations in the carriers due to thermal energy. The amount of motion is a direct function of the absolute temperature of the resistance. A major source is the switched-capacitor network associated with the sampling switches. The power spectral density for thermal noise is essentially white for frequencies up to the noise bandwidth.

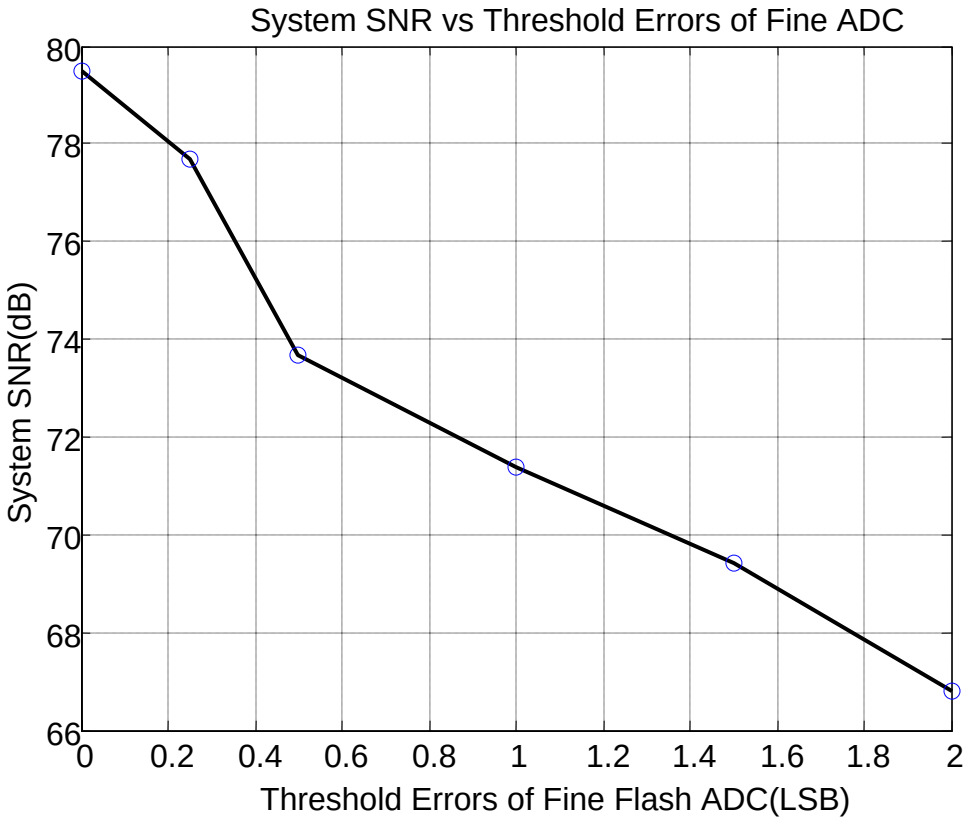

Figure 4.11 System SNR vs Threshold Errors of fine ADC

This noise determines the noise floor of the system output at the low frequency and sets a lower limit on the sampling capacitor of the first integrator. The relation between the system SNR and the sampling capacitor of the first integrator is given as [24]

$$\text{SNR} = \frac{V_s}{4}\sqrt{\frac{OSR \cdot C_s}{KT}} \tag{4.14}$$

where V_s and C_s are the full scale voltage of the ADC and the sampling capacitor of the first integrator respectively. K is Boltzmann's constant ($1.38\text{x}10^{-23}$) and T is the absolute temperature. Figure 4.12 shows the system SNR versus sampling capacitor values with two different OSRs and one volt full scale voltage. From this graph, one can find for an 80 dB SNR with an OSR of 8, the minimum sampling capacitor is around 1 pF, a moderate driving load for the opamp inside the integrator.

In practice, the sampling period is not constant but presents variations in its nominal value. These intrinsic uncertainties in the time when transitions occur are known as clock jitter. It can cause a non-uniform sampling, responsible for extra noise at the modulator output that can be estimated as follows.

The sampling error caused by the clock jitter can be represented as [36, 37]

$$\text{X(nT} + \Delta) - \text{X(nT)} = \omega_\text{b}\Delta\text{Acos}(\omega_\text{b}\text{nT}) \tag{4.15}$$

where Δ represents the error in the sampling instant. Assuming that this error has a Gaussian distribution with a standard deviation σ and a mean value of zero, its power spectral density results in

$$S(f) = \frac{A^2(\omega_b\sigma)^2}{2f_s} \tag{4.16}$$

where f_s is the sampling frequency. Equation 4.16 shows that the noise caused by the clock jitter is equally distributed over the sampling frequency and its power density is proportional to the square of the frequency of the input signal. Because of that, the jitter noise plays a very important role in high speed applications, where it may become the dominant error source.

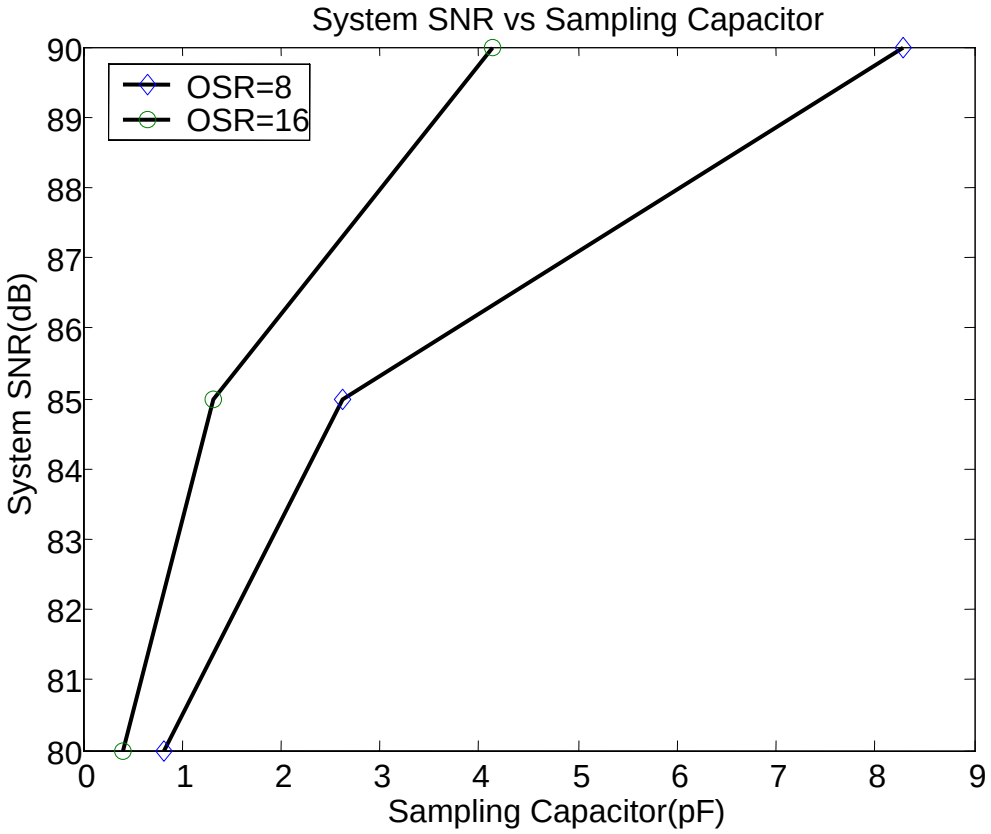

Figure 4.12 System SNR vs the sampling capacitor of the first integrator

4.4 Simulation Results Summary

A high speed and high resolution sigma-delta ADC with an 8-bit two-step quantizer is introduced. The proposed system architecture has been investigated and evaluated the performance. With all non-idealities discussed in the previous subsections, the behavioral model simulations are performed with Matlab. The design parameters for the building blocks are extracted from iterated simulations. Table 4.1 shows the design parameters obtained by the simulations.

Table 4.1 Circuit design parameters

Sampling Frequency	40 MHz	Opamp DC Gain	60 dB
Signal Bandwidth	2.5 MHz	Slew Rate	64 V/us
Oversampling Ratio	8 or 16	Integrator Gain Error	2%
Quantizer Bits	8 bits	DAC Mismatch 1st Integrator	Coarse 0.4% Fine 2%
Sampling Capacitor	1.6 pF	DAC Mismatch 2nd Integrator	Coarse 0.8% Fine 1.4%
ADC Mismatch	Coarse 0.5 LSB Fine 0.25 LSB	Reference Mismatch	1sth Integ 1% 2nd Integ 0.5%

5 CMOS VLSI Implementation

To test the architecture described in the previous chapter, a second-order sigma-delta modulator with 8-bit inner quantization has been designed in the TSMC 0.25 μm mixed-signal CMOS process. It is the first reported ΣΔ modulator with 8-bit inner quantization. Compared with the common single-stage ΣΔ modulator with less than 6-bit inner quantization, its oversampling ratio can be as small as eight while maintaining the high resolution. Because the critical analog building blocks such as integrators, DACs, and subtractors are all built with the switched capacitor circuitry, the overall system performance, to a large extent, depends on the performance of this type of circuitry. Therefore, the main blocks of switched capacitor circuitry including the operational amplifier (opamp) will be discussed in section 5.2 and 5.3. In addition, the implementations of the two-step ADC including coarse/fine flash ADCs, comparators, and subtractor are described in section 5.1. The design of the digital circuitry including DEM/REQ and the clock generator is in section 5.4. The final section is the floor plan and the layout design.

5.1 Two-Step ADC

The two-step ADC block is the inner quantization of the multibit Delta-Sigma modulator. Since it is one part of the system and has different timing diagram and offset

requirements compared to the common stand-alone two-step ADC, some special design issues must be addressed during the design of the two-step ADC block.

For most stand-alone two-step ADCs, the offset requirement of the coarse ADC is very relaxed because the digital correction block can correct one-bit error of the coarse ADC based on the output of the fine ADC [38]. However, for the two-step ADC block used as the inner quantization of this system, the coarse ADC needs to achieve the same accuracy as the entire two-step ADC block because no digital correction block can be applied due to the delay constraints of the system.

The two-step ADC block includes the coarse and fine flash ADCs with 30 comparators, a subtractor/DAC, and digital encoder circuitry to convert the thermometer code to binary code. The typical operation of two-step ADC is as followed [1,4]. The input signal first goes to the coarse flash ADC to convert the four MSBs. Then this digital code is fed to the coarse DAC to generate the 4-bit approximation of the input signal. The error of this 4-bit approximation can be obtained through a simple analog subtractor. This error then goes to the final ADC to get the four LSBs.

The block diagram of the two-step ADC can be seen in Figure 5.1. The amplifier with a gain of 2 is used to increase the input range of the fine ADC thus reducing its mismatch requirements.

Since the subtractor is realized by the switched-capacitor circuit, it is very convenient to add a fixed gain amplifier to it, simply by changing the capacitor ratio between the input and feedback capacitors. The drawback of adding this fixed-gain amplifier is that it increases the settling time of the subtractor due to the increase of the

feedback factor. The gain of the amplifier is set to 2 to achieve the moderate mismatch requirement of the fine ADC while maintaining the high speed of the subtractor.

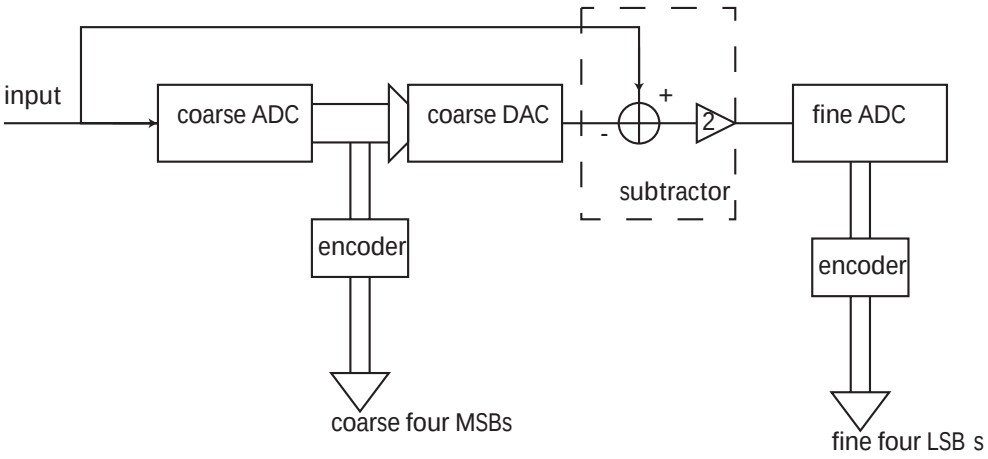

Figure 5.1 The block diagram of the two-step ADC

5.1.1 Flash ADC

The block diagram of the flash ADC is shown in Figure 5.2. Similar to the typical 4-bit flash ADC [1,4], it includes 15 comparators, one resistor string, and a decoder. The resistor string subdivides the main reference into 16 equally spaced voltages, and the comparators compare the input signal with these voltages. If the analog input is between Vj and Vj+1, comparators A1 through Aj produce ONEs at their outputs while the rest generate ZEROs. Consequently, the comparator outputs constitute a thermometer code, which is converted to binary code by the decoder and also provides the input to DAC to generate the analog approximation of the input signal. The actual circuit of the flash ADC uses the fully differential architecture instead of the single-ended structure shown in Figure 5.2 to improve its rejection of commode-mode noise. Instead of directly comparing the input signal with the reference voltage, in the fully differential

architecture, the difference of two analog differential inputs is compared to the difference of two reference voltages. Because the difference between reference voltages can be positive, zero, or negative, the mid point of the input range of the fully differential structure is zero compared with half of the reference voltage in the single-ended structure.

The offset of the flash ADC arises from two sources. One is the offset of the resistor string caused by the mismatch of the poly resistor during the process of fabrication. Another is the offset of the comparator generated from the mismatch of the differential pair transistors. Usually, the offset of the comparator is the dominant source of the mismatch because a simple layout technique can greatly reduce the mismatch of the resistor string while many complex circuit and layout techniques need to be used to deal with the mismatch of the comparator. Since the maximum allowable offset for both coarse and fine flash ADC is 0.5 LSB equaling 7.8 mV for the full-differential reference of 4V, the same comparator with a maximum offset of less than 7 mV can be applied to both coarse and fine ADC. Several circuit and layout techniques such as offset cancellation and common-centroid layout are applied to the design of the comparator and the resistor string to meet the offset requirement on the flash ADC.

As shown in Figure 5.2, the resistor string is nothing but sixteen resistors connected in series to get fifteen equal spaced voltages. Although it seems that any sixteen resistors with the same resistance can meet the requirement of the resistor string, too big will limit the conversion rate of the flash ADC because of the big RC time constant of the fifteen equal spaced reference voltages. Based on simulation, the unit resistor is set to be 100Ω to meet the speed requirement of the 50 MHz while maintaining low power dissipation.

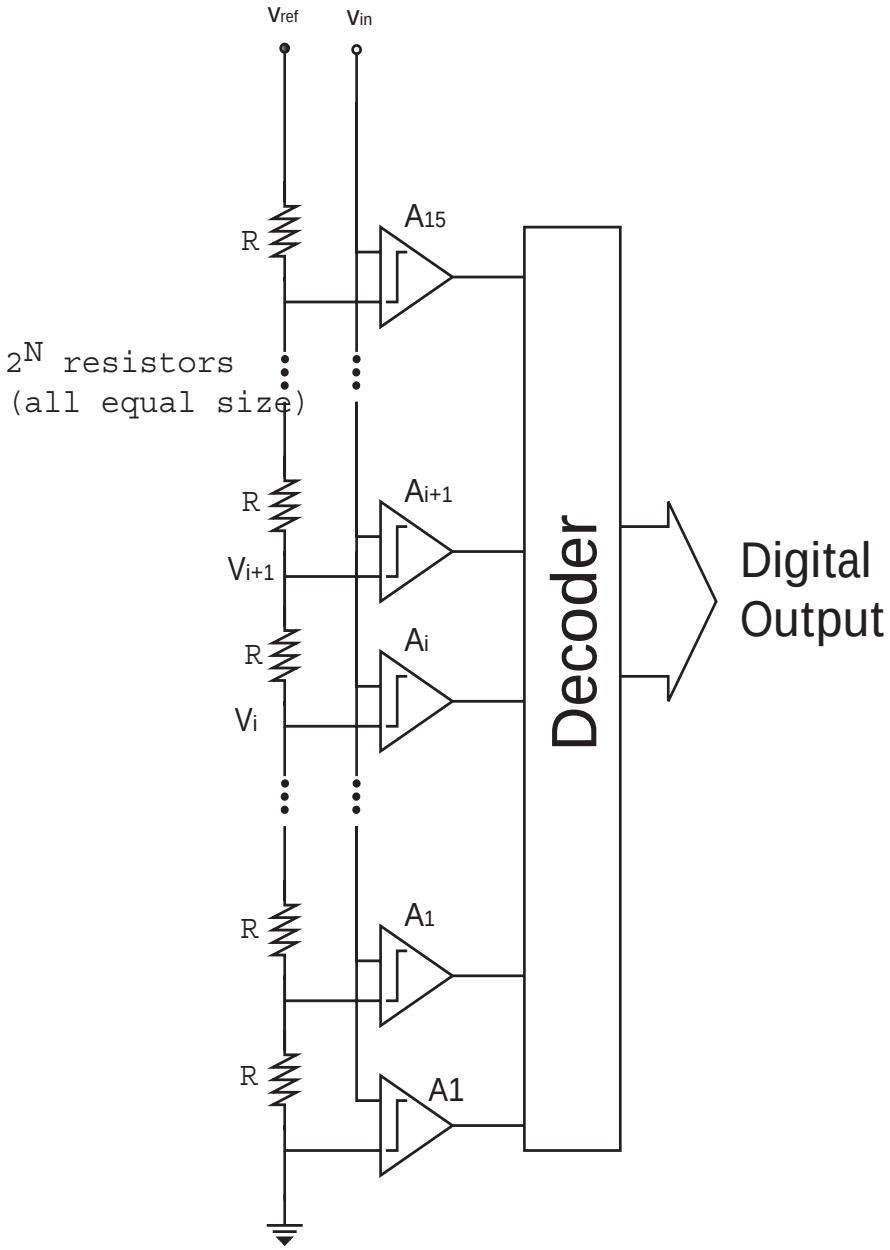

Figure 5.2 The block diagram of the flash ADC

To get equal size voltages, it is important to reduce the mismatch among the sixteen unit resistors. To avoid the problem of different etching speed of poly silicon, all

the unit resistors have the same interval from their two neighboring resistors while two dummy resistors are added to connect to the first and last resistor to make sure the first and last resistor have the same interval as those inside the string. Also all unit resistors are built in the same shape with large width to improve the matching.

5.1.2 Comparators

Figure 5.3 is the diagram of the comparator, which consists of two preamplifiers, one latch, one RS-latch and several switches. Similar to the comparators in [1,18], two preamplifiers are used to amplify the difference between input signal and the reference signal. If the total gain of the two amplifier stages is high enough, the large offset of the latch will have a small effect on the final output because the amplified difference becomes much larger than the offset. If the offset of the latch becomes negligible, the major source of offset in the comparator will be the two preamplifiers. A simple differential amplifier can be chosen to build these two preamplifiers to optimize the speed and power dissipation.

However, to meet the offset requirement of 7 mV, a very large differential pair with a gate area of over 20 μm^2 is required to accommodate the variance of the fabrication process. The large transistor results not only in a big chip area but a big capacitive load to the previous stage. To make the load problem even worse is that the previous stage of the coarse and fine ADC need to drive fifteen comparators in parallel. To solve this dilemma, offset cancellation techniques are used for the comparators to reduce the input capacitor while obtaining a low offset.

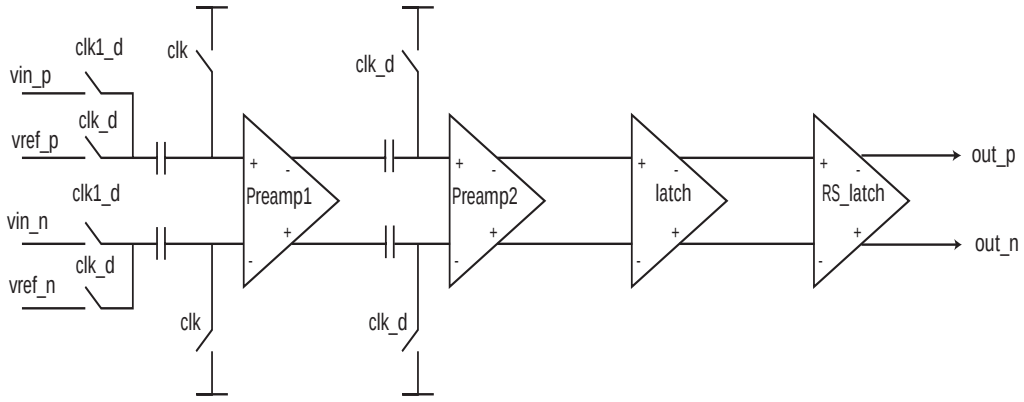

Figure 5.3 The block diagram of the comparator

There are two offset cancellation techniques in the design of comparators. One is called input offset storage (denoted by IOS), another is called output offset storage (denoted by OOS) [1]. Although both techniques save the offset on the small capacitors to correct offset errors, OOS is more appealing than IOS because in OOS the gain of the preamplifier can be less than 10 and it has a fast settling time during the reset mode, which can help to reduce the interference of the kickback noise on the resistor string [1, 39]. The small gain amplifier is not only easy to design but also shows a very high speed with low power dissipation.

Two phase clocks (clk, clk1) are used to divide the operation of the comparators into two periods: sampling and resetting period. During the resetting period when clk is high, the input of the first amplifier ties to the ground. Due to the offset of the first stage, the first stage has a small output. Since there are two coupling capacitors between preamp1 and preamp2, the offset output of the first preamplifier can be stored on these two coupling capacitors. In the next sampling period when clk1 is high, both preamplifiers are in the normal amplifying mode. Because the offset of first preamplifier

is already stored on the coupling capacitors, it cancels the offset of the first preamplifier. Thus the input of the second preamplifier includes only the first preamplifier output.

Although the same offset cancellation process can be applied to the second preamplifier to cancel its offset if there are two coupling capacitors to save the offset voltage, the direct coupling between preamp2 and latch can greatly help to reduce the large kickback noise of the latch generated when recovering from the imbalanced state.

Two phase clocks not only cancel the offset of the first preamplifier but also help to convert the fully differential inputs to a common single-ended one as illustrated in Figure 5.3. During the resetting phase when clk and clk_d are high, two differential references (vref_p,vref_n) are sampled on the coupling capacitors. In the next sample stage when clk1_d is high, the left plates of the coupling capacitors connect to the differential inputs and their right plates are floating, leaving the difference between two differential inputs and two differential references on the input of the preamp1. So the input voltages of preamp1 become

$$V_{+} = V_{inp} - V_{refp} \tag{5.1}$$

and

$$V_{-} = V_{inn} - V_{refn} \tag{5.2}$$

and the comparator output becomes

$$V_{out} = A(V_{+} - V_{-}) = A(V_{inp} - V_{refp} - V_{inn} + V_{refn}) = A\left[(V_{inp} - V_{inn}) - (V_{refp} - V_{refn})\right] \tag{5.3}$$

where A is the gain of the comparator.

Simply by adding two capacitors, a short-delay adder can be integrated into the comparator circuit in Figure 5.3. Figure 5.4 shows the schematic of this new type comparator with a short-delay adder. Due to the introduction of the two new sampling

capacitors, two inputs (Vin_1, Vin_2) will add together first and then compare with the reference voltage. So the comparator output becomes

$$V_{outl} = A\left|\frac{1}{2}(V_{inp1} - V_{inn1}) + \frac{1}{2}(V_{inp2} - V_{inn2}) - (V_{refp} - V_{refn})\right|. \quad (5.4)$$

Equation 5.4 reveals that the new comparator compares the sum of the input signal with the reference voltage. Although the input signal and the reference voltage have the different coefficient in equation 5.4, the reference voltage can be scaled down to one half to match the coefficient of the input signal.

The delayed version of the clock, clk_d, is used to eliminate the offset of charge-injection caused by the two switches connecting to the input of pramp1. When the main clock, clk goes low while the delay clock clk_d is still high, the imbalance of the input voltage in the preamp1 caused by the offset of charge-injection is amplified by preamp1 and saved on two coupling capacitors. So the offset due to charge-injection in the first preamp can also be removed in same way as the offset in preamp1. Although switches connecting to the reference voltage during the resetting stage also have the problem of different charge injections, this effect can be ignored if all the switches controlled by clk_d turn off later than the switches connecting the input of the first preamp, which will be further discussed in the design of the integrator.

5.1.2.1 Preamplifier

Figure 5.5 shows the schematic of two preamplifiers using the architecture of the simple differential amplifier [1,4] to get a small dc gain. Because the offset of preamp1 can be eliminated using the offset cancellation techniques discussed above, preamp1 has smaller input differential pair than that of preamp2. The gain of this simple differential

amplifier is determined by the ratio of gm of the input differential pair and that of the load transistor. Since the input differential pair uses NMOS transistor while the load transistor use PMOS, the gain of this amplifier can easily reach 6V/V with the small size of the input differential pair. Table1 is the performance summary of these two amplifiers.

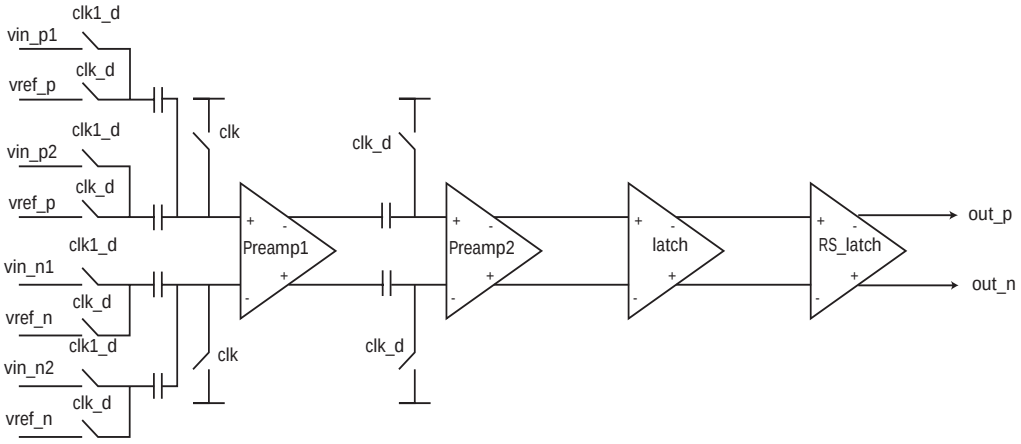

Figure 5.4 Block diagram of the new type comparator with short-delay adder

Figure 5.6 shows the post-layout simulation results of the two preamplifiers. From the bottom to top, it contains the waveforms of preamp1 input, preamp2 input and preamp2 output respectively. Because of the big kickback noise from the latch, premap2 has a much longer delay than that of preamp1.

The output range is another factor considered during the design of the preamplifier. The wide output range in preamp1 can help to avoid the saturation errors occurring when the preamp output is out of its range due to the large product of offset and gain. The output range of preamp1, 1.2 V, as illustrated in Table 5.1 has enough margins to avoid saturation errors.

Table 5.1 Performance summary of the two preamplifiers inside the comparator

Amplifier name	Gain	Bandwidth	Delay	Input Range	Output Range	Tail Current(A)	Offset
Pramp1	6	240 MHz (35 fF load)	0.358 ns	1V~1.7V	0.8V~2V	50uA	15mV
Pramp2	6.5	176MHz (40 fF load)	0.586 ns	1V~1.4V	1V~1.8V	40uA	10mV

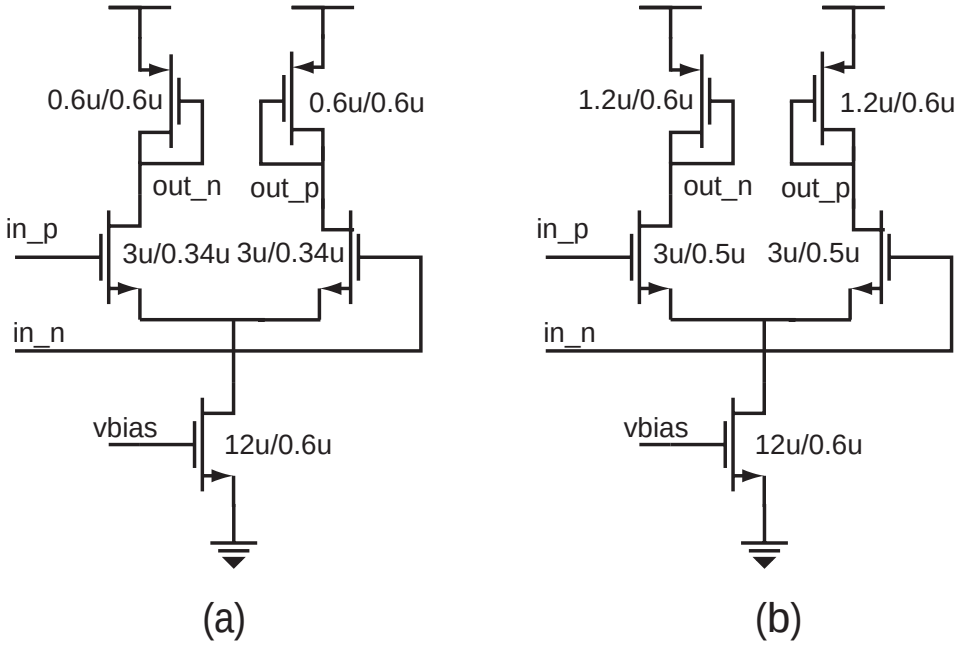

Figure 5.5 The schematics of the two preamplifiers. (a) and (b) are the schematic of the preamp1 and preamp2 respectively.

5.1.2.2 Latch

Figure 5.7 shows the schematic of the latch, which was first proposed in [31]. The dynamic operation of this circuit is divided into two modes: reset mode and regeneration mode. During the reset mode, switch M12 is on, resetting the previous state in nodes Va and Vb. At the end of the reset mode, a voltage proportional to the input voltage

difference is established between nodes Va and Vb. This voltage will act as the initial imbalance for the following regeneration time interval. In the meantime, as the n-channel flip-flop is reset, the p-channel one is also reset by the two closed pre-charge transistors which charge two output nodes (out_p and out_c) to the positive power supply voltage.

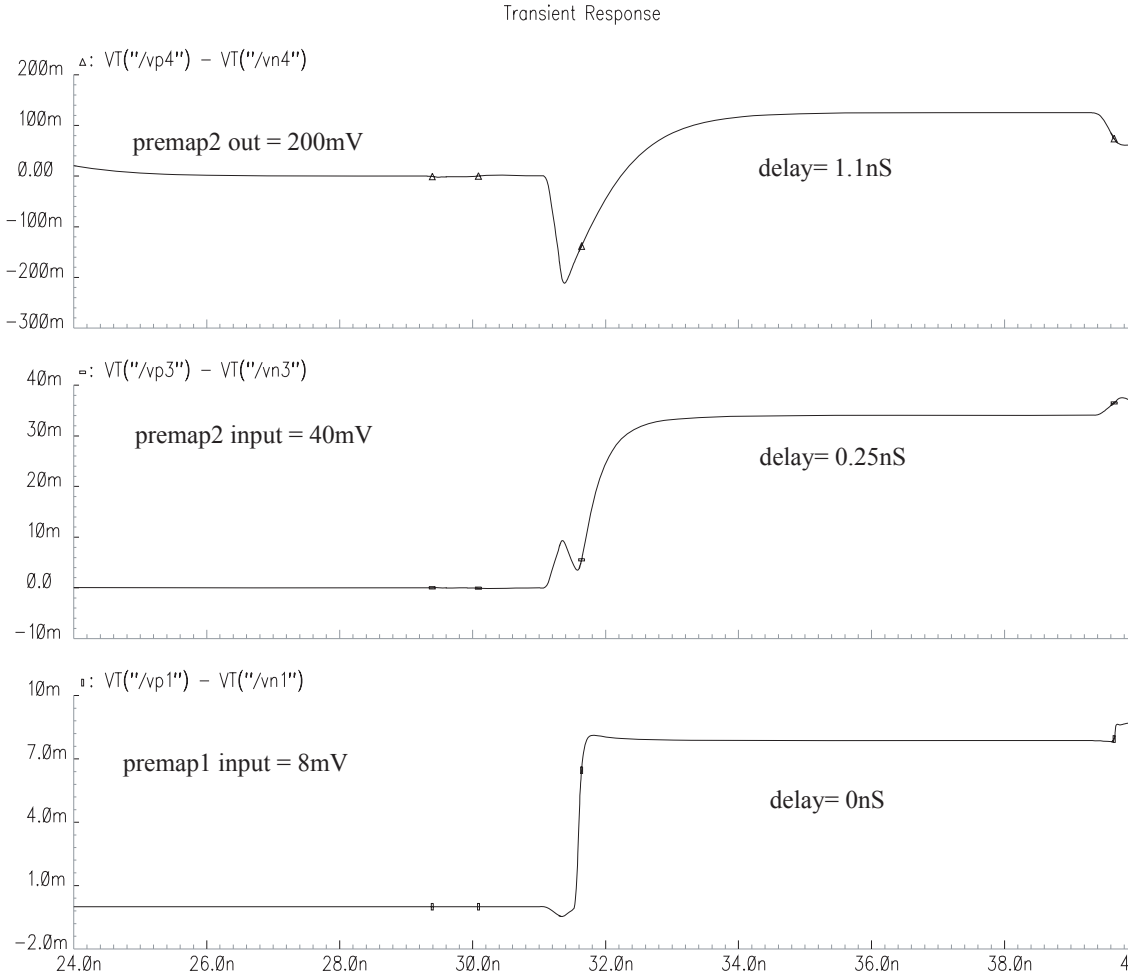

Figure 5.6 The post-layout simulation of the two preamplifiers

The regeneration is initialized by the opening of swich M12. Since the strobing transistors M8 and M9 isolate the n-channel flip-flop from the p-channel flip-flop when clk1 is low, the use of two nonoverlapping clocks performs the regeneration process in two steps.

The first step of regeneration is within the short time slot between clk going low and clk1 going high. The second regeneration step starts when clk1 goes high and M8 and M9 are closed. The n-channel flip-flop, together with the p-channel flip-flop, regenerate the voltage differences between nodes a and b and between vout_p and vout_n. The voltage difference between two output nodes is soon amplified to a voltage swing nearly equal to the power supply voltages. There is no slew rate problem in the regeneration period because the p-channel flip-flop is used instead of two class-A current sources.

The short time slot between clk going low and clk1 going high is critical to reducing the offset of the latch. The total mismatches caused by the charge injection of M8 and M9, the mismatch of p-channel flip-flop, and the mismatch of the R-S latch in the next stage are divided by the gain of in the first regeneration step when referred to the input node to calculate the input equivalent offset voltage. If the regeneration gain in the first step is high enough, the above mismatches can be neglected. Therefore, the mismatch of the latch comes mainly from the input differential pair (M1, M2), n-channel flip-flop transistor pair (M4,M5), and switching transistor M12. The total equivalent input offset voltage can be approximately expressed as

$$V_{\text{offt}} = V_{\text{off1}} + \frac{g_{m4}}{g_{m1}}(V_{\text{off2}} + V_e) \tag{5.5}$$

where V_{off1} and V_{off2} represent the offset voltages in the input transistor pair and the n-channel flip-flop transistor respectively and V_e is the differential charge injection error caused by the unequal injected charge between a and b when M12 turns off rapidly. The offset of the charge injection error can be reduced by choosing small size for M12 in relation to the total capacitances of a or b and the symmetrical layout. The term $g_{m4}/g_{m1}V_{off2}$ is normally smaller than V_{off1} since the two transistors in the n-channel flip-flop are at 0V substrate bias.

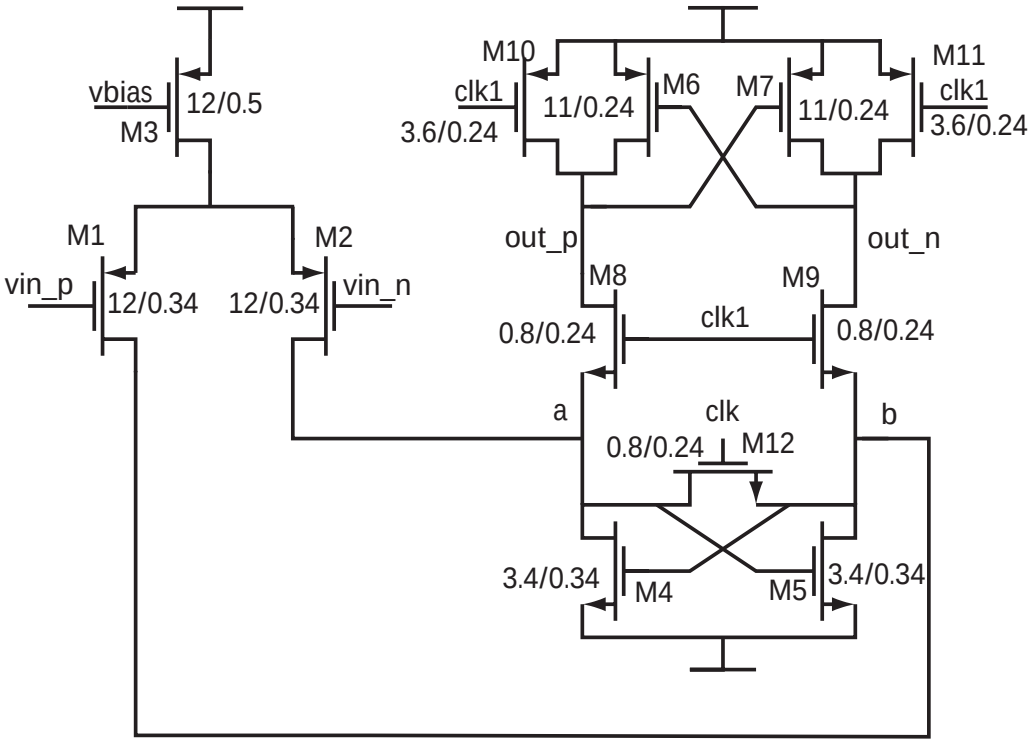

Figure 5.7 The schematic of the latch

The regeneration time constant in the first step is determined by the total capacitance of node a or b, the transconductance of the n-channel flip-flop and the conductance of the switching transistor M12. It can expressed as

$$\tau = C_a /(g_{m4} - 2g_{o12}) \tag{5.6}$$

where g_{m4} and g_{o12} are the tranconductance of M4 and the conductance of M12 respectively.

Equation (5.5) shows that when g_{o12} is smaller than half of g_{m4}, the time constant becomes positive and the first step of regeneration begins. It also indicates that the parasitic capacitance on the two nodes (a,b) will directly slow down the regeneration speed. Therefore careful layout is needed to reduce the parasitic capacitance on those two nodes. In this design the total capacitance of a or b is around 20 fF and the time constant is 0.1 ns. Since the time for the first step generation is about 1 ns, or ten times the time constant, that the latch obtains enough gain to make any mismatch after the first step of regeneration negligible.

In order to minimize the charge injection error, the minimum size of switch transistor M12 should be applied. However, there is a limit on the size of M12 especially during the resetting mode. If M12 is too small it can cause an incomplete resetting between a and b. For example, assume that node a is at the high-voltage level before reset. The voltage difference between nodes a and b reduces very quickly at the beginning of reset. Later the reduction rate slows down. It will have a local minimum at some instant if the current through M12 is equal to the current through M5 while M4 just reaches the edge of conduction, which should be avoided in high-speed applications. In this design, W/L of M12 is about one third that of M4 to avoid settling on the local minimum point.

5.1.3 Subtractor

The subtractor is a very important part of the two-step ADC. It is used to subtract the input signal from the output of the coarse DAC to result in the error of the coarse approximation, which in turn goes to the input of the fine flash ADC to generate the fine bits. The accuracy of the analog subtractor needs to be similar to that of the two-step ADC.

Figure 5.8 (a) shows the schematic of a simple single-ended subtractor based on a switched-capacitor circuit [4]. Two nonoverlapping clocks indicated as 1 and 2 divide the operation of the subtractor into two stages. First, in the sampling stage when clock 1 goes high, input v1 is sampled on C_{s1} while another sampling capacitor C_{s2} and feedback capacitor C_F are reset. In the next subtracting stage when clock 2 goes high, C_{s1} is reset and V_2 is sampled on C_{s2}. Because of the virtual ground and high input impendence of opamp, in the subtracting stage, the combination of the charging or discharging current flowing into or out of the two sampling capacitors (C_{s1} and C_{s2}) equals the current flowing in or out of the feedback capacitor C_F. The same amount of charging /discharging current means that the total charge change on the sampling capacitors must equal the charge change on the feedback capacitor in the subtracting stage. This basic charge transfer equation can be expressed as

$$\Delta Q_s = \Delta Q_F \tag{5.7}$$

where ΔQ_s and ΔQ_F are the total charge change of the sampling capacitor and the feedback capacitor respectively.

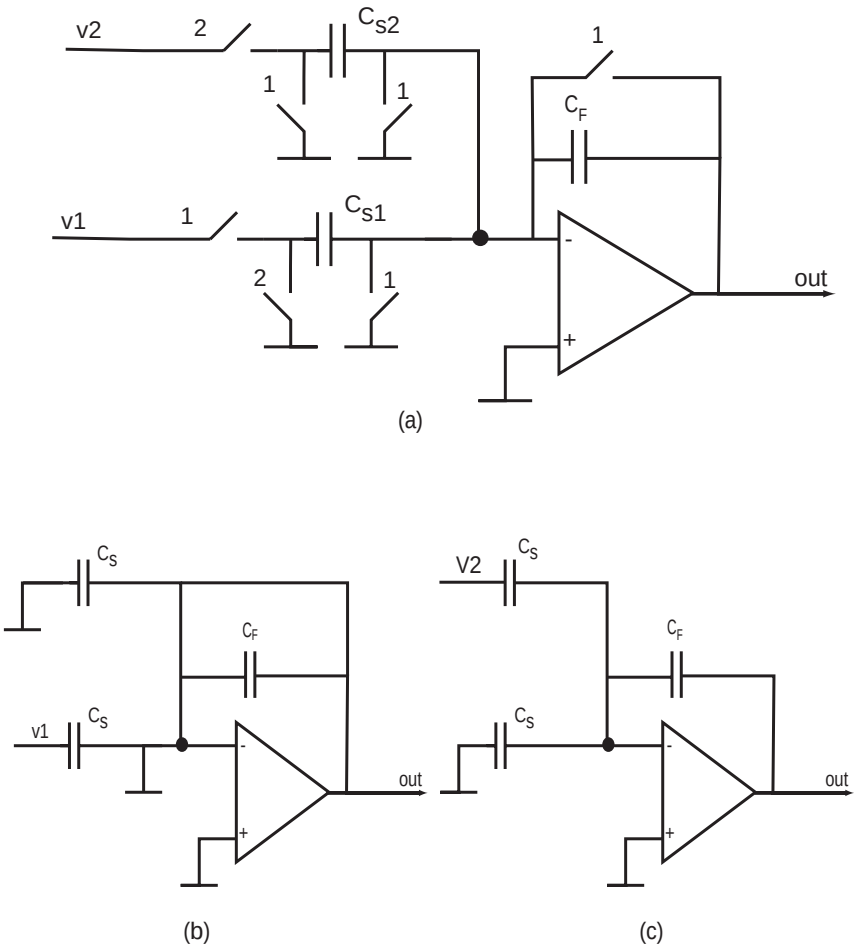

Figure 5.8 The block diagram of a simple single-ended subtractor

The charge change of the capacitors can be seen in Figure 5.8 (b) and (c). In the sampling stage as illustrated in Figure 5.8 (b), only C_{s1} is charged to the input voltage. In the next subtracting stage as shown in Figure 5.8 (c), C_{s1} is reset and both C_{s2} and C_F are charged. Suppose *nT* and *(n+0.5)T* represent the end of one sampling stage and the following subtracting stage respectively, where *T* is the clock cycle. The charge change of the sampling capacitor and feedback capacitor can be derived as

$$\Delta Q_s = V2(nT + 0.5T)C_{s2} - V1(nT)C_{s1} \tag{5.8}$$

and

$$\Delta Q_F = -V_{out}(nT + 0.5T)C_F . \tag{5.9}$$

Combining equations (5.7)-(5.9) and assuming that both C_{s1} and C_{s2} equal C_s, one can get the expression of output voltage which is define as

$$\begin{aligned} V_{out}(nT+0.5T) &= V1(nT)\frac{C_{s1}}{C_F} - V2(nT+0.5T)\frac{C_{s2}}{C_F} \\ &= \frac{C_s}{C_F}\left[V1(nT) - V2(nT+0.5T)\right] \end{aligned} . \qquad (5.10)$$

Assuming $V1(nT+0.5T)$ equals $V1(nT)$, equation (5.10) can be rewritten as a

$$V_{out} = \frac{C_s}{C_F}(V1 - V2). \qquad (5.11)$$

Equation (5.11) demonstrates that the output in Figure 5.8 (a) equals the difference of the two input voltages times the capacitor ratio. If the feedback capacitor C_F is one half of the sampling capacitor C_s, the difference between the two inputs can be amplified by a factor of two.

To improve the rejection of the common-mode noise, the fully differential subtractor/DAC shown in Figure 5.8 is used in the design [40]. The fully differential circuit uses the voltage difference between the positive node and the negative node to represent a signal while the single-ended circuit only uses the absolute voltage.

Similar to the single-ended subtractor, the operation of the circuit in Figure 5.9 can also be divided into two stages: the sampling stage and the subtracting stage. During the sampling stage when clock 1 and 1d go high, one pair of the fully differential input signals (vin_p, vin_n) is sampled on two sampling capacitors, while all thirty unit-capacitors of the DAC and two feedback capacitors are reset. In the next subtracting stage when clock2 and clock2d stay high, two input capacitors are reset while the unit-capacitors of the DAC are either charged to the positive reference voltage or discharged to the negative reference voltage depending on the input digital code of the DAC. If the

input digital code of the DAC is N, N unit-capacitors will be charged to vref_p and the rest of the unit-capacitors will be discharged to vref_n in the upper portion of the DAC. In the low portion of the DAC, things are just the opposite. 15-N unit-capacitors are charged to vref_p and the N unit-capacitors are charged to vref_n.

Because of the virtual ground and high impendence of the opamp inside the subtractor, the same method used to analyze the circuit of Figure 5.8 can also apply to the fully differential circuit in Figure 5.9. According to the charge transfer equation, the total charge change of the input capacitor connecting to V_{inp} and all the unit-capacitors in the upper portion of the DAC equals the charge change of the output capacitor connecting to vout_p. So the voltage at the positive output node can be derived as

$$V_{outp} = V_{inp}\frac{C_s}{C_F} - \left(\frac{NC_s}{16C_F}V_{refp} + \frac{(15-N)C_s}{16C_F}V_{refn}\right). \tag{5.12}$$

In the same way, the voltage at the negative node can be expressed as

$$V_{outn} = V_{inn}\frac{C_s}{C_F} - \left(\frac{(15-N)C_s}{16C_F}V_{refp} + \frac{NC_s}{16C_F}V_{refn}\right). \tag{5.13}$$

Because the real output in the differential circuit is the difference between the positive node and negative node, the output of the fully differential subtractor/DAC is

$$V_{out} = V_{outp} - V_{outn} = V_{in}\frac{C_s}{C_F} - \left(\frac{NC_s}{16C_F}V_{ref} - \frac{(15-N)C_s}{16C_F}V_{ref}\right) \tag{5.14}$$

where $V_{in} = V_{inp} - V_{inn}$ and $V_{ref} = V_{refp} - V_{refn}$. The second and third terms in equation (5.14) express the output of the 4-bit DAC. Equation (5.14) reveals that the output range of the DAC is from $-15V_{ref}/16$ to $15V_{ref}/16$, two times bigger than that of the single-ended DAC.

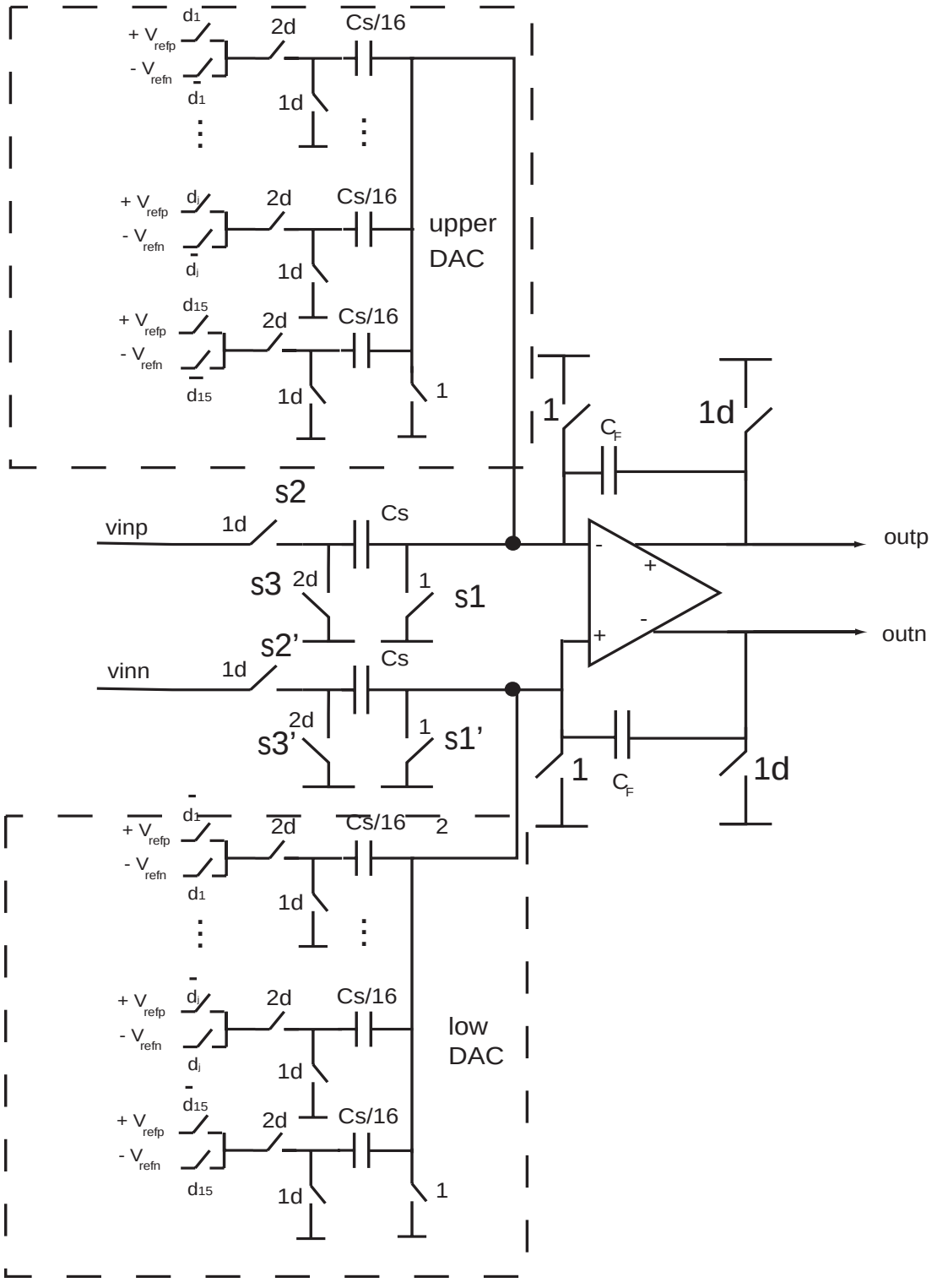

Figure 5.9 The schemtic of the subtractor/DAC

5.2 Integrator and Adder

The integrator and adder are the main parts of the sigma-delta modulator determining the transfer function of the quantization noise shaping. Similar to the subtractor discussed in the last section, the switched-capacitor circuits are used to implement both integrator and adder. Figure 5.10 shows the schematic of a fully differential integrator/DAC [20,30].

Controlled by two nonoverlapping clocks, the operation of the circuit in Figure 5.10 is divided into two stages: the sampling stage and integrating stage. In the sampling stage when clock 1 and 1d go high, one pair of the fully differential input signals (vin_p, vin_n) are sampled on two sampling capacitors, while the unit capacitors of the upper DAC are charged to the positive reference voltage and those in the low DAC are charged to the negative reference voltage. The charge in the feedback capacitors is unchanged because of the disconnection between the feedback capacitors and the sampling capacitors.

In the next integrating stage when clock 2 and 2d stay high, the two input capacitors are reset due to the virtual ground of the opamp while the unit-capacitors of the DAC are either connected to the positive input or the negative input of the opamp depending on the input digital code of the DAC. If the input digital code of DAC is N, N unit-capacitors in the upper the DAC will connect to the negative input of the opamp and the rest will connect to the positive input. In the low portion of the DAC, things are the opposite. N unit capacitors will connect to the positive input and the rest to the negative input.

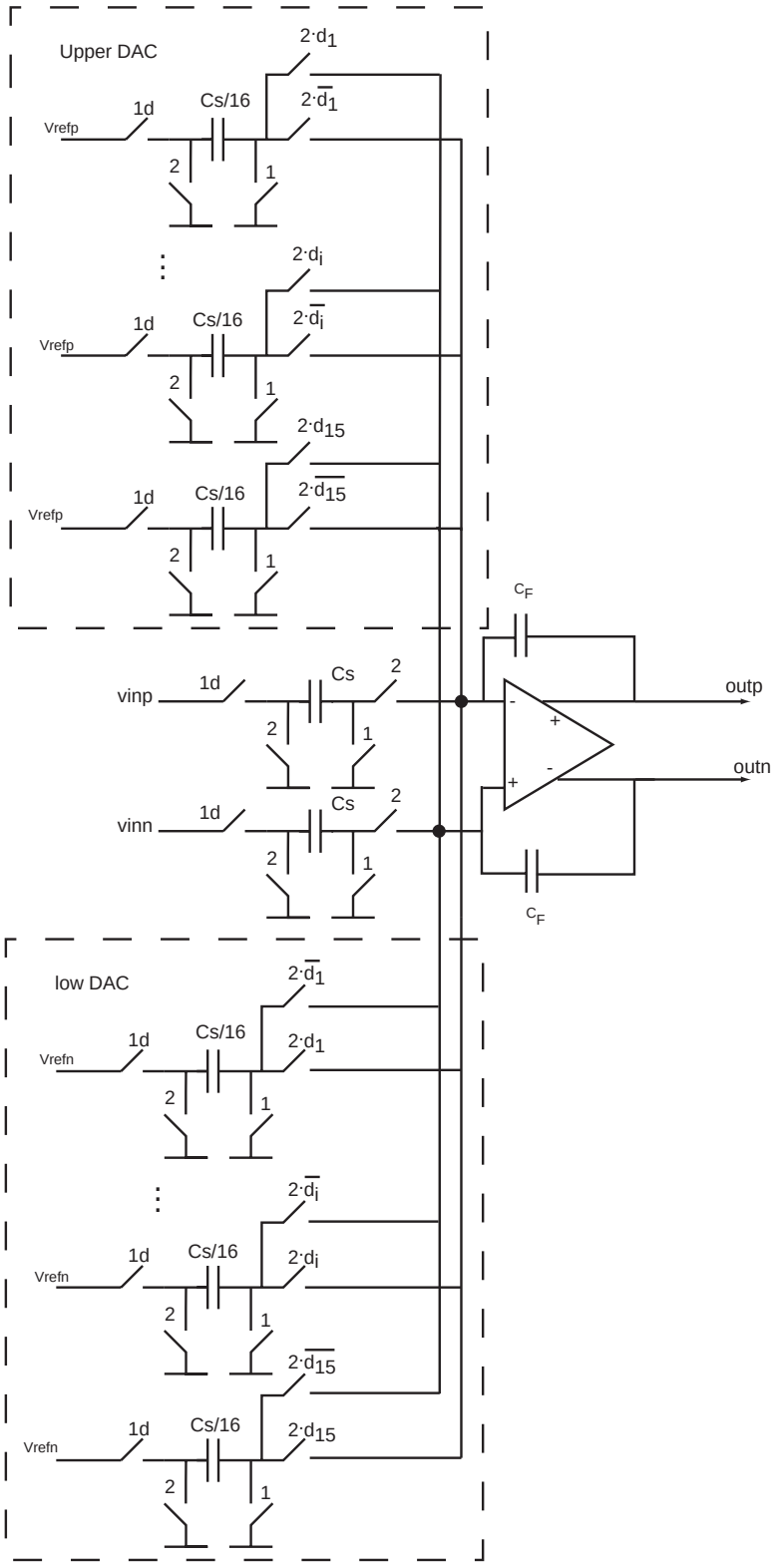

Figure 5.10 Block diagram of an integrator/DAC

When the switches separating the sampling capacitor and DAC from the feedback capacitors turn on, charge will be transferred from the sampling capacitors and DAC to the feedback capacitors resulting in the update of the integrator output. The voltage of the positive and negative nodes of integrator can be expressed as

$$V_{outp}(nT+T) = V_{outp}(nT) + V_{inp}(nT)\frac{C_s}{C_F} - \left(\frac{NC_s}{16C_F}V_{refp} + \frac{(15-N)C_s}{16C_F}V_{refn}\right) \quad (5.15)$$

and $$V_{outn}(nT+T) = V_{outp}(nT) + V_{inn}(nT)\frac{C_s}{C_F} - \left(\frac{(15-N)C_s}{16C_F}V_{refp} + \frac{NC_s}{16C_F}V_{refn}\right). \quad (5.16)$$

and the output of the integrator is the difference between these two nodes, which can be written as

$$V_{out} = V_{outp} - V_{outn} = V_{out}(nT) + V_{in}(nT)\frac{C_s}{C_F} - \left(\frac{NC_s}{16C_F}V_{ref} - \frac{(15-N)C_s}{16C_F}V_{ref}\right). \quad (5.17)$$

Equation (5.17) shows that the integrator gain is determined by the capacitor ratio between the input capacitor and the feedback capacitor, which can achieve very high accuracy in the integrated circuit.

Figure 5.10 shows only the block diagram of the coarse ADC, the fine ADC with same architecture as that of the coarse ADC also connects to the opamp in same way the coarse DAC does. Since the gain of the fine ADC is only one sixteenth of the coarse ADC, its gain and the reference voltage need to be four times smaller than that of the coarse ADC. Table 5.2 is the summary of the unit capacitor and reference voltage in both coarse and fine DACs.

Table 5.2 Summary of the coarse and fine DAC inside the integrator

DAC type	Unit capacitor	Positive Reference	Negative Reference	Fully differential reference
Coarse DAC	100fF	2.2v	0.2v	2v
Fine DAC	25fF	1.45v	0.95v	0.5v

To reduce the output swing of the second integrator, a short delay adder is inserted between the second integrator and the two-step ADC to add the system input to the output of the second integrator. Because the adder has no time delay in the signal path, it has to sample and add the output of the second integrator at the same time that the second integrator is integrating its input. Although both adder and the second integrator can operate simultaneously, the signal delay of the second integrator is not only determined by its settling time but also determined by the settling time of adder. So the adder needs to be very fast. Figure 5.11 shows the schematic of the short delay adder implemented with a switched-capacitor circuit [4]. Unlike the integrator, a very small value of the sampling capacitor can be chosen for the adder due to the much looser requirement on the mismatch and thermal noise. So the power dissipation of the adder is much less than that of the integrator even though it is two times faster than the integrator.

Controlled by two nonoverlapping clocks, the operation of the circuit in Figure 5.10 can also be divided into two stages: a sampling stage and an adding stage. During the sampling stage when clock 2 and 2d go high, one pair of the fully differential input signals(vinp, vinn) is sampled on two sampling capacitors, while another pair of capacitors and two feedback capacitors are reset. In the next adding stage when clock 1 and 1d stay high, two capacitors sampling two differential input signals are reset while

another pair of capacitors that were reset during the sampling stage are charged by two differential outputs of the second integrator.

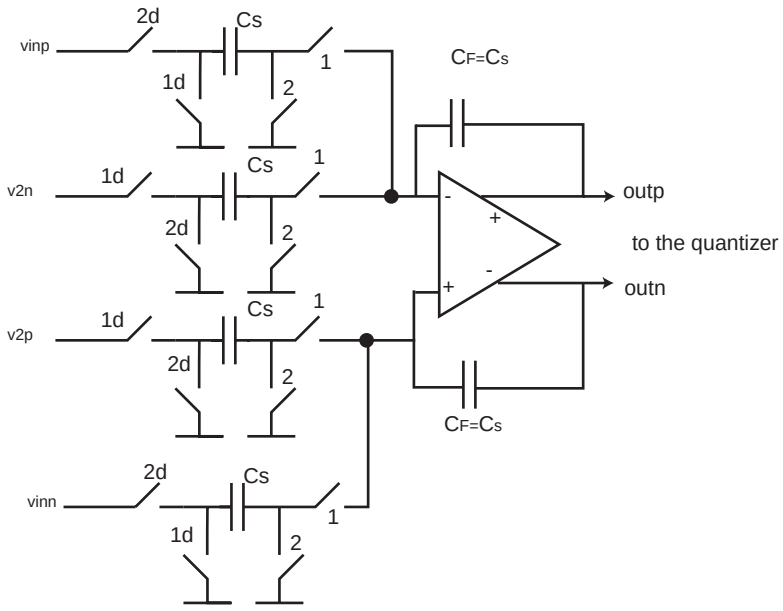

Figure 5.11 Block diagram of the adder

Because of the virtual ground and high impendence of the opamp inside the adder, the same method used to analyze the circuit of the integrator can also apply to the fully differential adder in Figure 5.11. According to the charge transfer equation, the total charge change of the two input capacitors connecting to vinp and v2n respectively equals the charge change of the feedback capacitor connecting to outp. So the voltage in the positive output node can be derived as

$$V_{outp} = V_{inp}\frac{C_s}{C_F} - V_{2n}\frac{C_s}{C_F} \quad . \tag{5.18}$$

In the same way, the voltage in the negative output node can be expressed as

$$V_{outn} = V_{inn}\frac{C_s}{C_F} - V_{2p}\frac{C_s}{C_F} \quad . \tag{5.19}$$

Thus the output of fully differential adder becomes

$$V_{out} = V_{outp} - V_{outn} = (V_{inp} - V_{inn})\frac{C_s}{C_F} + (V_{2p} - V_{2n})\frac{C_s}{C_F} = \frac{C_s}{C_F}(V_{in} + V_2) \tag{5.20}$$

where $V_{in} = V_{inp} - V_{inn}$ and $V_2 = V_{2p} - V_{2n}$. Equation (5.20) shows that if the feedback capacitor C_F equals the sampling capacitor $C_{s,}$ the output is simply the combination of the two inputs.

The block diagram of the overall system containing two integrators/DACs and an adder is shown in Figure 5.13. The overall timing diagram can be found in Figure 5.12. According to the timing diagram, first, the system input signal is sampled into the first integrator during phase 1 and then in phase 2, the first integrator integrates the difference between the sampling input and 8-bit DAC output. Also in phase 2, the second integrator samples the first integrator output and the system input. In the next phase 1, the second integrator adds two sampled signals together and then subtracts from the DAC output. Similar to the first integrator, the second integrator also integrates the difference signal to its last state. At the same time, the adder in the last stage adds the output of the second integrator to the system input. At the end of the next phase 1, the output of the adder will be ready for the two-step quanitzer in the next stage.

5.3 Opamp

The Opamp is the core of the switched-capacitor circuit determining its speed and power dissipation. Two types of opamps are used in this design based on the requirement of the output range. The telescopic architecture with small output range is chosen for the

opamp inside the integrator and subtractor while the opamp in the adder uses a folded-cascode to get a large output range.

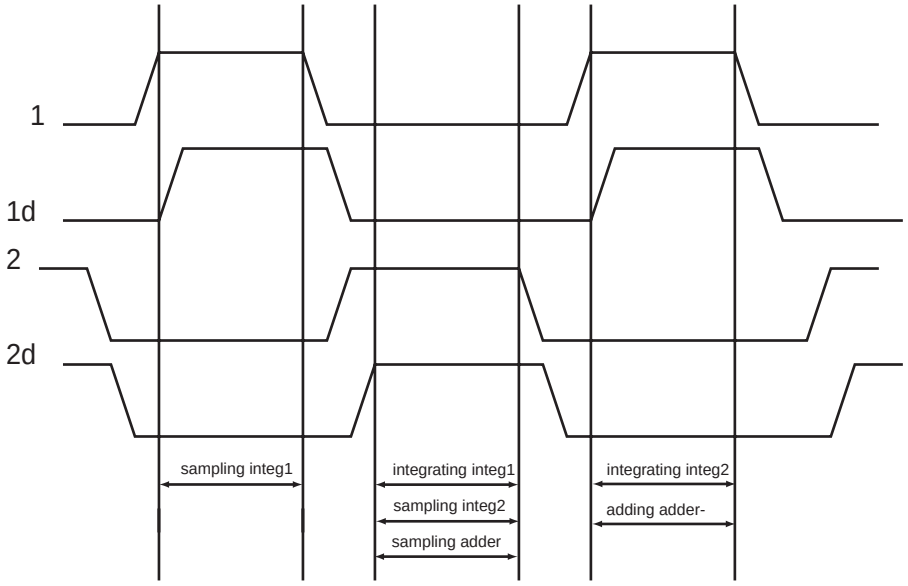

Figure 5.12 Overall timing diagram of the system

5.3.1 Telescopic Architecture

Although most of the single-stage opamps choose the folded-cascode architecture to obtain a large output swing, opamps in the subtractor and integrator use the telescopic architecture [4,28] to save power and get better phase margin. The schematic of the opamp is in Figure 5.13 where n-channel cascode transistors, NM4 and NM5 and p-channel cascode transistor, PM3 and PM4 are applied to increase the output impedance of the input differential pair and the current source load. The gain of opamp can be easily calculated as

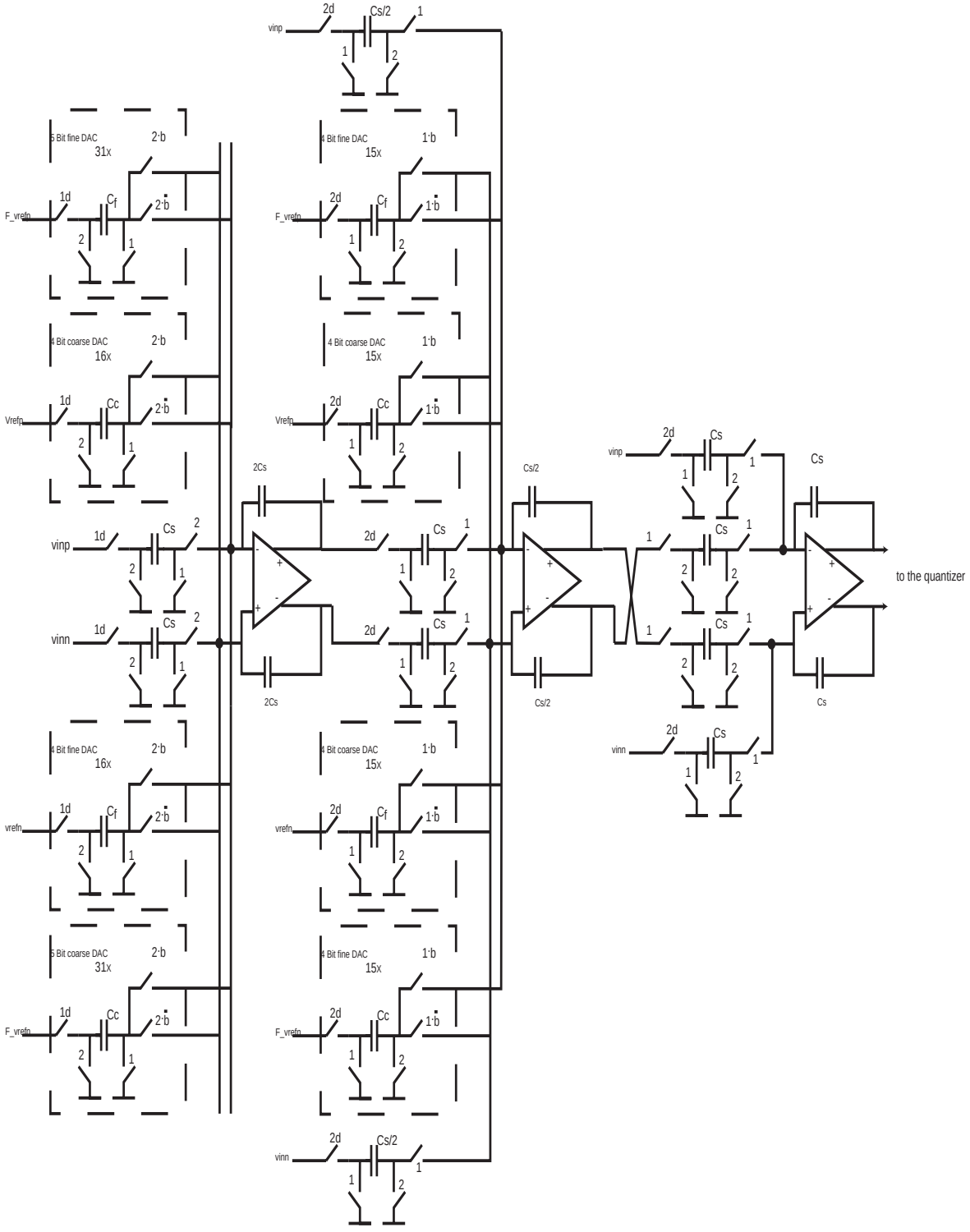

Figure 5.13 Block diagram of two integrators and adder

$$G = g_{mn1}.R_L = g_{mn1}.(r_{dsp3}r_{dsp1}g_{mp3} \,//\, r_{dsn4}r_{dsn1}g_{mn4}) \tag{5.21}$$

where R_L is the output impedance.

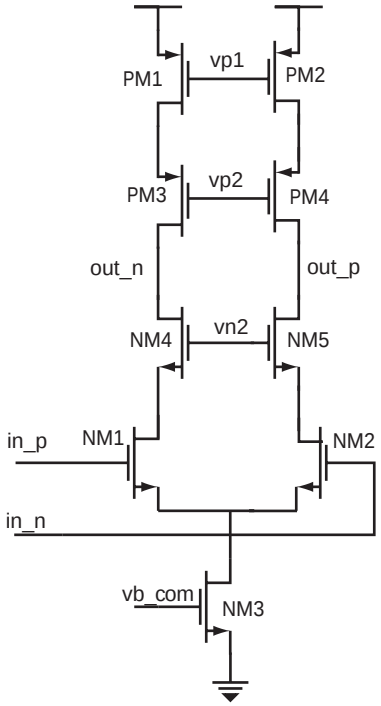

Figure 5.14 The schematic of telescopic opamp

Even though the opamp is basically a single gain stage, its gain can still reach 2000 because of the high output impedance. Another advantage of the single stage opamp is that only the output nodes have high impedance. The admittance seen at other nodes of the opamp is on the order of a transistor's transconductance, and thus they have relatively low impedance. By having all internal nodes of relatively low impedance, the speed of the opamp is maximized. The compensation of the opamp is achieved by the load capacitance because the high impedance output nodes create a dominant pole. Thus, as the load capacitance gets larger, the opamp usually becomes more stable but also slower.

The second poles of this opamp are primarily due to the time constants introduced by the impedance and parasitic capacitances at the sources of the p-channel cascode transistors, PM3 and PM4. The impedances at these nodes is given as

$$R_{sp3} = 1/g_{mp3} + R_L /(g_{mp3} r_{dsp3}). \tag{5.22}$$

At high frequency, this impedance reduces to $1/g_{mp3}$ because of the capacitive load at the output. The parasitic capacitance at the source nodes of the cascode transistors is primarily due to the gate-source capacitances of the cascode transistors as well as the drain-to-bulk capacitances of the current-source transistors PM1 and PM2. Comparing this with the parasitic capacitance created the second pole in the folded-cascode architecture, it does not include the drain-to-gate capacitances of the input transistors, and thus this telescopic opamp shows a better phase margin than its folded-cascode counterpart.

Another advantage of the telescopic opamp over the folded-cascode opamp is that the transconductance of the input differential pair is maximized because all the currents of opamp except bias circuit flow through the input differential pair while in the folded-cascode architecture part of the currents goes to the output branch. Although the telescopic opamp has a much smaller output swing, it is sufficient for the needs of the subtractor and integrator.

In the fully differential telescopic opamp of Figure 5.14, four different bias voltages are needed to put all the transistors of opamp into the active region. The bias circuit of the opamp can be found in Figure 5.15.

Transistors M9-M10 in Figure 5.15 form a special bias circuit called the “wide-swing cascode current mirror” [41.42] to provide two bias voltages vp1 and vp2 to the

current source transistors and the cascode transistors. The basic idea of this current mirror is to bias the drain-source voltages of transistors PM1 and PM3 to be close to the minimum possible without going into triode region. The configuration of M10 is similar to diode connection to provide the bias voltage to the current source. However, the gate of M10 connects to the drain of M11 to lower the drain-source voltage of M10. Therefore, it is matched to the drain-source voltage of PM1 and PM2.

To determine the bias voltage of V_{p2}, let V_{eff} be the effective gate-source voltage of M10. Ignoring the change of threshold, the gate voltage of M11 should equal $V_T + 2V_{eff}$ because M10 and M11 have the same size. Since V_{eff} is determined as

$$V_{eff} = \sqrt{\frac{2I_D}{uC_{ox}(W/L)}}, \tag{5.23}$$

doubling V_{eff} means reducing W/L four times. Considering body effect of MOSFET, the W/L of M8 is nearly five times smaller than that of M10.

Transistors from M1 to M9 form another "wide-swing cascade current mirror". To better match the differential amplifier circuit in Figure 5.14, M7 is added to the bias circuit to sink the current for the current mirror M1 and M2. Since the input range of two inputs of the opamp is rather narrow, their common-mode voltage vcom is applied to the gate of M5 to match the drain-source voltage of M7 in the bias circuit to that of NM3 of the opamp. Due to the body effect of M4, M5 and M6, the W/L of M6 is about six times smaller than that of M5. The minimum size transistor M3 is connected as a diode to prevent an incorrect stable state in which no current flow through the current mirror M1 and M2.

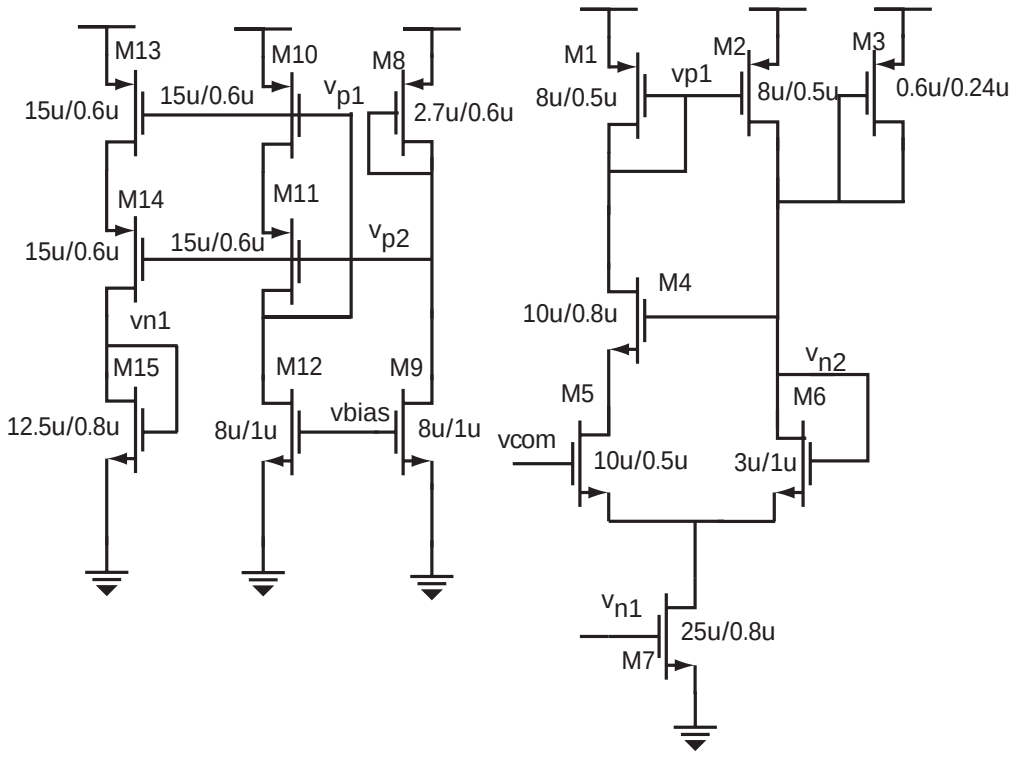

Figure 5.15 The schematic of bias circuit for the telescopic opamp

Table 5.3 is the performance summary of the opamps inside the subtractor and the integrator. It shows that the opamp has a large phase margin because the second pole is much higher than the dominant pole.

Table 5.3 The performance summary of the telescopic opamps

	Subtractor	Integrator
DC Gain	66 dB	70 dB
GBW	160 MHz	240 MHz
Phase Margin	61.6°	71°
Power dissipation	3 mW	17 mW

5.3.2 Folded-Cascode Architecture

To deal with the big output swing, the folded-cascode architecture [20, 24] in Figure 5.16 is chosen for the opamp inside the adder. The basic idea of the folded-cascode opamp is to apply cascode transistors to the input differential pair by using transistors opposite in type from those used in the input stage. Like the telescopic architecture, its DC gain can be expressed as

$$G = g_{mn1}.R_L = g_{mn1}.(r_{dsp3}r_{dsp1}g_{mp3} \,//\, r_{dsn4}r_{dsn6}g_{mn4}) . \tag{5.24}$$

The compensation is realized by the load capacitor, $C_{L,}$ thus, as the load capacitance gets larger, the opamp usually becomes more stable. The second poles of this opamp are primarily due to the time constants introduced by the impedance and parasitic capacitances at the sources of the p-channel cascode transistors, PM3 and PM4. The parasitic capacitance at the source nodes of the cascode transistors is primarily due to the gate-source capacitances of the cascode transistors as well as the drain-to-bulk capacitances of the current-source transistors PM1 and PM2 and input differential pair transistors NM1 and NM2. Compared to the parasitic capacitance creating the second pole in the telescopic architecture, this capacitance adds the drain-to-gate capacitances of the input transistors, and thus shows a slower speed than its telescopic counterpart.

Due to the existence of the input and output branches in the folded architecture, the input common-mode voltage has very limited effects on the output of the opamp. So the output swing of the fold-cascode opamp is much higher than that of the telescopic opamp. To get maximum output swing, two pairs of cascode transistors are biased with the wide-swing current mirror of Figure 5.17 and the output swing can be calculated as

$$V_{eff}^{N4} + V_{eff}^{N6} < V_{out} < V_{DD} - V_{eff}^{P1} - V_{eff}^{P3} \quad . \tag{5.25}$$

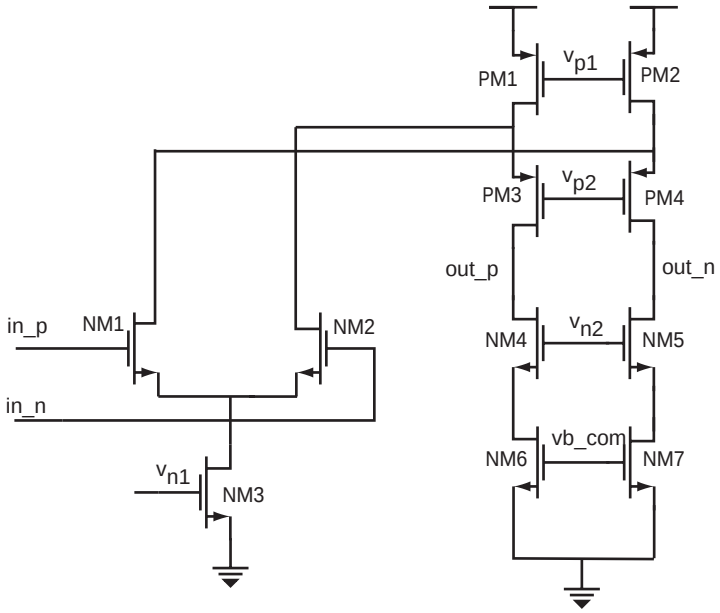

Figure 5.16 The schematic of the folded-cascode opamp

The bias circuit of Figure 5.17 is used to provide four bias voltages, V_{p1}, $V_{p2,}$ $V_{n1,}$ and V_{n2} to the fully differential opamp. Similar to the telescopic architecture, transistors M8-M12 in Figure 5.17 form a special bias circuit called the "wide-swing cascode current mirror" to provide two bias voltages V_{p1} and V_{p2} to the current source transistors and the cascode transistors

Table 5.4 is the performance summary of the folded-cascode opamp inside the adder. It shows that the opamp has greater power dissipation than its telescopic counterparts. This is because the folded-cascode architecture has two current branches (input and output branch) while the telescopic architecture only has one.

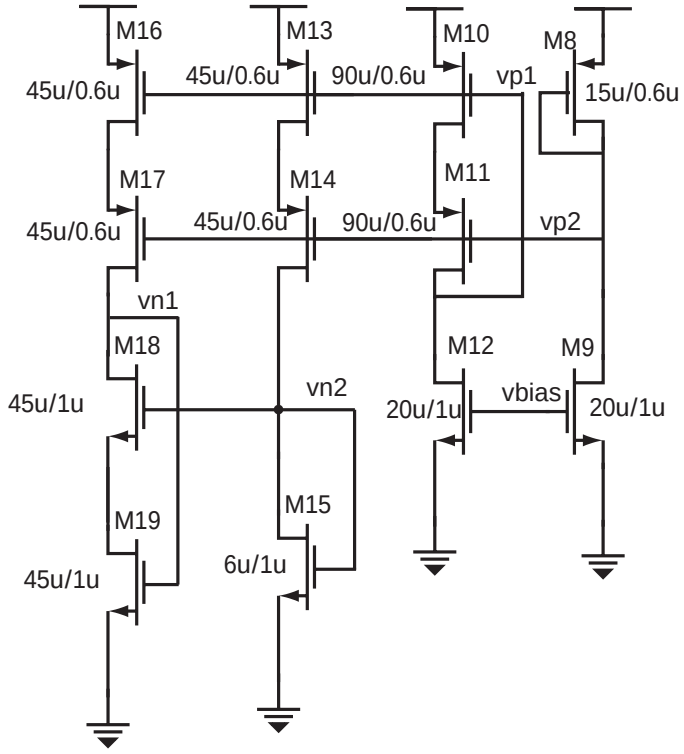

Figure 5.17 The bias-circuit of the folded-cascode opamp

5.3.3 Common-Mode Feedback

Since all opamps are in fully differential form, a special circuit called a common-mode feedback circuit is needed to set the output commom-mode voltage. To allow for the maximum output swing of the opamp, the commom-mode voltage usually is set halfway between the power-supply voltages and ground. Because all opamps in the system are part of the switched-capacitor circuit controlled by two nonoverlapping clocks, the switched-capacitor common-mode feedback circuit shown in Figure 5.18 is a reasonable choice [43,44].

In this circuit, the capacitors labeled Cc generate the average of two fully differential outputs of the opamp, Vp and Vn, which is used to create control voltages for the opamp current sources. The dc voltage across Cc is determined by capacitors Cs,

which are switched between bias voltages. This circuit acts much like a simple switched-capacitor low-pass filter having a dc input signal. The bias voltages are designed to be equal to the difference between the desired common-mode voltage and the desired control voltage used for the opamp current sources.

Table 5.4 The performance summary of the folded-cascode opamp

DC Gain	69 dB
GBW (load =9.2 pF)	131 MHz
Phase Margin	62°
Power dissipation	10 mW

The capacitors being switched, Cs, equal the nonswitched capacitors, Cc. Using larger capacitance values overloads the opamp more than necessary during the phase p1. Reducing the capacitors too much causes common-mode offset voltages due to charge injection of the switches. Normally, all of the switches would be realized by minimum-size n-channel transistors, except for the switches connected to the outputs, which might be realized by transmission gates to accommodate a wider signal swing.

Because the common-mode feedback circuit consists only of static components such as capacitors and switches, no limitation is imposed on the input range of the signal.

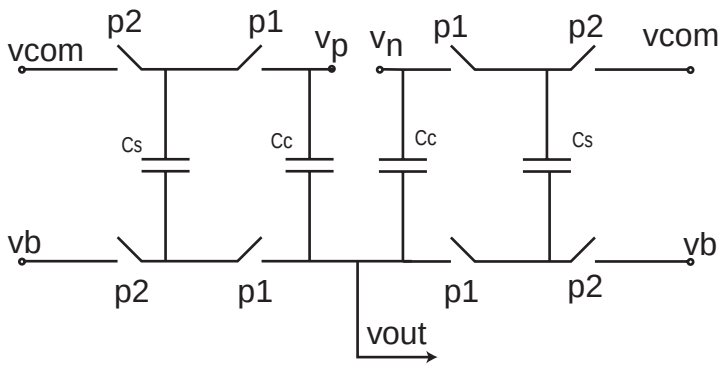

Figure 5.18 The schematic of the common-mode feedback circuit

5.4 Digital Circuitry

There are two types of digital blocks in the design. One is called the clock generator providing two nonoverlapping clocks to the system, another is called the digital feedback block digitally shaping the mismatch noise of the DACs.

5.4.1 Clock Generator

Since the Delta-Sigma Modulator is implemented with the switch capacitor circuit driven by two nonoverlapping clocks, the clock generator circuit must provide the different phases of clock signals from an external high-precision clock source.

The block diagram of the clock generator can be found in Figure 5.19. It consists of three parts: the waveform converter, the driving buffer and the delay circuit [45]. The waveform converter block first converts the waveform of the input clock from a sinusoid wave to a square wave. Then the clock signals pass through delay blocks to generate the delayed clock. Finally all of the clock signals go through driving buffers to obtain large driving capacity.

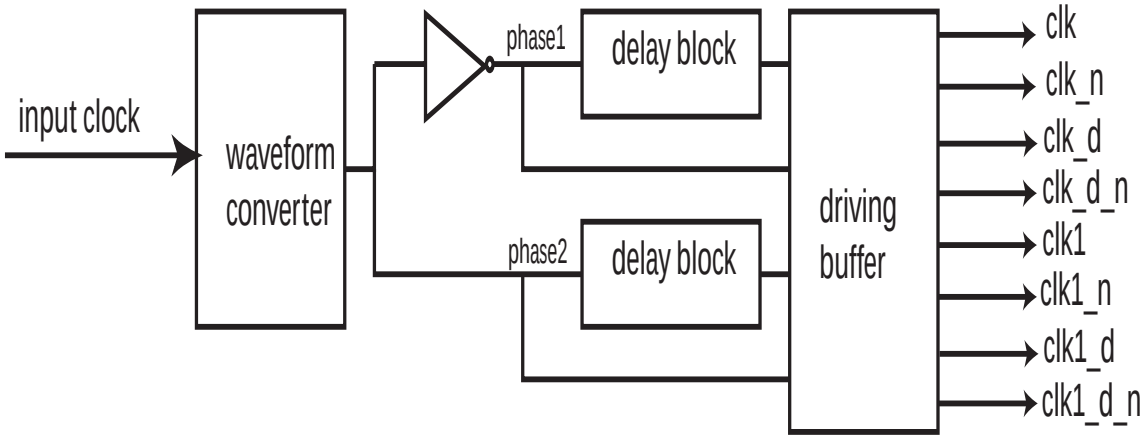

Figure 5.19 Block diagram of the clock generator circuit

The waveform converter consists of two cascaded D flip-flops as shown in Figure 5.20. The reset signal goes high to reset all the inner states of the two flip-flops. Because the output of the converter connects to the negative output of the D flip-flop, its value is zero while the output of the first flip-flop is one. Then the reset signal goes low leaving the two flip-flops into normal mode. After one clock cycle, the output of the second flip-flop shifts to the output of the first flip-flop while the output of the first flip-flop shifts to the negative output of the second flip-flop causing the state transition of the converter output. This process of state change occurs for every clock cycle, generating 50% duty cycle clock signal with a square waveform. Since the state transition of the output clock occurs every input clock cycle, the frequency of the output clock is decreased by half.

5.4.2 Digital Feedback Block

The digital feedback block providing the thermometer code to the DACs is used to digitally filter the mismatch noise of the DACs. It includes the REQ, DEM and some encoder and decoder circuits. Figure 5.21 shows the diagram of the digital block. The

input signal coming from coarse and fine ADCs pass through the binary encoder to convert to a binary code. Then it passes through the REQ block to generate new coarse and fine bits. After that, it goes through the thermometer encoder to convert the coarse and fine bits to the thermometer code. Finally the coarse and fine bits pass through coarse and fine DEM respectively before getting to the coarse and fine DACs. The total delay of the digital feedback block is 8ns because the highest sampling frequency is 50 MHz. This restraint is not very difficult to satisfy in a 0.25 μm process.

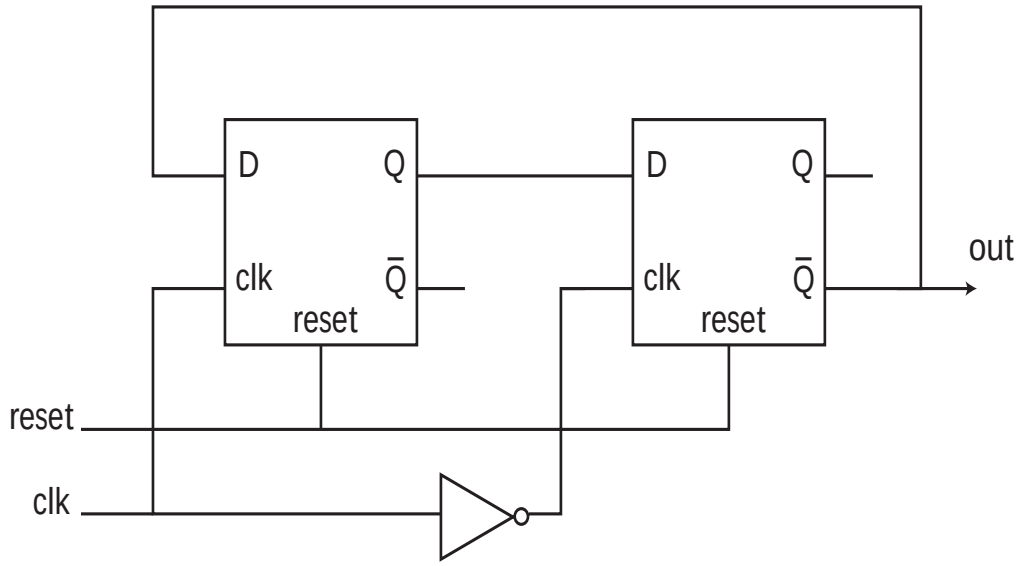

Figure 5.20 Block diagram of the waveform converter circuit

5.4.2.1 REQ Block

The REQ circuit shown in Figure 5.22 consists of two 8-bit adders and one 4-bit register. The 8-bit binary input is added to the output of a 4-bit register storing the 4-bit fine bits of the last clock cycle. The four-bit coarse output of the REQ comes from four MSBs of the 8-bit adder output. The rest of the bits are obtained by subtracting the 8-bit

input signal from the 8-bit coarse signal generated by shifting four coarse output bits to the left by four bits.

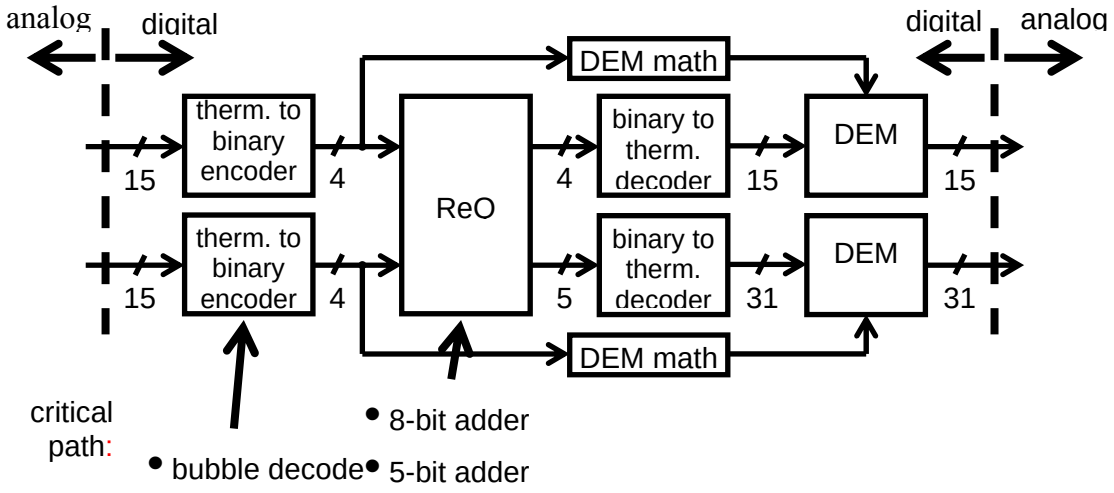

Figure 5.21 Block diagram of the digital circuit

The eight-bit adder and subtractor inside the REQ circuit are realized by cascading eight full-adders, connecting $C_{o,k-1}$ to $C_{i,k}$. This cascading architecture known as a ripple-carry adder is shown in Figure 5.23. Since the propagation delay of a ripple adder is input dependent, its maximum delay is determined by the worst-case delay occurring when a carry bit generated at the least significant bit position propagates all the way to the most significant bit.

The carry and sum circuit of a full adder is shown in Figure 5.24. The pull up and pull down circuits in Figure 5.24 are completely symmetrical, which guarantees identical rise and fall transitions if the NMOS and PMOS devices are properly sized. Two series transistors appear in the carry-generation circuitry.

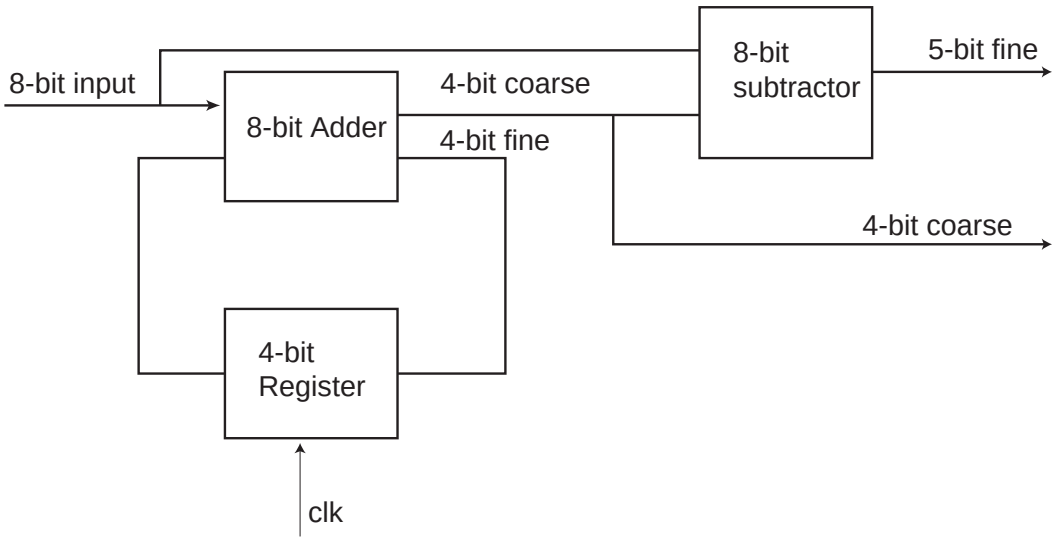

Figure 5.22 Block diagram of REQ circuit

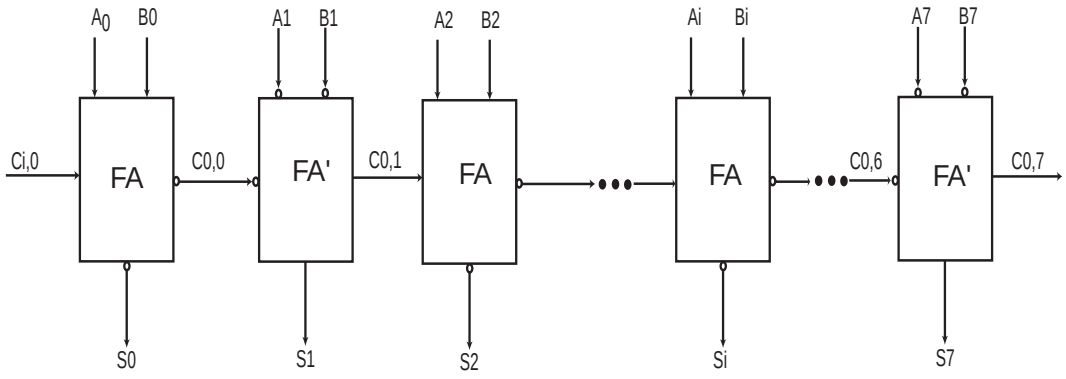

Figure 5.23 Block diagram of 8-bit ripple adder

Since the output of the carry circuit is the inverted version of Co and the input of the carry circuit is Ci, an inverter is needed to reverse the output of the carry circuit before feeding to the next stage. To reduce the delay of the extra inverter in the carry circuit, an inverted version of the full adder denoted as FA' is used in Figure 5.23, where

all three inputs are inverted. Because the input of the carry circuit of FA' is the inverted version of Ci, the output of FA in the previous stage can connects directly to it.

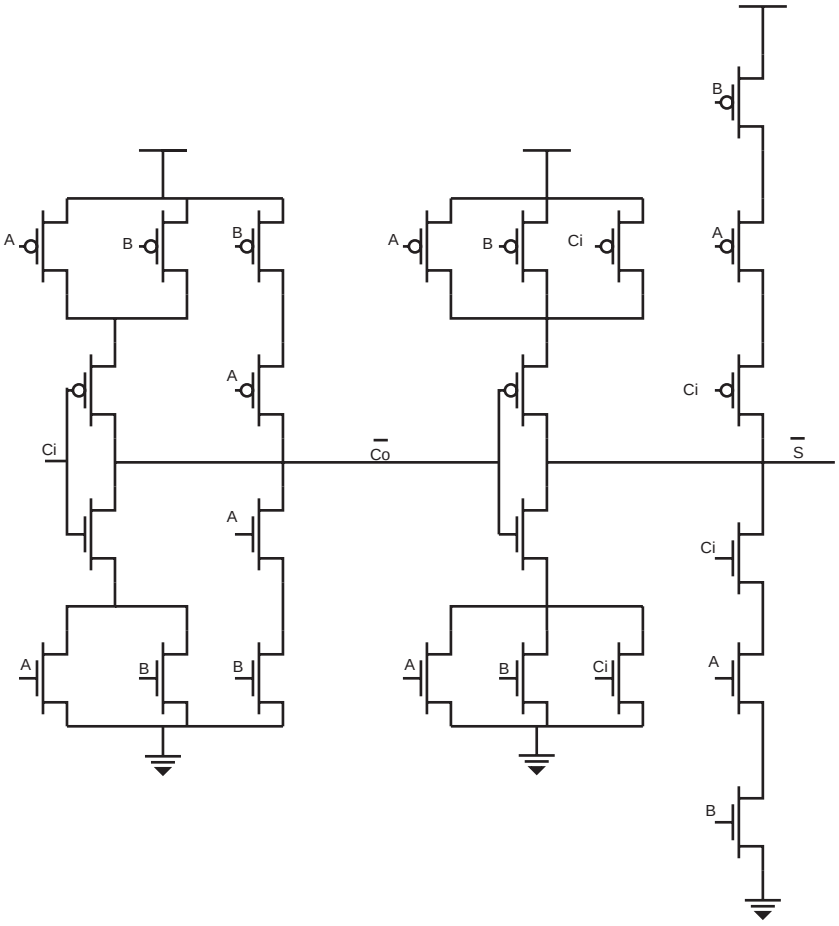

Figure 5.24 Schematic of one-bit fully adder

Because the two nonoverlapping clocks are available in the chip, D registers with two cascade D-latches and two nonoverlapping clocks in Figure 5.25 are chosen for all the registers in the chip. The nonoverlapping clocks p1 and p2 avoid a race condition that could occurr when both p1 and p2 are high and input D propagates into the second stage.

Two positive feedback branches in the circuit are used to sustain the state of the register and avoid the state loss caused by the leakage of the pn junction.

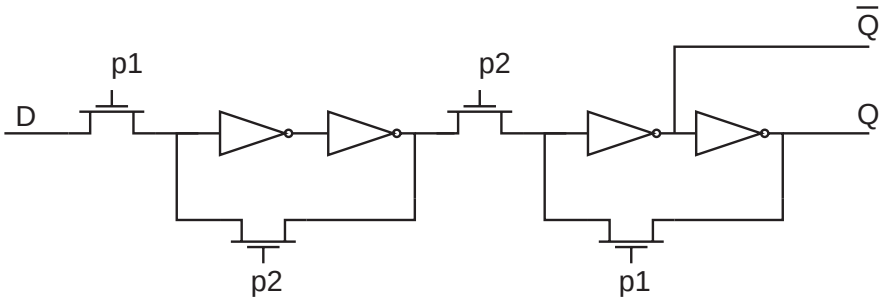

Figure 5.25 Schematic of D-register

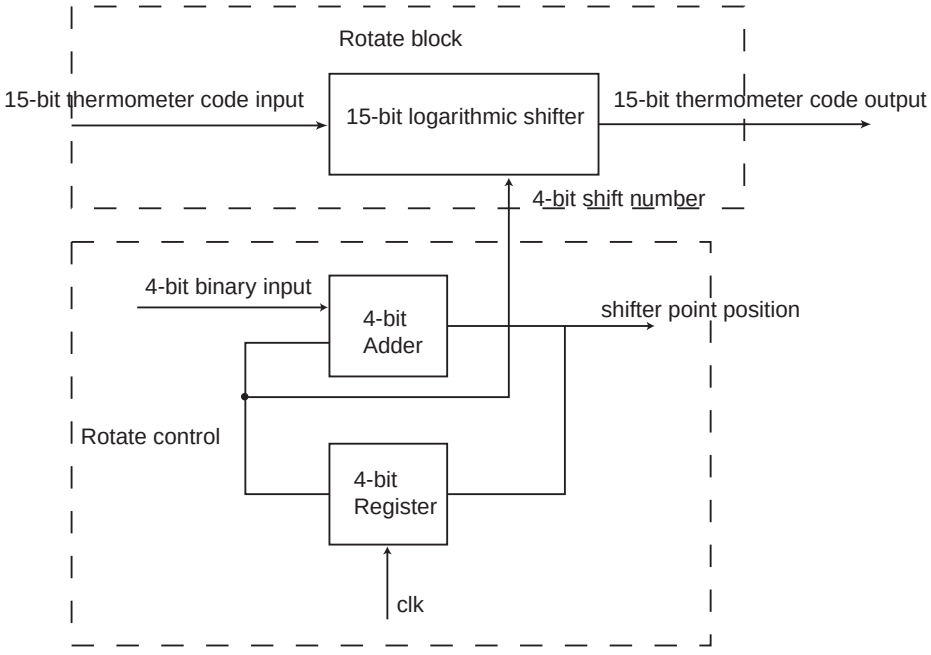

Figure 5.26 Block diagram of the DEM circuit

5.4.2.2 DEM Block

The block diagram of the DEM block is shown in Figure 5.26. It includes two parts: the logarithmic shifter and the shifter control. The shifter control accepts the binary input from the REQ block and adds it to the current pointer stored in the 4-bit register. Because the sum in the 4-bit adder is not immediately used to control the shifter, the delay of adder does not contribute to the total delay of the digital block.

5.5 Floor plan and layout design

5.5.1 Floor plan

The proposed design prototype is implemented by the TSMC 0.25 μm process. In mixed-signal physical implementations, it is important to minimize the impacts of any parasitic, mismatch, and noise. Special attention needs to be paid to the noise coupling from the digital circuit to the sensitive analog circuit since both digital and analog circuit share the same substrate. Hence several approaches are taken below to reduce the noise coupling of the digital circuit.

- Separation of supply voltage is used for the digital and analog circuits and they are designated as VDD, GND ,VCC, and VSS respectively.
- Guard ring is employed to isolate the analog circuit from the substrate noise produced by the digital circuit.
- Shielding is used to protect sensitive lines such as the modulator input and reference voltages. This technique surrounds the net with a grounded metal layer.
- Symmetrical layout is used for analog circuits.

Figure 5.27 depicts the layout floor plan for the proposed sigma-delta modulator. The noisy digital part of the chip and clock generator, is placed at the top. To reduce its interference with other circuits, the most sensitive analog circuits such as the integrators and the adder are placed at the bottom. The digital feedback block including DEM/REQ is placed adjacent to the clock generator. All the capacitors of the DACs are put in a capacitor array to reduce the mismatch. Also the integrators, adder, and subtractor are placed together to reduce the parasitic capacitors caused by the wire routing.

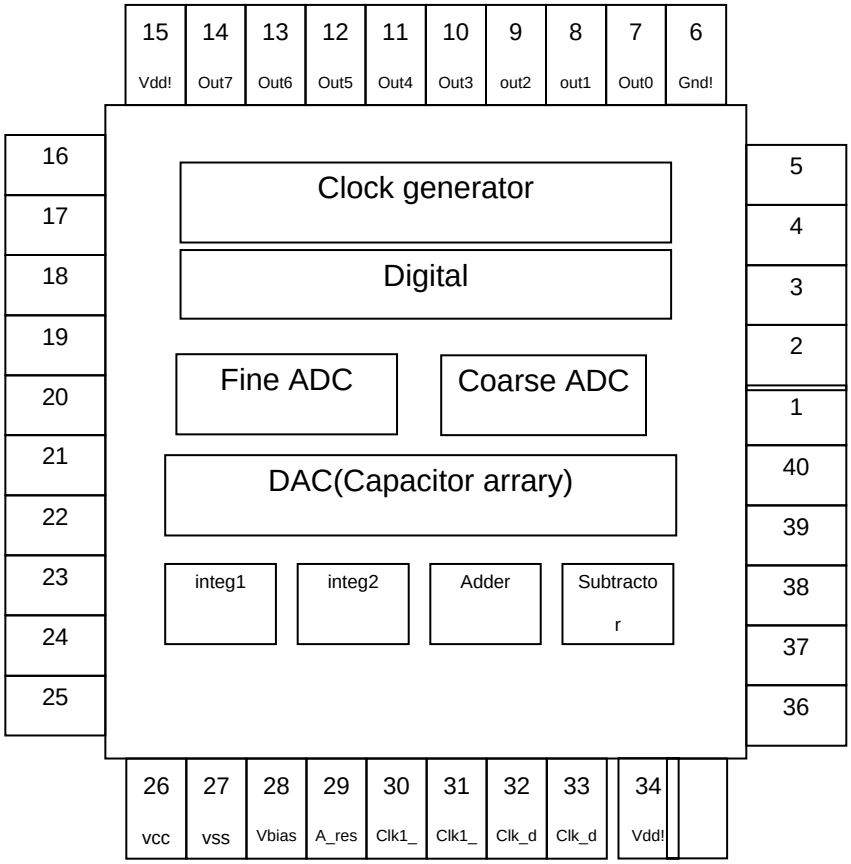

Figure 5.27 Floor-plan of the chip

5.5.2 Layout Design

Figure 5.28 shows the layout design of the comparator. Since the comparator includes both analog and digital circuits, the separate power supply and ground are needed in the layout to prevent noise coupling from the common power signals. The capacitor array with a width of 50 μm is used to separate the analog preamplifiers with all other digital circuits including the latch and R-S latch.

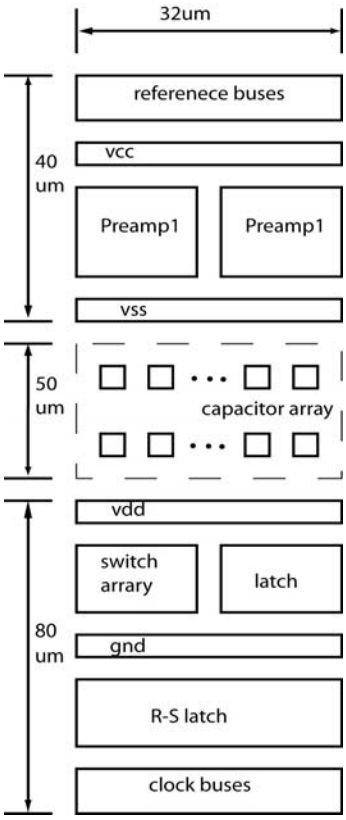

Figure 5.28 The diagram of the layout design of the comparator

Both analog and digital circuits are placed between the power and ground wires to get easy access to power supply and ground. The reference buses are placed at the top to reduce noise coupling from the noisy clock buses at the bottom. Because all the buses in

Figure 5.28 are placed horizontally, it is very easy to abut the comparators to form the coarse/fine comparator array for the coarse/fine ADC. Each comparator in the array shares the same buses to improve the match of different comparators.

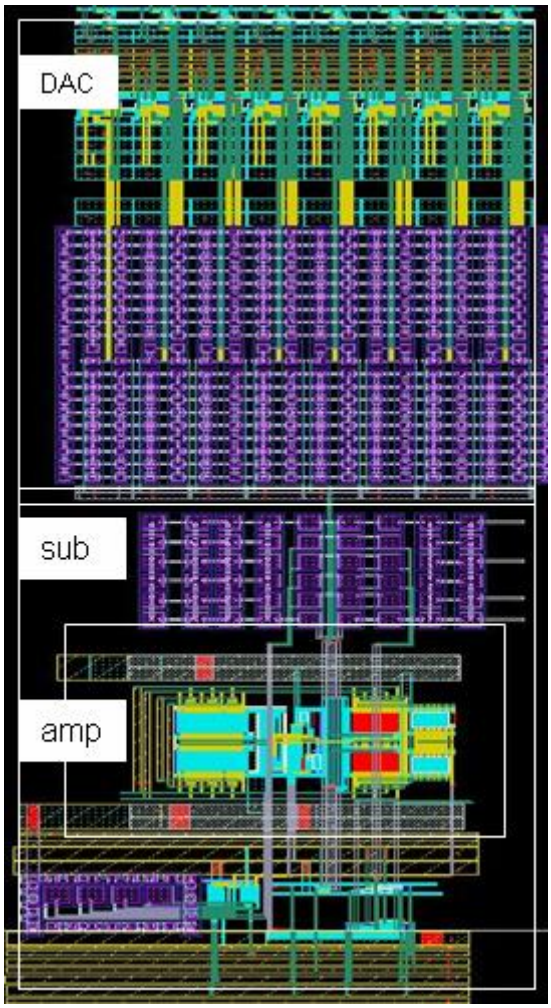

Figure 5.29 The layout of the Subtractor/DAC

Figure 5.29 shows the layout of the subtractor/DAC. Since the clock bus has the largest digital noise than all other digital signal wires, this bus is placed at the bottom to reduce the inferences to the sensitive analog circuits. Because the subtractor uses fully

differential architecture to increase its common-mode noise rejection, it is important to route all these fully differential signals next to each other to take advantage of the differential architecture.

Based on the layout floor plan, Figure 5.30 shows the layout of the whole chip. The dimension for this chip is 3.3 mm X 3.3 mm and the core circuit inside the chip is 1.6mmX1.6mm. The total chip includes 12,000 MOS transistors, 3,000 MIM capacitors and 400 poly resistors.

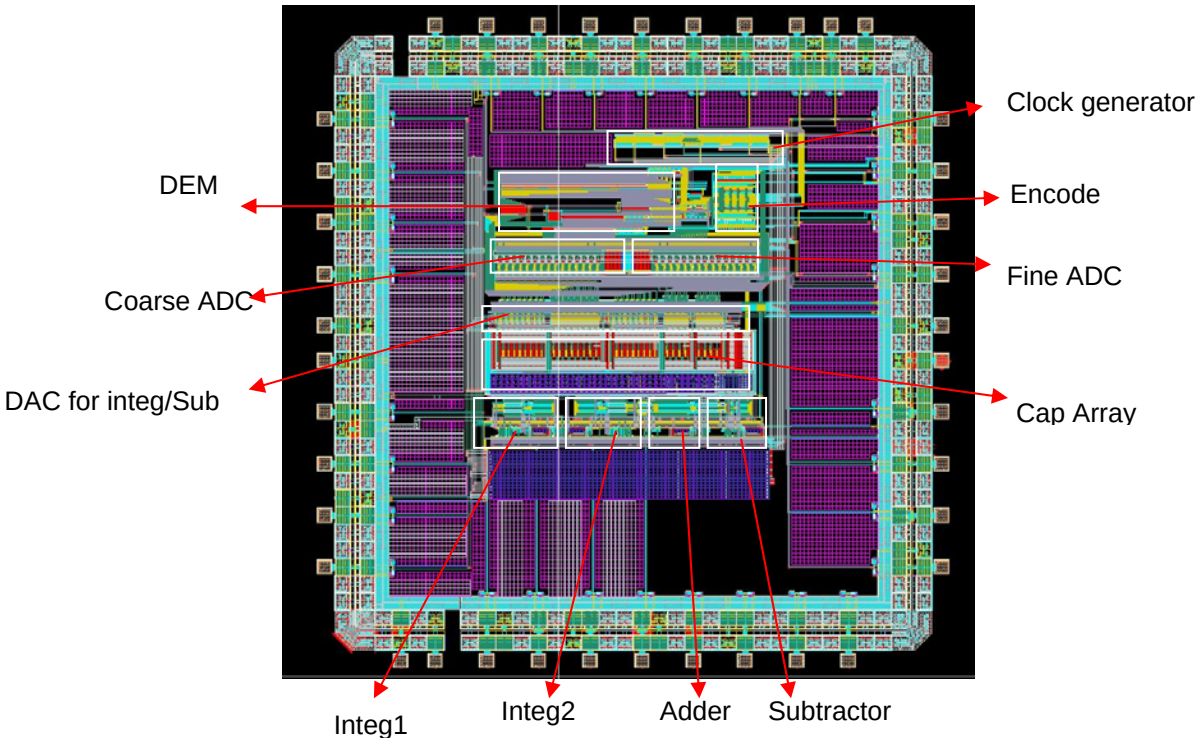

Figure 5.30 The layout of the whole chip

6 Experimental Results

The measurement of high resolution converters requires a specific measurement setup to create an interference-free environment. Because of this, the test set-up together with the equipment needed is described in detail. Afterwards, the dynamic testing results of the ADC are presented. Finally, we include a summary of the ADC performance.

6.1 Test Setup

Figure 6.1 represents the configuration used to evaluate the ADC performance. An arbitrary waveform generator (Agilent 33250A) and high precision sine wave generator (B&K 1051) are used to generate the clock signal and input signal respectively. The ADC, mounted on a testing printed board, receives the clock signal and input signal from the signal generator block. The samples at the ADC output are captured at the clock rate by the logic analyzer (HP 16700A) and transferred to the PC for post-processing using Matlab.

6.2 Printed Board and Environment Features

Special precautions are required in the design of the testing board. First, a differential input is required to have higher resolution than the specification of the tested chip. Also low noise, low impedance voltage buffers are needed on the testing board to

provide the high precision reference voltages to the chip. The basic requirement on the design of the testing board is that the noise contribution from the testing board must be low enough so that it does not affect the performance of the tested chip.

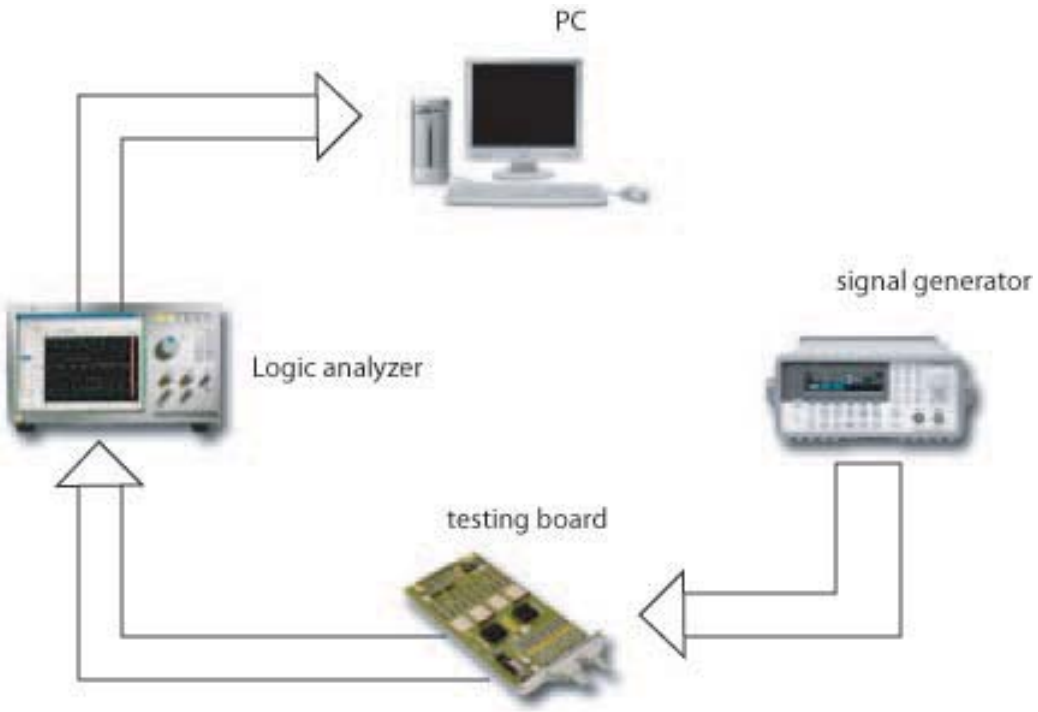

Figure 6.1 Measurement configuration

The schematic of the differential input generator circuit is shown in Figure 6.2, where TI 4141, the fully differential amplifier, is configured to convert the single-ended input to a fully differential output. A high precision, low distortion, sine wave generator (B&K 1051) is used to provide the pure sinusoid at input that is terminated by a 50 Ω resistor. The resistor R3 at the negative input node of the amplifier is to balance the parallel impedance of the 50 Ω source termination. The positive and negative differential outputs of TI4141 are connected to the respective differential inputs of the tested chip via

a pair of 50 Ω resistors. The input common-mode voltage signal vcom is bypassed by a 0.1 μF capacitor.

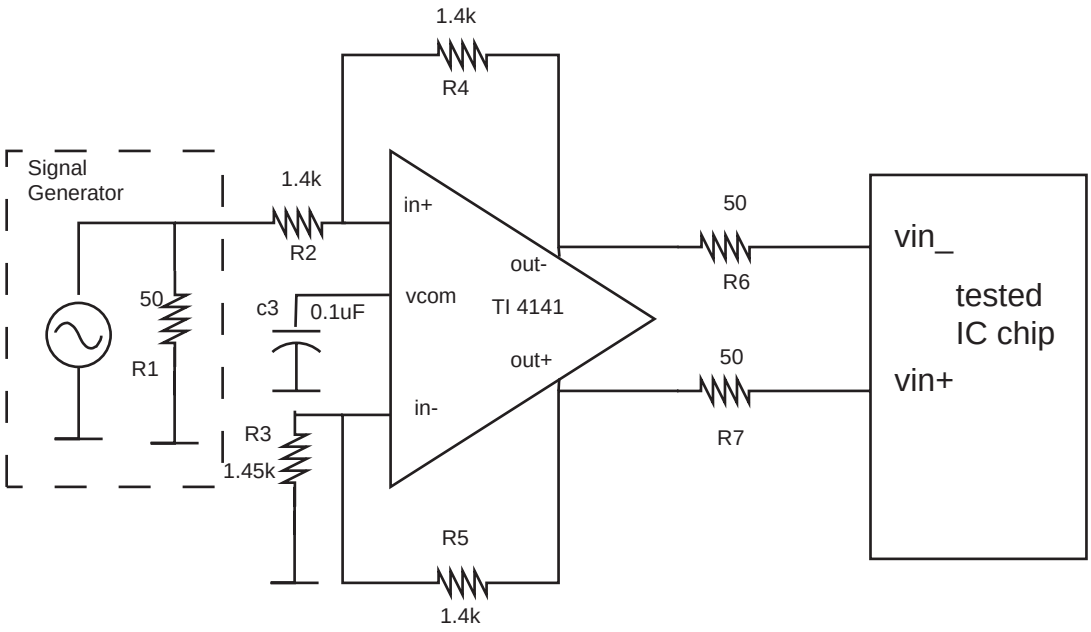

Figure 6.2 Schematic of the differential inputs generator

The resistor voltage divider and the following voltage buffer circuit are depicted in Figure 6.3. During the test, the potentiometer R2 is adjusted carefully to generate the exact voltage needed. This voltage is then buffered by a low-noise voltage buffer based on a low-noise, high-precision operational amplifier (MAX410). The opamp, MAX410 has noise power density of 2.4 nV / $\sqrt{\text{HZ}}$ and an offset voltage of 240 μV. It is powered by the positive and negative 5 V supplies bypassed with 0.1μF capacitors. The required clock signal is derived from the external arbitrary waveform generator, Agilent 33250A. The output data is stored in the logic analyzer and then transferred to a PC for performing Fast Fourier Transform (FFT).

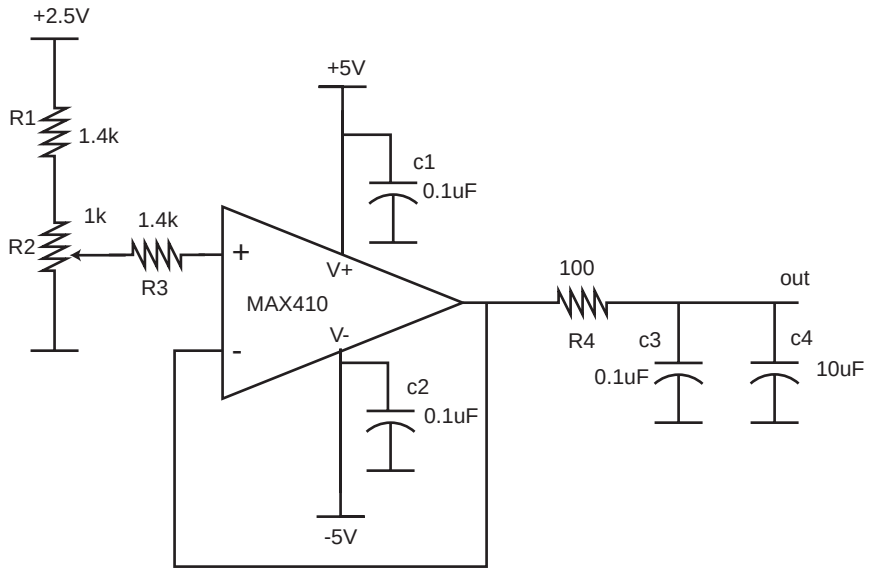

Figure 6.3 Schematic of the voltage buffer

A good testing board not only depends on the schematic design but also on the layout design. There are three electromagnetic coupling mechanisms on the testing board leading to inference in the testing system. They are as follow:

- Direct coupling, generated by the presence of undesired currents in the ground plane or in certain return lines. This type of coupling is responsible for most of the switching noise presented in the analog lines.
- Inductive coupling, caused by magnetic fields that induce noisy current in the signal traces. The magnitude of noise grows with the circuit loop area and with the proximity to the magnetic field source.
- Capacitive coupling, produced by parasitic capacitors which grow as the distance between lines is reduced.

- Due to these coupling mechanisms, the reference voltages and the power supplies on the testing board include not only the DC component but also the harmonic distortions of the clock signal. This high frequency interference could be modulated with each other and eventually appear in the signal band.

To reduce the interference, each of the reference voltages and power supplies is bypassed by two decoupling capacitors of 100 pF and 1μF. Each of these decoupling capacitors should be placed close to their respective pins of the chip during the layout design. In addition to the bypass capacitors, an inductor is put between the decoupling capacitors and the pin of the chip to further reduce high frequency interference.

Figure 6.4 shows the part of the testing board where two techniques are used to ensure the stability of the power supplies. The same method also applies to the reference voltage. The photograph of the four-layer testing board is shown in Figure 6.5 where separate power and ground planes are used to reduce direct coupling from the power supplies.

6.3 Test Results

The supply voltage of the tested chip is 2.5V and the power consumption of the chip is 120 mW at 4 MHz clock frequency. The input signal is a tone with variable amplitude and frequency in the base band of the modulator, generated from the high precision sine wave generator (B&K 1051). To ensure the input signal is band limited, a first-order low-pass filter is put on the testing board just before the input signal enters the chip to avoid aliasing.

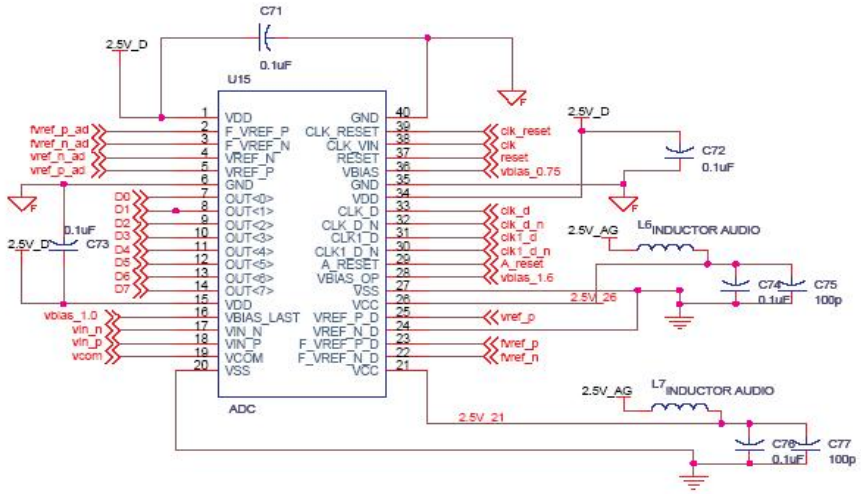

Figure 6.4 Part of the testing board

The performance of the converter can be characterized by a signal-to-noise-plus distortion ratio (SNDR) measurement. The SNDR is defined as the ratio of the signal power to all other noise and harmonic power in the digital output stream. The peak SNDR is called the dynamic range defined as the difference between the largest signal and the smallest detectable signal in dB.

In the testing, the clock frequency is set to be 4 MHz and the input signal has a frequency of 8 kHz and an amplitude of -5 dB relative to full scale. To evaluate the power spectrum, 8,000 consecutive samples are collected from the ADC output using the logic analyzer (16700A), while the amplitude and the frequency of the input are maintained constant. Once transferred into the PC, each data series is processed off-line with a dedicated MATLAB program, performing FFT with a hanning window.

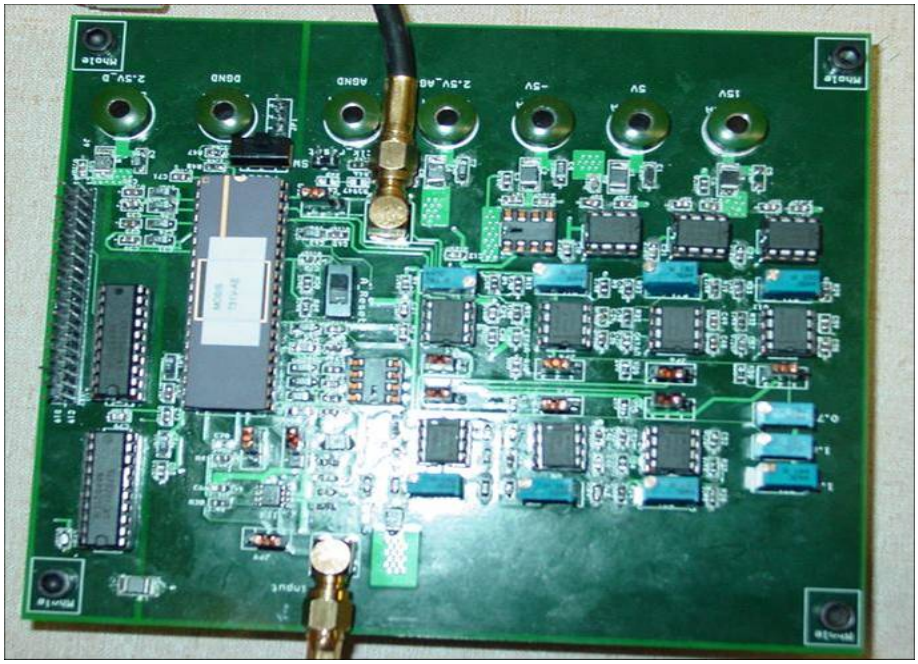

Figure 6.5 The picture of the testing board

The performance of the 8-bit two-step inner quanitzer can be measured simply by resetting all the integrators. Figure 6.6 shows the measured output spectrum of the 8-bit two-step inner quantizer at a sampling frequency of 4 MHz. Due to the mismatch of the comparators and other source of distortion, the two-step quantizer achieve a peak SNDR of 42.5 dB, which is equivalent to 6.7-bit resolution.

The output spectrum in Figure 6.8 demonstrates that the uncompensated coarse quantization noise caused by the mismatch of coarse and fine DACs can be greatly reduced with the requantization algorithm. The application of the requantization algorithm makes it possible to apply the large bit inner quantization inside the sigma-delta modulator. The effectiveness of the requantization method is also shown in Table 6.1 where the performances with or without requantization method are compared with each other.

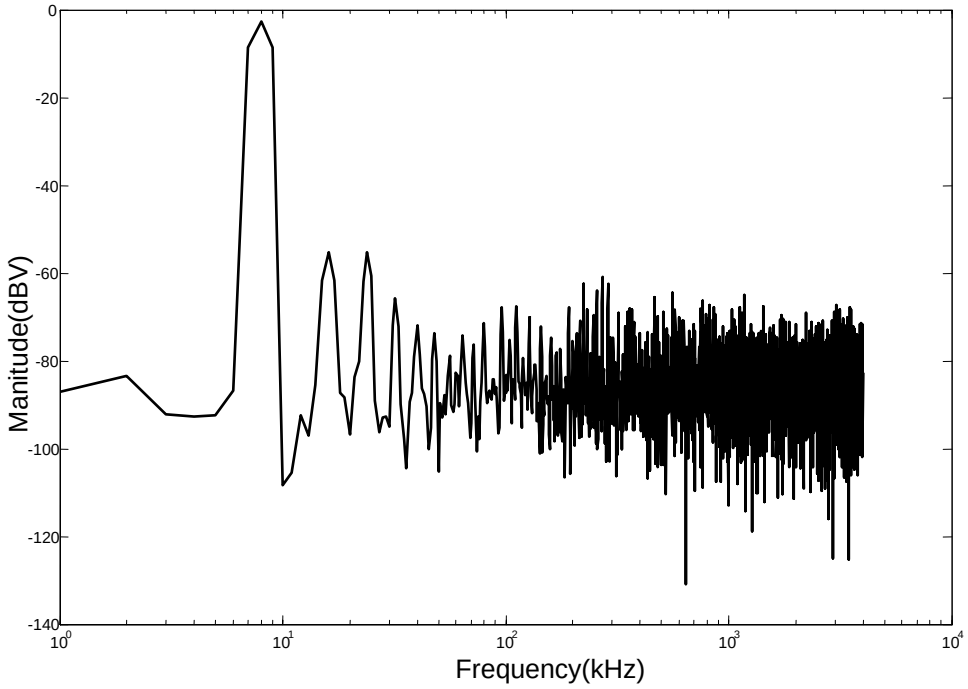

Figure 6.6 The power spectrum of the two-step 8-bit inner quantizer

For the common multibit sigma-delta ADC, the dominant noise source in the signal band is the thermal noise because the quantization noise has been shaped by the modulator. However, in the proposed system where coarse and fine DAC are combined together to form the DAC output, the dominant noise source in the signal band can still be the quantization noise if no requantization algorithm is used as shown in Figure 6.7. This is because the mismatch between 4-bit coarse DAC and 4-bit fine DAC can cause incomplete cancellation of the coarse quantization noise, which in turn leaks into the system output and raises the noise floor of the signal band.

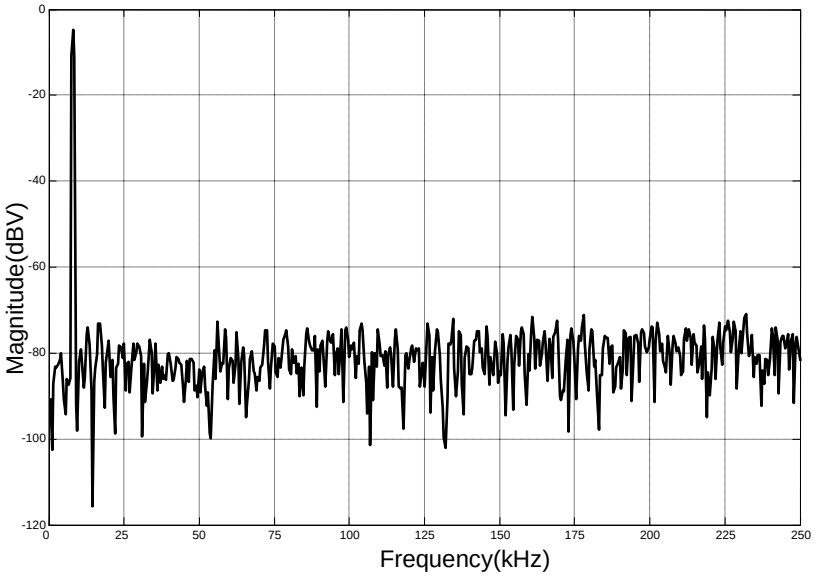

Figure 6.7 The output spectrum without digital requantization algorithm

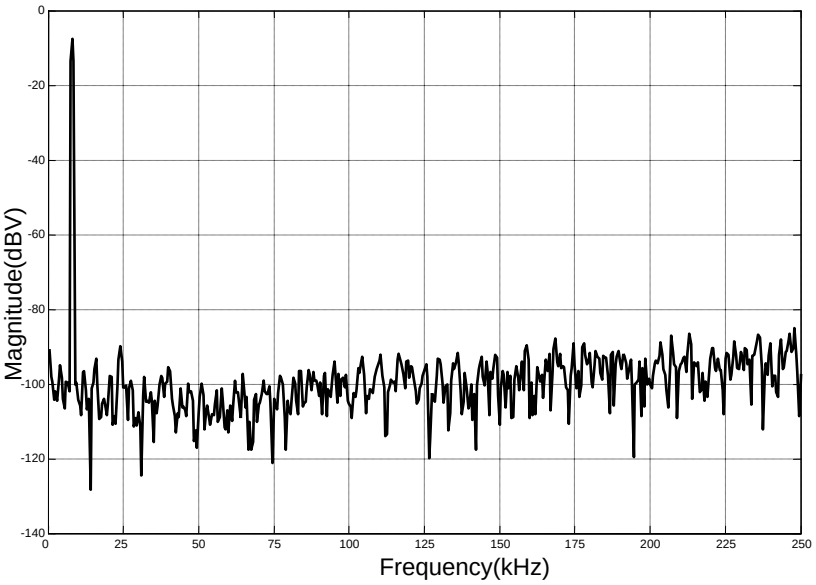

Figure 6.8 The output spectrum with digital requantization algorithm

Table 6.1 The performance comparison with or without the requantization algorithm

	Noise floor	Dynamic Range (OSR=8)	Dynamic Range (OSR=16)
Without requantization	80 dB	49 dB	53 dB
With requantization	100 dB	63 dB	70 dB

Table 6.2 Summary of the measured system

SNDR(OSR=8)	63 dB
SNDR(OSR = 16)	70 dB
Sampling frequency	4 MHz
Input range	2 V
Power supply	2.5 V
Power dissipation	120 mW
Input capacitance	1.6 pF
Active area	3 mm^2
Technology	TSMC 0.25 μm

Table 6.2 is the performance summary of the measured system. The measured system showed a maximum SNDR of 70 dB with a signal bandwidth of 250 kHz, which is much below the design target and system simulation results. Several factors may degrade the performance of the tested system.

1. As can be seen in the oscilloscope, the reference voltage of the coarse DAC has more than 100 ns settling time, which prevents the further increase of the sampling clock frequency.
2. The equivalent bit of less than seven in the two-step inner quantizer suggests that the offsets of the comparators and the subtractor are not as good as expected.
3. The undesired coupling between the analog and the digital circuits in the chip as shown from the waveform of the analog ground in the oscilloscope, which adds the noise to the sensitive analog circuit.
4. The clock timing skew and mismatch of the parasitics are also limiting factors, which can cause the incomplete cancellation of the charge injection error during the integration and the subtraction.
5. The mismatch of the capacitors has a larger impact than expected. It changes the gain of the integrator and therefore the position of the poles and zeros in the noise transfer function.

Although the prototype chip did not achieve the expected performance, it demonstrates the possibility of designing a single-stage sigma-delta ADC with 8-bit inner quantization. The major contribution of this design, the introduction of a requantization algorithm to overcome the mismatch between the coarse and fine DAC is proved in this prototype with the measured noise floor in the signal bandwidth reduced by 20 dB. The benefits of this single-stage sigma-delta ADC with an 8-bit inner quantizer could be fully exploited if the system clock frequency can go ten times faster than that in the prototype.

7 Conclusions and Future Work

Sigma-delta modulation has emerged as an important technique for high resolution and high speed analog-to-digital conversion. This dissertation has explored the potential of applying a very large inner quantization to a single stage sigma-delta modulator to reduce the oversampling ratio (OSR). A new architecture of the ΣΔ modulator with two-step inner quantization and segmented DACs has been proposed to solve the problem of the exponential increase in the complexity of the flash ADCs and DACs associated with the large inner quantization. The consequence of the segmentation, mismatch between coarse and fine DACs is noise-shaped by using a digital requantization (REQ) algorithm. Additionally, an analytical study of the REQ algorithm was performed to get the upper limit of the DAC mismatch.

To verify the new architecture, an experimental prototype has been fabricated with TSMC 0.25um mixed-signal process. The effectiveness of the REQ algorithm was demonstrated by reducing the noise floor in the signal bandwidth by 20 dB. The measured system achieved a dynamic range of 70 dB with OSR of 16.

7.1 Contributions of the Dissertation

Key research contributions and results are summarized below:

1. Two-step inner quantization using traditional, power-efficient switched-capacitor circuits has been developed in a single-stage mulibit ΣΔ modulator by incorporating half-delay integrators, careful two-step ADC timing, and other architectural changes. The application of the two-step inner quantization solves one potential problem associated with the large number of quantization bits, unrealistic number of comparators in the common flash architecture. Both the MSB and LSB signals produced by the two-step quantization are fed back simultaneously to all integrator stages, making it suitable for low oversampling ratios. Two conference papers on this part of research have been published in [6,7].

2. A segmented architecture with coarse/fine DEM and DAC has been proposed to reduce the complexity of DEM and DAC due to the large number of bits used in the internal quantization. The consequence of the segmentation, mismatch between coarse and fine DACs, can be noise-shaped by using a digital requantization (REQ) algorithm. A theoretical analysis of the REQ algorithm has been conducted to obtain the upper limit of the gain mismatch between coarse and fine DACs. Both behavior simulation and the circuit implementation demonstrated the effectiveness of the REQ algorithm. A journal paper on this part of research has been accepted for publication [8].

3. A new architecture for the second-order ΣΔ modulator design has been developed. This architecture uses the 8-bit two-step ADC as the inner quantization, achieving high resolution with very low oversampling ratio. Two feed-forward branches are used to reduce the output swing of the integrators, therefore greatly relaxing the requirement on the DC gain of the opamp inside the integrators. A theoretical analysis of the feed-forward braches was performed to find the best gain of the branches.

4. An experimental prototype, including the proposed new architecture, has been fabricated with TSMC 0.25 μm mixed-signal process. The REQ algorithm has been implemented in the system to reduce the uncompensated coarse quantization noise caused by the gain mismatch of coarse and fine DAC. The measured results showed that the REQ algorithm can reduce the noise floor in the signal-band by 20 dB. The measured system achieved a dynamic range of 70 dB with an oversampling ratio of 16.

5. A static circuit with only switches and capacitors was developed to realize a non-delay adder before the inner quantization. By adding two extra capacitors to the front-end of the fully differential comparators, the non-delay adder becomes an integral part of the flash quantizer, which first adds two signals together and then quantizes their sum. The static circuit

adder has less power and chip area compared with that implemented with switched-capacitor circuit.

7.2 Future Work

Although this dissertation has proved the possibility of using the inner quantization with a large number of bits in a single-stage ΣΔ modulator, there are still several areas that warrant further study. They are summarized as follow:

1. Improve the bandwidth of the input signal. One of problems of the measured prototype chip is that the bandwidth of the input signal is much lower than expected even with a small oversampling ratio. The reason for the problem of low bandwidth is that the sampling frequency of the measured system can only achieve 4 MHz due to the distortion on the reference voltage and the coupling noise from the digital circuit. An improved design of the reference block and better isolation of the sensitive analog circuits during the layout design can help to increase the sampling rate of the system and therefore improve the bandwidth of the input signal.

2. Increase the noise shaping order of the single-stage ΣΔ modulator. Because each additional quantization bit improves overall SNR by 6 dB and also improves the linearity of the inner quantization, the single-stage ΣΔ modulator with the inner quantization of the large number of bits is more stable than the common multi-stage ΣΔ modulator, permitting more

aggressive noise shaping. To better take advantage of the improved stability brought by the large-number-bit inner quantization, a high-order single-stage ΣΔ modulator with more integrators and DACs can be built to increase the noise shaping order and achieve even higher resolution with a small oversampling ratio.

3. Improve the high-order REQ algorithm. Although the current first-order REQ algorithm is simple and suitable for the circuit implementation, the implementation complexity of the high-order REQ increases exponentially with each added order. An improved high-order REQ algorithm with reduced complexity may be very attractive for a high resolution ΣΔ modulator.

4. Optimize the power dissipation of the system. Because the integrators of the modulator only operate at one clock phase, staying idle at another clock phase, it is desirable to turn off the integrators when they are in the idle phase to save power dissipation. Additionally, the most powerful block, the clock generator can be optimized to reduce the power on the parasitic capacitors.

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