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A theoretical basis for practical amplifier design using cascaded operational amplifiers

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Abstract: A procedure is developed for the design of amplifiers to meet specified gain and bandwidth figures. The number of required operational amplifier stages is minimised. A figure of merit is introduced to determine if a particular operational amplifier can be used to satisfy a given set of specifications.

1 Introduction

Most electronics textbooks treat single stage operational amplifier designs [1, 2], but many practical amplifiers require multiple, cascaded operational amplifier stages to meet the given specifications. Two of the most significant specifications of amplifier performance are the overall voltage gain and the overall upper 3 dB frequency or bandwidth. In order that a finished design be considered acceptable, the actual overall gain and bandwidth must equal or exceed the specified values. An additional constraint imposed in practice is that of minimising the component cost of the finished product. Two dominant factors in determining overall component cost are the cost of the operational amplifier and the number of stages required.

A practical design procedure should allow the designer to [3]

(a) easily determine if a given operational amplifier can be used to satisfy overall gain and bandwidth specifications

(b) minimise the number of stages required for the design

(c) determine the individual stage gains and bandwidths required to meet the overall specifications.

(a) and (b) must be jointly considered to minimise component cost. A very expensive operational amplifier may lead to fewer stages required, yet total cost may be decreased by using more stages of a cheaper operational amplifier.

Although a good deal of amplifier theory has been developed in past years, it has been directed towards the goal of achieving a required overall gain along with maximum possible bandwidth [4-6]. When the resulting bandwidth exceeds the specified value, it is obvious that the number of stages could be reduced. In the past, the only method used to reduce stages was trial and error. This is by no means a trivial task. When the number of stages is reduced from the number used to maximise overall bandwidth, the individual stage gains must be adjusted; the individual stage bandwidths will consequently change, and the factor relating overall bandwidth to individual stage bandwidth also changes. Use of trial-and-error methods is highly inefficient. The theory and procedure developed in this paper allows the designer to meet specifications without resorting to a trial and error approach. Appropriate operational amplifiers can be selected and cost can be minimised with this procedure.

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2 The operational amplifier

The basic element in this procedure is the operational amplifier compensated for unity gain, shown in Fig. 1.

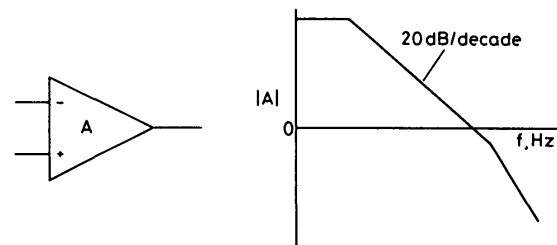


Fig. 1 The operational amplifier and frequency response

These devices exhibit a 20 dB/decade roll off in gain above the upper corner frequency and allow gain and bandwidth to be exchanged directly [7]. The gain-bandwidth product (GBW) is then constant with gain changes. The direct exchange of gain and bandwidth is possible for gains equal to or greater than unity.

For the noninverting stage of Fig. 2(a), the gain is given by

$$A_s = 1 + R_F/R_2$$

whereas the inverting stage of Fig. 2(b) has a gain of

$$A_s = -R_F/R_1$$

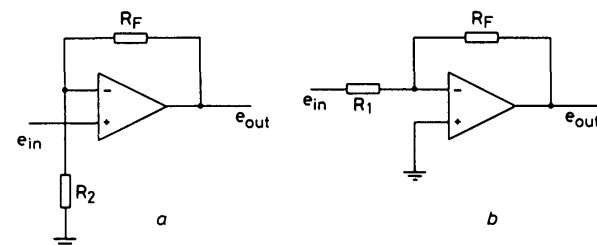


Fig. 2 Operational amplifier stages

a Noninverting
b Inverting

The bandwidth in either case can be found from

$$f_s = GBW/A_s$$

Not only do most commercial operational amplifiers have a constant GBW , the high input and low output impedances of these devices lead to negligible interaction of stages when cascaded. Thus, gain and bandwidth of an individual stage can be adjusted without affecting gain or bandwidth of adjacent stages.

3 Theoretical background

Most amplifier designs specify a value of required gain and required bandwidth that cannot be achieved by a single operational amplifier stage. When more than one stage is used, the overall gain and bandwidth values become rather complex functions of the individual stage values. If n identical or iterative stages are used, the overall gain A_0 is expressed as

$$A_0 = A_s^n \quad (1)$$

where A_s is the individual stage gain. The overall bandwidth f_0 is given in terms of the individual stage bandwidth f_s as

$$f_0 = f_s(2^{1/n} - 1)^{1/2} \quad (2)$$

Eqn. 2 is referred to as the bandwidth shrinkage equation [5]. For $n > 2$, eqn. 2 can be approximated quite accurately [5] by

$$f_0 = f_s/1.2n^{1/2} \quad (3)$$

If constant GBW stages are used, the overall bandwidth can be maximised with respect to individual stage gain. This is accomplished by expressing f_0 in terms of A_s to give

$$f_0 = GBW(\ln A_s)^{1/2}/1.2A_s(\ln A_0)^{1/2} \quad (4)$$

Eqn. 4 is then differentiated with respect to A_s and this derivative is equated to zero. The result of this maximisation process is well-known [4, 5] and states that the individual stage gain must equal 1.65 to yield the maximum overall bandwidth with the given GBW .

This theory can be used to calculate the minimum required GBW of an operational amplifier for use in an amplifier. If A_{or} and f_{or} , the required overall gain and bandwidth, respectively, are specified, the gain can be taken to be 1.65. The actual overall bandwidth from eqn. 4 must exceed the required bandwidth or

$$GBW(\ln A_s)^{1/2}/1.2A_s(\ln A_{or})^{1/2} \geq f_{or}$$

assuming the overall gain is caused to equal A_{or} . Substituting 1.65 for A_s and solving for GBW gives

$$GBW \geq 2.8f_{or}(\ln A_{or})^{1/2} \quad (5)$$

If the operational amplifier GBW does not equal or exceed the value given in eqn. 5, the amplifier specifications cannot be met regardless of the number of such stages used. If the operational amplifier GBW happens to equal the minimum value, the amplifier can be realised only if the individual stage gain is set to 1.65. The number of stages required in this instance is

$$n = \ln A_{or}/\ln 1.65 \approx 2 \ln A_{or} \quad (6)$$

From a practical standpoint the most interesting case occurs when the operational amplifier GBW exceeds the minimum value. The amplifier could now be constructed to equal or exceed both the overall gain and bandwidth requirements. Rather than allow excess gain or bandwidth, however, it is economically advantageous to reduce the number of stages to the minimum required to achieve the overall specifications. In many cases, this results in a significant reduction in the number of stages and component cost of the amplifier.

Before proceeding to the calculation of the minimum number of stages required, another result must be established. This result applies to noniterative stages as well as iterative. Given any number of stages and a required overall bandwidth, it has been shown that gain is maximised by setting individual stage bandwidths equal [8].

Using this result allows the bandwidth shrinkage formula to apply to noniterative amplifiers in which gain is being maximised.

4 Minimising the number of stages

To calculate the minimum number of operational amplifier stages needed to satisfy a given design, it is first assumed that n stages with an individual stage gain of 1.65 are used. Assuming an excess overall bandwidth results from this situation, stages can be removed if the proper adjustment is made in individual stage gain and bandwidth. If m is the minimum number of stages, the adjusted single stage gain must be

$$A_s = (1.65)^{n/m} = (A_{or})^{1/m} \quad (7)$$

The adjusted single stage bandwidth can be found from eqn. 3 to be

$$f_s = 1.2m^{1/2}f_{or}$$

To solve for the three unknowns A_s , f_s and m , a third equation is required. The simple relationship between gain and bandwidth yields this third equation, that is,

$$GBW = A_s f_s$$

Solving for m from the two preceding equations results in

$$m = GBW^2/1.44f_{or}^2 A_s^2$$

Taking the natural logarithm of both sides of eqn. 7 gives

$$\ln A_s = (\ln A_{or})/m$$

Eliminating m from the last two equations leads to the requirement on A_s that

$$\ln A_s = Z A_s^2 \quad (8)$$

where

$$Z = 1.44f_{or}^2(\ln A_{or})/GBW^2 \quad (9)$$

For a given value of Z , eqn. 8 can be solved graphically or with the aid of a hand calculator. Table 1 tabulates values of A_s for various practical values of Z . The range of individual stage gain from 1.65 to 10 is sufficient for most practical amplifier stages. Larger values of gain limit the individual stage bandwidth to impractical values.

Once the proper value of A_s is determined, the minimum number of stages can be calculated from eqn. 7 and is

$$m = \ln A_{or}/\ln A_s \quad (10)$$

Table 1: Individual stage gain as a function of Z

Z	A_s	Z	A_s
0.184	1.65	0.090	3.88
0.180	1.85	0.080	4.25
0.170	2.06	0.070	4.70
0.160	2.26	0.060	5.26
0.150	2.44	0.050	5.98
0.140	2.62	0.040	6.98
0.130	2.82	0.035	7.62
0.120	3.05	0.030	8.42
0.110	3.29	0.026	9.24
0.100	3.56	0.023	10.0

5 Relating theory to design

The constant Z is a useful figure to describe the effectiveness of a specific operational amplifier in meeting the specifications of a given design problem. It can be noted from eqn. 9 that Z depends not only on the operational

amplifier GBW , but also on the required overall gain and bandwidth of the amplifier to be designed. Eqn. 8 can be used to obtain the graph of Fig. 3 showing Z as a function

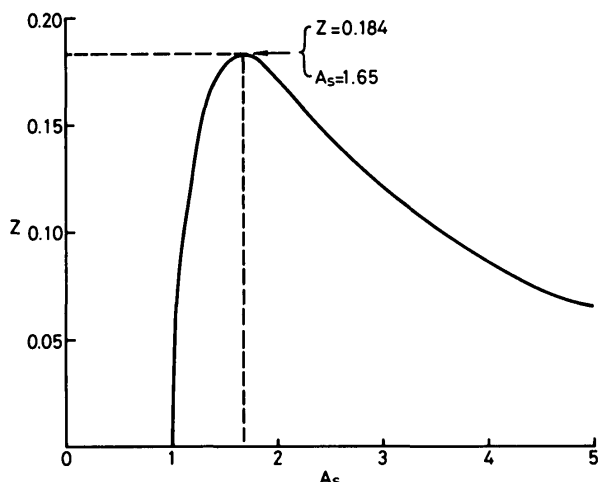


Fig. 3 Required value of Z as a function of single stage gain

of A_s . The maximum value of Z occurs when $A_s = 1.65$. This value is 0.184. For any value of gain, Z must be less than or equal to the value 0.184. If an operational amplifier is selected that leads to a value of Z from eqn. 9 that exceeds 0.184, it is immediately known that the operational amplifier cannot satisfy the overall amplifier specifications. If Z equals 0.184, then the interstage gain must equal 1.65 to achieve the desired overall gain and bandwidth. If Z is less than 0.184, the number of stages can be minimised as outlined in the previous section. The designer can immediately evaluate the suitability of a particular operational amplifier for the specified amplifier simply by calculating Z . The operational amplifier leading to the lowest value of Z will result in the least number of stages required, assuming Z is less than 0.184. Although Z can be considered to be a figure of merit, it is to be emphasised that lower values of Z are most desirable.

As the cost of an operational amplifier is determined by production volume and performance of the operational amplifier in addition to other factors, there is no analytic method of minimising the overall amplifier cost. The minimum number of stages calculated for one operational amplifier will often be different from that calculated for a second operational amplifier with a different GBW . For example, operational amplifier A may require six stages, whereas operational amplifier B which is 20% more expensive than operational amplifier A, may require only four stages to satisfy the amplifier specifications. Thus, component cost minimisation will generally require trial-and-error methods.

The design procedure consists of the following steps:

- (a) calculate the figure of merit Z for the operational amplifier
- (b) find the values of single stage gain A_s from Table 1 or by solving eqn. 8
- (c) calculate m , the minimum number of stages required, from eqn. 10
- (d) repeat for all other operational amplifiers under consideration
- (e) compare component cost for each case.

6 A design example

An amplifier is to be designed with an overall gain of 800 and an overall bandwidth of 100 kHz. The maximum

output signal will be small enough to neglect slew rate limiting. Three types of operational amplifier are available, as shown in Table 2.

Table 2: Available types of operational amplifier

Operational amplifier	GBW	cost
A	2×10^5	x
B	1×10^6	$1.23x$
C	1.5×10^6	$1.95x$

The first step in the procedure calls for Z to be calculated. For operational amplifier A, the figure of merit is found to be $Z = 2.4$ which exceeds the maximum allowable value of 0.184; hence, this operational amplifier cannot be used. For operational amplifier B, $Z = 0.096$. The value of A_s corresponding to this value of Z is found by interpolation from Table 1 to be $A_s = 3.68$. Applying eqn. 10 results in a minimum number of stages of 5.13. For a practical amplifier, an integer number of stages is required. Six stages would be used in this case. Repeating the calculations for operational amplifier C yields values of $Z = 0.043$, $A_s = 6.68$, and $m = 3.52$. Four stages would be required if operational amplifier C is used for the amplifier. Before choosing the operational amplifier, the overall device cost is compared. For operational amplifier B, the device cost is $6(1.23x) = 7.38x$ and the device cost for operational amplifier C is $4(1.95x) = 7.80x$. Although the amplifier requires fewer stages when using operational amplifier C, the device cost for the overall amplifier is less when realised with operational amplifier B.

The result obtained in this example should be compared to the number of stages required to optimise the overall bandwidth. In this case $A_s = 1.65$ and $n = 14$ stages. If classical theory is applied, 14 stages would be used rather than 4 operational amplifier C or 6 operational amplifier B stages.

In practice, a given operational amplifier type will exhibit broad variations of GBW from one device to the next. The procedure outlined assumes equal values of GBW for all devices. For practical amplifiers, the designer is generally interested in worst-case design. If several amplifiers are to be manufactured, each must meet minimum specifications even for that possible combination of stages that minimise performance. With the proposed method, minimum performance occurs when individual stage values of GBW are lowest. Thus, if the value used to calculate Z in eqn. 9 is GBW_{min} for the operational amplifier used, the resulting amplifier is the worst-case design.

7 Conclusions

The procedure discussed in the paper allows a designer to realise a specified overall gain and bandwidth of an amplifier while minimising the number of required stages. The figure of merit Z is a useful parameter in determining whether or not a particular operational amplifier can be used in the specified amplifier design. This parameter also aids the designer in calculating the required gain per stage and the minimum number of required stages. Worst-case design can be carried out with this procedure and overall component cost can be minimised.

8 References

- 1 WATSON, J.: 'Analogue and switching circuit design' (Adam Hilger, Bristol, 1984), Chap. 7

- 2 WAIT, J.V., HUELSMAN, L.P., and KORN, G.A.: 'Introduction to operational amplifier theory and applications' (McGraw-Hill, New York, 1975), Chap. 1
- 3 COMER, D.J.: 'Video amplifier design based on operational amplifiers', *IEEE Trans.*, 1976, **CAS-23**, pp. 169-171
- 4 VALLEY, G.E., and WALLMAN, H.: 'Vacuum tube amplifiers' (McGraw-Hill MIT Radiation Lab Series, New York, 1948, Vol. 18), Chap. 4
- 5 GHANSI, M.S. 'Electronic devices and circuits: discrete and integrated' (Holt, Rinehart and Winston, New York, 1985), Chap. 8
- 6 SEDRA, A.S., and SMITH, K.C.: 'Microelectronic circuits' (Holt, Rinehart and Winston, New York, 1982), Chap. 11
- 7 COMER, D.J.: 'Electronic design with integrated circuits' (Addison-Wesley, Reading, 1981), Chap. 1
- 8 COMER, D.J., and GRIFFITH, J.M.: 'Optimisation of bandwidth in noniterative amplifiers', *Proc. IEE*, 1969, **116**, (3), p. 384



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