

Brigham Young University BYU ScholarsArchive

**Faculty Publications** 

2007-01-26

# Frequency response of solid-state impact ionization multipliers

Joshua Beutler jlbeutler@byu.edu

Carlton S. Clauss

Michael S. Johnson

Aaron R. Hawkins hawkins@ee.byu.edu

Mike D. Jack

See next page for additional authors

Follow this and additional works at: https://scholarsarchive.byu.edu/facpub

Part of the Electrical and Computer Engineering Commons

# **Original Publication Citation**

Beutler, Joshua L., Carleton S. Clauss, Michael S. Johnson, Aaron R. Hawkins, Mike D. Jack, George R. Chapman, and Ken Kosai. "Frequency response of solid-state impact ionization multipliers." Journal of Applied Physics 11 (27)

# **BYU ScholarsArchive Citation**

Beutler, Joshua; Clauss, Carlton S.; Johnson, Michael S.; Hawkins, Aaron R.; Jack, Mike D.; Chapman, George R.; and Kosai, Ken, "Frequency response of solid-state impact ionization multipliers" (2007). *Faculty Publications*. 275.

https://scholarsarchive.byu.edu/facpub/275

This Peer-Reviewed Article is brought to you for free and open access by BYU ScholarsArchive. It has been accepted for inclusion in Faculty Publications by an authorized administrator of BYU ScholarsArchive. For more information, please contact ellen\_amatangelo@byu.edu.

# Authors

Joshua Beutler, Carlton S. Clauss, Michael S. Johnson, Aaron R. Hawkins, Mike D. Jack, George R. Chapman, and Ken Kosai

# Frequency response of solid-state impact ionization multipliers

Joshua L. Beutler,<sup>a)</sup> Carleton S. Clauss, Michael S. Johnson, and Aaron R. Hawkins *Electrical and Computer Engineering Department, Brigham Young University, 459 Clyde Building, Provo, Utah 84602* 

Mike D. Jack, George R. Chapman, and Ken Kosai Raytheon Vision Systems, 75 Coromar Drive, Goleta, California 93117

(Received 13 July 2006; accepted 6 November 2006; published online 26 January 2007)

A study of the frequency response of solid-state impact ionization multipliers (SIMs) is presented that emphasizes the role of resistive and capacitive elements of the device to establish response limitations. SIMs are designed to amplify input currents from an external source through the impact ionization mechanism. An equivalent circuit model for the SIM is developed based on its current versus voltage characteristics, which is used to derive a frequency response model. Theoretical frequency response matches very closely to measured responses for first generation SIM devices constructed on *p*-type silicon epitaxial layers with nickel silicide Schottky contact injection points. Devices were measured using a photodiode as a current source under light intensities between 74 nA and 7.4  $\mu$ A. These SIMs were shown to have a low frequency response that follows a *KT/I* relationship. Using an external photodiode with an effective capacitance of 6.8 pF, frequency response for a 1.8  $\mu$ A input current was limited to 100 kHz. A large effective barrier resistance due to the Schottky contact and 12 k\Omega space charge resistance dependent on device geometry dominate the response. Future SIM designs with higher frequency response will have to significantly lower both the input barrier resistance and space charge resistance. © 2007 American Institute of Physics. [DOI: 10.1063/1.2426376]

### I. INTRODUCTION

The solid-state impact ionization multiplier (SIM) was introduced in an effort to create an electronic device capable of producing impact ionization based current gain for a signal from an arbitrary current source. Other devices such as avalanche photodiodes<sup>1</sup> (APDs) and impact ionization avalanche transit-time (IMPATT) diodes<sup>2</sup> utilize impact ionization gain. Current sources for APDs reside within the depletion region of the device itself. IMPATT diodes rely on an external voltage source to induce avalanche gain in the depletion region of the device. Consequently, a current source cannot be "wired up" to these devices and exhibit a steady-state current gain over unity. However, this is the intended purpose of the SIM. Impact ionization based gain is attractive because it can provide very low noise amplification for small current signals. This is most easily illustrated by the continued use and development of APDs for the detection of low light signals. APDs provide additional gain to a photocurrent generated within their depletion regions while operating below the noise floor of subsequent transistor based amplifiers (transimpedance amplifiers) used to convert current into readable voltage levels. Levels of light can thus be detected that would be indistinguishable without the additional gain provided by the APD. SIMs are intended to operate in much the same way. A current source feeds signal into the SIM where it is amplified and then fed into a transimpedance amplifier for voltage readout. Potential current sources compatible with the SIM include photodiodes made

from any semiconductor (and thus sensitive to a large selection of light wavelengths) and charge collectors.<sup>3</sup>

Initial SIM designs have been fabricated on silicon substrates and measured 4-6 to confirm that impact ionization based gain is present in these devices. Photodiodes constructed from silicon and indium-gallium-arsenide were connected to devices under test, and current gain was measured when photocurrent was generated by visible and near infrared ( $\lambda$ =1300 nm) light sources. To this point, SIM operation has been reported for only dc injection. Since most applications utilizing SIMs would involve the measurement of current pulses, it is important to understand their frequency response. This paper provides an investigation of the parameters contributing to SIM frequency response emphasizing the resistive and capacitive elements that will establish the fundamental speed limitations for the device. A theoretical groundwork is laid out to model frequency response and this is compared to measured values on real SIM devices based on first generation SIM designs. The paper is organized as follows. Section II provides a thorough discussion of electron and hole actions that lead to the current versus voltage characteristics of the SIM. From these characteristics, Sec. III develops a circuit model for a general SIM design from which a frequency response can be derived. Section IV investigates the key parameter for the frequency response of first generation SIMs-the resistance due to the Schottky metal contact used for current injection. Section V compares the predicted frequency response based on the circuit model and barrier resistance to measurements on first generation SIM devices. Section VI then examines the de-

0021-8979/2007/101(2)/023117/9/\$23.00

101, 023117-1

<sup>&</sup>lt;sup>a)</sup>Electronic mail: jlbeutler@byu.edu



FIG. 1. Example of SIM structure. This is a cross sectional view of a device made using a p-type epitaxial layer on a p+ substrate. The electron collector is the n+ doped region and the hole sink is the p+ doped substrate. This represents what is called a vertical device as excess holes are drawn vertically to the hole sink.

sign changes the current generation of SIM devices would need to significantly increase their frequency response.

# II. CURRENT AND VOLTAGE CHARACTERISTICS OF SIMS

An accurate explanation of the frequency response of the SIM must begin with a precise description of its current versus voltage characteristics, from which a circuit model can be developed. Current versus voltage plots have been presented before,<sup>4–6</sup> but here we present a thorough description of carrier movement, carrier injection mechanisms at the device's metal-semiconductor barrier, and biases at critical nodes of the device. A diagram illustrating the structure of SIMs made up to this point is shown in Fig. 1. This represents what is referred to as a "vertical SIM" in which the p+ doped substrate is grounded. The fundamental idea behind the SIM's operation is that electrons can be injected at the metal-semiconductor contact and drawn toward the positively biased voltage  $(V_{SIM})$  node connected to an n+ doped region. This n+ doped region will be referred to as the electron collector. The injected electrons move through a high field region established between both the n+ doped region and the metal-semiconductor contact (in Fig. 1 this could be described as a horizontal field) and the n+ doped region and the p+ doped substrate (in Fig. 1 this could be described as a vertical field). As electrons drift in this field, they experience impact ionization events leading to the creation of electronhole pairs. Newly created electrons are drawn toward the  $V_{\rm SIM}$  voltage node while newly created holes are drawn toward ground. Drawing holes toward a "hole sink" instead of back toward the metal-semiconductor interface is critical to achieving current gain in the SIM. Without this action, newly created holes would recombine with incoming electrons at the metal-semiconductor interface, eliminating any net gain produced by the device. For operation with gain, the voltage at the metal-semiconductor contact must be positive in relation to ground to induce holes towards the hole sink.

The semiconductor doping and structure illustrated in Fig. 1 represent the SIM introduced,<sup>4</sup> but many variations can be made to the device while maintaining the same operation principle. For example, hole sinks could be made on the surface of a semiconductor substrate through *p*-type doping, creating regions offset to either side of the n+ doped



FIG. 2. Graph showing  $I_{\text{SIM}}$  vs  $V_{\text{SIM}}$  for a vertical device built using a *p*-type epitaxial layer on a *p*+ substrate. Current injection was done by illuminating a silicon photodiode connected to the SIM.

region (electron collector). "Surface SIMs" made in this way have already been demonstrated.<sup>5</sup> Another variation to the SIM could be made to the metal-semiconductor interface that serves as the current injection point. In devices made thus far, this interface is best described as a Schottky contact with a large energy barrier for incoming carriers, but more Ohmic contacts would be a possibility. Previously made devices were also made using epitaxial silicon wafers with a lowdoped p layer on top of a p+ substrate. Variations could include a n- doped epitaxial layer, alternate semiconductors, and a device optimized for the injection of holes instead of electrons. For any of these variations, contact spacings and operation voltages would have to be adjusted to account for changes in doping depletions and electric fields. For coherence, the descriptions and measurements in this paper will be based around the vertical SIM design in silicon with a *p*-type epitaxial layer (the surface SIM on a p-type epitaxial layer will be similar). Developing accurate models for variations to this design should be straightforward following the same framework established here.

A typical current versus voltage curve for a vertical silicon SIM is shown in Fig. 2. Current was injected into the device using a reversed biased photodiode illuminated with a light source. This particular SIM had a spacing (*d*) between the metal-semiconductor interface and *n*+ doping region of around 5  $\mu$ m and was built on a *p*-epitaxial layer of approximately 3  $\Omega$  cm resistivity. The curve in Fig. 2 shows the current out of the electron collector ( $I_{\text{SIM}}$ ) versus the voltage applied to this node ( $V_{\text{SIM}}$ ). The measurement was done using an HP/Agilent 4156 source-measure unit, which can bias and measure several voltage nodes simultaneously allowing the measurement of current flow through the photodiode, the hole sink, and the electron collector.

The shape of the  $I_{\text{SIM}}$  vs  $V_{\text{SIM}}$  curve is of particular interest in understanding the action of carriers within the SIM. Figure 2 shows three distinct operation regions for the device—first a region where there is very little current flowing through the electron collector, then a region in which the current increases very rapidly, followed by a region in which the current increases further but at a more gradual rate. These three distinct regions have been illustrated in Fig. 3. The



FIG. 3. Representation of a model SIM current vs voltage curve with the three important operating regions labeled.

action of electrons and holes within the SIM will now be closely examined for each of these regions as well as what is happening at the metal-semiconductor interface, it being a key element to quantifying the SIM's operation.

#### A. Region A

The operation of the SIM in region A is illustrated in Fig. 4. A constant negative voltage  $V_{pd}$  is applied to a photodiode so that it is reverse biased. The hole sink of the SIM is grounded and  $V_{SIM}$  is reverse biased above ground. Monitoring the currents flowing in or out of these voltage nodes indicates that current flows into the  $V_{pd}$  voltage node (equal to the photocurrent being generated in the photodiode), current flows out of the grounded hole sink, and virtually no



FIG. 4. Representation of carrier action in the SIM when operating in region A. (a) Carrier action and semiconductor depletion in a cross section of a vertical SIM. (b) Band diagram representation of the metal-semiconductor interface and carrier action.



FIG. 5. Representation of carrier action in the SIM when operating in region B. (a) Carrier action and semiconductor depletion in a cross section of a vertical SIM. (b) Band diagram representation of the metal-semiconductor interface and carrier action.

current flows in or out of the electron collector. These monitored currents are the manifestation of the following carrier action: Holes generated in the photodiode move toward the negative V<sub>pd</sub> node while electrons move toward the metalsemiconductor interface and the floating voltage node  $V_{\rm ms}$ . Holes are drawn from the p+ doped hole sink toward the metal-semiconductor interface. At the interface, holes are thermionically ejected over the metal-semiconductor barrier where they combine with electrons in the metal as illustrated in Fig. 4(b). The floating voltage  $V_{\rm ms}$  at the metalsemiconductor interface adjusts to allow for enough hole current flow over the barrier (by lowering  $\Theta$ ) to equal the incoming electron current flow from the photodiode. This means that  $V_{\rm ms}$  must be negative in relation to ground and the Schottky contact at the metal-semiconductor interface forward biased.

While there is no appreciable current flow into or out of the electron collector when the SIM is operating in region A, applying positive voltage  $V_{\text{SIM}}$  depletes the p- doped semiconductor surrounding the N+ region and raises the electric field in these regions. Current injected at the metalsemiconductor contact does not affect the current through the electron collector because the extent of the depletion region is less than the spacing (*d*) between the electron collector and metal-semiconductor contact.

## **B. Region B**

The operation of the SIM in region B is illustrated in Fig. 5.  $V_{\text{SIM}}$  is reverse biased above ground to around a specific voltage  $V_{\text{dep}}$ . Monitoring the currents flowing in or out of these voltage nodes indicates that current flows into the

Downloaded 13 Feb 2009 to 128.187.0.164. Redistribution subject to AIP license or copyright; see http://jap.aip.org/jap/copyright.jsp

 $V_{\rm pd}$  voltage node (equal to the photocurrent being generated in the photodiode), current flows out of the electron collector, and current now flows into the hole sink. The currents through the nodes maintain the following relationship:  $I_{\rm SIM}$ =current through the photodiode + current into the hole sink. These monitored currents are the manifestation of the following carrier action: Holes generated in the photodiode move toward the negative  $V_{\rm nd}$  node while electrons move toward the metal-semiconductor interface and the floating voltage node  $V_{\rm ms}$ .  $V_{\rm SIM}$  has now reached the point where the depletion region surrounding the electron collector has reached the metal-semiconductor interface. When this happens, holes are no longer drawn up from the hole sink and ejected over the metal-semiconductor barrier. Instead, electrons are thermionically ejected over the barrier and into the depletion region as illustrated in Fig. 5(b). The floating voltage  $V_{\rm ms}$  at the metal-semiconductor interface adjusts to allow for electron current flow over the barrier (by lowering  $\Theta$ ) to equal the incoming electron current flow from the photodiode. This means that  $V_{\rm ms}$  is now positive in relation to ground. The injection of current from the photodiode into the depletion region is manifested in Fig. 3 by an abrupt increase in current. While this clearly indicates that a substantial amount of photocurrent is injected into the depletion region, electron-hole recombination may still take place at the metalsemiconductor junction until the depletion region moves across a substantial part of the metal-semiconductor contact.

Electrons ejected over the metal-semiconductor barrier will drift in the depletion region toward the electron collector and appreciable current will finally flow toward this node. If the electric field is high in the depleted semiconductor surrounding the electron collector, impact ionization can occur leading to the creation of electron-hole pairs. Additional electrons also drift toward the electron-hole collector, but created holes now drift toward the hole sink accounting for any current flowing into the hole sink. The magnitude of  $I_{\text{SIM}}$ is then equal to  $I_{\text{pd}}G$ , where G is the current gain resulting from impact ionization. The magnitude of the current flowing into the hole sink is equal to  $I_{\text{pd}}(G-1)$ .

### C. Region C

The operation of the SIM in region C is illustrated in Fig. 6.  $V_{\text{SIM}}$  is reverse biased above  $V_{\text{dep}}$ , the voltage characteristic of region B. Again the current flowing into the  $V_{\text{pd}}$  voltage node remains constant and equal to the photocurrent being generated in the photodiode, current flows out of the electron collector, and current flows into the hole sink. The currents through the nodes maintain the same relationship that was true in region B:  $I_{\text{SIM}}$ =current through the photodiode+current into the hole sink. Carrier action in region C is similar to what happens in region B. The same current is injected from the photodiode at the metal-semiconductor interface.  $V_{\text{SIM}}$  has now increased, however, increasing the strength of the electric field around the electron depletion region. Electrons injected into this region can experience more impact ionization events and the current



FIG. 6. Representation of carrier action and semiconductor depletion in a cross section of a vertical SIM when operated in region C.

 $I_{\text{SIM}}$  increases according to  $I_{\text{SIM}} = I_{\text{pd}}G$ . Holes created through impact ionization continue to be drawn to the grounded hole sink.

The effect of increasing  $V_{\rm SIM}$  on the floating voltage  $V_{\rm ms}$ should be noted. Because  $V_{\rm ms}$  is determined by the amount of current injected by the current source attached to the SIM (the metal-semiconductor barrier adjusts to allow the current over the barrier to equal the current injected), the voltage between  $V_{\rm ms}$  and  $V_{\rm SIM}$  for a given input current will remain a constant given by  $V_{dep}$ . Therefore as  $V_{SIM}$  is raised above  $V_{\text{dep}}$ ,  $V_{\text{ms}}$  rises according to  $V_{\text{ms}} = V_{\text{SIM}} - V_{\text{dep}}$ .  $V_{\text{ms}}$  will vary with input currents, but this variation will be relatively small compared to  $V_{\text{SIM}} - V_{\text{dep}}$  for most conceivable applications. The effect of "locking down" the voltage difference between  $V_{\rm SIM}$  and  $V_{\rm ms}$  will have several important implications for the SIM. First, the lateral extent of the depletion region in the direction of the metal-semiconductor contact will be constant (d) even as  $V_{\text{SIM}}$  increases. Second, because the depletion region remains unchanged, the electric field profile must remain the same. Any additional impact ionization must then be due to the increased electric field between the electron collector and the hole sink (vertical field). A third effect of this "voltage locking" is that increasing  $V_{\text{SIM}}$  beyond  $V_{\text{dep}}$  has no effect on the injection mechanism at the metalsemiconductor and cannot raise or lower the barrier seen by carriers as they enter the SIM.

### III. SIM CIRCUIT MODEL AND RC FREQUENCY RESPONSE LIMITS

Given the current versus voltage characteristics described in the previous section, there are several important elements to the SIM that should be included in a circuit model for the device. These elements include (1) the Schottky diode between the metal-semiconductor contact and the p+ doped hole sink, (2) a representation of the metalsemiconductor barrier that is dependent on the input current and whether  $V_{\text{SIM}}$  is greater than  $V_{\text{dep}}$ , and (3) a current gain element between the hole sink and electron collector that can account for net impact ionization gain. In addition to these elements, the circuit model should include capacitive and resistive terms present with p-n junctions and metal to semiconductor contacts. Since SIMs have many characteristics in



FIG. 7. Circuit model for a SIM connected to a photodiode current source when  $V_{\text{SIM}}$  is greater than the depletion voltage. Note that  $I_3$  is a dependent current source representing the impact ionization gain mechanism.

common with avalanche photodiodes, a common model for these devices<sup>7</sup> has been adapted, neglecting for now any temperature dependence for the device.

Figure 7 represents the circuit elements used to model the SIM. Included in this circuit is a model for a photodiode being used as a current source connected to the SIM. The model takes into account the connections between the three voltage nodes for the device. Between  $V_{\rm ms}$  and the grounded hole sink, a diode is used to allow for current flow when  $V_{\rm ms}$ is negatively biased compared to ground. In addition, a capacitor is added to represent the capacitance between the metal-semiconductor interface and ground (including the contact pad necessary in real devices). The series resistance and space charge terms are also included. Between metalsemiconductor contact and electron collector ( $V_{\rm ms}$  and  $V_{\rm SIM}$ ), the resistor  $R_{\text{barrier}}$  is used to represent the metalsemiconductor barrier that is current dependent and infinitely large when  $V_{\rm SIM} < V_{\rm dep}$ . This is the barrier electrons see when injected into a depleted region between these nodes. The resistance values for this barrier will be developed in the following section. A capacitor is also included between the two nodes representing the capacitance between the metalsemiconductor contact and electron collector. The series and space charge resistance terms are also included. Between the electron collector and hole sink ( $V_{\text{SIM}}$  and ground) a dependent current source is used to represent the net impact ionization gain produced by the device. Parallel to this current source is a diode representing the reversed biased p-n junction between the electron collector and hole sink. Also parallel to the current source is a capacitor representing the capacitance between electron collector and ground (including contact pads). Finally the series and space charge resistance terms are added between these two nodes. While this model does not take into account effects such as carrier transit time and impaction ionization multiplication delay times, it can provide a frequency response limit based on resistive and capacitive elements for the device. As will be shown in later sections, these elements dominate the frequency response of current SIM designs.

Utilizing the circuit model in Fig. 7 to solve for the relationship between  $I_{\text{SIM}}$  and  $I_{\text{pd}}$  at different operating frequencies  $\omega$  is a straightforward exercise but the expressions for  $I_{\text{SIM}}$  become quite complicated when including all of the elements found in the circuit model. By making several approximations, however, a solution can be derived that is physically insightful and accurate in most cases. The first approximations to be made are that the series resistances and space charge resistances can be neglected in the case of  $R_{\rm pd}$ ,  $R1_{s.sc}$ , and  $R3_{s.sc}$ . In each of these cases, the series resistance is due to an Ohmic metal-semiconductor contact and so should be quite low. The space charge resistance comes from a relatively large area contact over a thin depletion region and, so too, should be low. Typically series and space charge resistances of this type are less than 50  $\Omega$ . Compared to other elements in the SIM, these should have a very small effect on the overall response. Not to be neglected, however, is the space charge term contained in the resistance  $R2_{s,sc}$ which we have shown<sup>6</sup> to be quite significant (~10000  $\Omega$ ) due to the large channel lengths between the metalsemiconductor contact and electron collector and relatively short channel depths. The second approximation to be made is that the capacitive term  $C_2$  can be neglected compared to other capacitive terms and  $R_{\text{barrier}}$ . Given that this represents the capacitance between two nodes in a lateral direction on the surface of a wafer, this assumption should be valid. Given these approximations, relationships for  $I_{\text{SIM}}$  and  $I_{\text{pd}}$  at given frequencies  $\omega$  can be written in terms of the floating voltage  $V_{\rm ms}$ ,

$$I_{\text{SIM}} \approx \frac{V_{\text{ms}}}{R_{\text{barrier}} + R2_{\text{s,sc}}} G,$$

$$I_{\text{pd}} \approx \frac{V_{\text{ms}}}{R_{\text{barrier}} + R2_{\text{s,sc}}} [1 + j\omega(R_{\text{barrier}} + R2_{\text{s,sc}})](C_1 + C_{\text{pd}}).$$
(2)

Dividing (1) by (2) a relationship for  $I_{\text{SIM}}/I_{\text{pd}}$  can be obtained.

$$\frac{I_{\text{SIM}}}{I_{\text{pd}}} \approx \left[\frac{G}{1 + j\omega(R_{\text{barrier}} + R2_{\text{s,sc}})(C_1 + C_{\text{pd}})}\right].$$
 (3)

The 3 dB down frequency in which  $\sqrt{(I_{\text{SIM}}/I_{\text{pd}})(I_{\text{SIM}}/I_{\text{pd}})^*} = \sqrt{1/2}$  will be given by

$$f_{3 \text{ dB}} = \frac{\omega_{3 \text{ dB}}}{2\pi} \approx \frac{1}{2\pi (R_{\text{barrier}} + R2_{\text{s,sc}})(C_1 + C_{\text{pd}})}.$$
 (4)

The simple relationship derived in (4) gives us tremendous insight into the frequency response limits for the SIM. In essence, the dominant terms will be the barrier resistance at the metal-semiconductor interface and any space charge resistance terms between this interface and the electron collector. Because the barrier height is input current dependent for the vertical SIM with a Schottky metal-semiconductor contact, the barrier resistance and thus the frequency response should also be current dependent. A derivation of the barrier resistance for this type of interface is given in the next section.

To confirm the accuracy of our assumptions in deriving (4), the circuit in Fig. 7 was modeled using SPICE (Ref. 8) and the 3 dB frequency responses shown to match with less than 1% discrepancy for a large range of component values. Because component values such as  $R_1$  and  $R_3$  were neglected or assumed to be small (50  $\Omega$ ) in the frequency response derivation, further simulations were needed to determine the extent to which these values could be realistically ignored before noting a substantial deviation from the calculated 3 dB frequency response.  $R_1$  and  $R_3$  typically represent contact resistances and space charge resistance seen by carriers. Consequently, initial values for  $R_1$  and  $R_3$  used in these simulations were small. However, because of possible space charge effects that occur at high gains, resistance values ranged as high as 10 k $\Omega$  in the simulation. Assuming realistic values for  $C_1$  and  $C_{pd}$  of 2 and 2 pf, respectively, variations of  $R_1$  and  $R_3$  revealed a weighted two pole effect on frequency response. These poles are not evident in (4) due to simplification intent on only revealing the most dominant pole, however, SPICE models reveal their existence.  $R_3$ proved to be the dominant pole. Increases to  $R_3$  similar to those mentioned in  $R_1$  caused simulations to deviate substantially from the derived frequency response calculation. Increasing  $R_3$  to 1  $\Omega$  caused 2% deviation and 55% at 5 k $\Omega$ .  $R_1$  proved the second largest pole showing a 1% deviation on derived frequency response for 1 k $\Omega$  and a 10% deviation at 10 k $\Omega$ . Changing the values of  $C_1$  and  $C_{\rm pd}$  can change the pole order dominance; however, the capacitive values were specifically chosen to reflect a realistic scenario. The main exception would be specifying the value of  $C_{pd}$ , which may exhibit substantial variation depending on the type and speed of photodiode being used. Use of a large capacitance photodiode will reduce overall bandwidth by causing the photodiode, not the SIM, to become the dominant pole.

#### IV. METAL-SEMICONDUCTOR BARRIER RESISTANCE AND SPACE CHARGE RESISTANCE

Due to the important role the resistance of the metalsemiconductor interface plays in determining the frequency response of the SIM, a derivation of the resistance will be made for the vertical SIM with a Schottky contact on a p-type semiconductor. R<sub>barrier</sub> is based on the thermionic ejection of electrons over the barrier and can be found by considering the current versus voltage relationship that is barrier height dependent. The energy barrier for electrons between the metal-semiconductor contact and electron collector is illustrated in Fig. 8 assuming that the semiconductor layer between the two nodes has been completely depleted and there is a constant doping between the nodes. As  $V_{\rm SIM}$ continues to increase, the electron barrier height drops by an amount  $\Delta \Theta$  allowing more electrons over the barrier. The value for  $R_{\text{barrier}}$  can be found by determining the relationship between ejected current and  $V_{\text{SIM}}$ .



FIG. 8. Energy band diagram showing the barrier for electrons injected from a metal contact into a SIM built on a *p*-type epitaxial layer. After the *p*-type semiconductor between the metal and n+ semiconductor is completely depleted, raising  $V_{\text{SIM}}$  will lower the barrier as shown.

The current flowing between the metal-semiconductor contact and electron collector can be described by

1000

$$I = I_0 e^{\Delta \Theta/kT} + I_d, \tag{5}$$

where k is Boltzmann's constant and T is the temperature.<sup>9</sup> The first term is related to electrons ejected over the barrier and the second term is due to current generation within the depletion region (dark current). The  $I_0$  term found in (5) is the current that would flow over the barrier without any barrier lowering and  $\Delta \Theta$  is the amount the barrier has lowered by applying  $\Delta V$  to the electron collector such that  $\Theta_{bi} = \Theta + \Delta \Theta$ , as shown in Fig. 8. The derivative of the current versus this barrier lowering can be written as

$$\frac{dI}{d\Delta\Theta} = \frac{(I - I_d)}{kT}.$$
(6)

In order to obtain resistance over this barrier, we need the derivative of I versus the voltage applied to the electron collector which can be written as

$$\frac{dI}{dV_{\rm SIM}} = \frac{-dI}{d\Delta\Theta} \frac{d\Theta}{dV_{\rm SIM}}.$$
(7)

To obtain  $d\Theta/dV_{\text{SIM}}$ , we need to establish the relationship between  $\Theta$  and  $I_{\text{SIM}}$ . This is done by examining the electric field between the metal-semiconductor contact and the electron collector when the semiconductor between them is depleted. The electric field versus position is illustrated in Fig. 9.

As indicated in Fig. 9, the area under the electric field curve between 0 and W is equal to the height of the barrier  $\Theta$ as shown in Fig. 8 so that we can write

$$\Theta = \frac{qN_A}{\varepsilon_s} \frac{W^2}{2},\tag{8}$$

where q is the electron charge,  $N_A$  the semiconductor doping level, and  $\varepsilon_s$  the permittivity in silicon. The length W represents the distance into the semiconductor that the maximum barrier is positioned. At the point where the area between the nodes is first depleted ( $V_{\text{SIM}} = V_{\text{dep}}$ ), W will be the same as



FIG. 9. Electric field vs position in the depleted region between metalsemiconductor contact and electron collector. As  $V_{\text{SIM}}$  increases, the slope of the electric field  $(-qN_A/\varepsilon_s)$  remains constant and  $\Theta$  decreases.

the depletion depth for an unbiased Schottky contact. As  $V_{\text{SIM}}$  increases beyond this, W will decrease in length, but in most cases the change in W's length will be small since the barrier height will not have to drop very much to account for large changes in ejected current. The area under the electric field between W and d is equal to  $V_{\text{SIM}}$  so that we can write

$$V_{\rm SIM} = \frac{qN_A}{\varepsilon_s} \frac{(d-W)^2}{2}.$$
(9)

Using both (8) and (9) we can write the derivative for barrier height versus  $V_{\text{SIM}}$  as

$$\frac{d\Theta}{dV_{\rm SIM}} = \frac{-W}{d-W}.$$
(10)

To take into account changes in W with current, we can use (5) and (8) to derive the relationship

$$W = \sqrt{\frac{2\varepsilon_s}{qN_A}} \sqrt{\Theta} = \sqrt{\frac{2\varepsilon_s}{qN_A}} \sqrt{\Theta_{\rm bi} - kT \ln\left(\frac{I+I_d}{I_0}\right)}.$$
 (11)

Inserting (11) into (10) we can derive the derivative for barrier height versus  $V_{\text{SIM}}$  that has a current dependent term given by

$$\frac{d\Theta}{dV_{\rm SIM}} = \left(\frac{1}{\{d/\sqrt{(2\varepsilon_s/qN_A)}\sqrt{\Theta_{\rm bi} - kT\ln[(I-I_d)/I_0]}\} - 1}\right).$$
(12)

Substituting the relationships from (6), (10), and (12) into (7) we obtain

$$R_{\text{barrier}} = \left(\frac{dI}{dV_{\text{SIM}}}\right)^{-1}$$
$$= \frac{kT}{I - I_d} \left(\frac{d - W}{W}\right)$$
$$= \frac{kT}{I - I_d} \left(\frac{d}{\sqrt{(2\varepsilon_s/qN_A)}\sqrt{\Theta_{\text{bi}} - kT \ln[(I - I_d/I_0)]}} - 1\right).$$
(13)

The role of space charge must also be considered for the SIM. Space charge resistance is caused by the electric field reduction in a depletion region due to the presence of charge carriers. The field reduction can be expressed as  $\Delta E_m$ 



FIG. 10.  $R_{\text{barrier}} + R_{\text{sc}}$  resistance vs input current between the metalsemiconductor and electron collector. The theoretical curve is calculated using (13) and (14) assuming a vertical SIM device made using a *p*-type epitaxial layer, Schottky injection contact, and a spacing d equal to 4  $\mu$ m. Measured values correspond to fabricated SIM devices with those parameters.

= $Id/(2\varepsilon_0\varepsilon_s vA)$ , where  $E_m$  is the maximum value of the electric field in the depletion region, d is the spacing between the metal-semiconductor contact and the electron collector,  $\varepsilon_s$  is the permittivity in silicon, v the electron drift saturation velocity, and A is the depletion region cross section area.<sup>7</sup> The equation indicates that with higher current flowing inside the diode, field reduction will become larger. The field reduction can also be realized as a corresponding voltage reduction equal to  $d\Delta E_m$ . Therefore, the space charge effect can be represented by an effective space charge resistance,

$$R_{\rm sc} = \frac{d^2}{2\varepsilon_s v A}.$$
 (14)

The cross sectional area in the SIM device<sup>6</sup> can be estimated by the width of the depletion region in the direction perpendicular to the path between the metal-semiconductor contact and the electron collector times the depth of the depletion region.

The magnitude of the two resistance terms  $(R_{\text{barrier}})$  $+R_{\rm sc}$ ) as a function of input current into the SIM was verified by matching measured values with theoretical equations. Substitution of actual device parameters into (13) and (14)yields a theoretical representation of  $R_{\text{barrier}} + R_{\text{sc}}$  versus input current as shown in Fig. 10. For this case,  $d=4 \ \mu m$ , p-type doping equaled  $3 \times 10^{15}$ , and the metal-semiconductor barrier equaled 0.45 eV (Ref. 10) (nickel silicide on p-type silicon). A dark current  $(I_d)$  of approximately 1 nA was used to represent the real device in (13). This dark current term dominates the resistance curve at low currents. At high currents, space charge resistance dominates as R<sub>barrier</sub> drops below  $R_{\rm sc}$ . Calculations for the space charge resistance of the device used in Fig. 10 yield a value of  $R2_{sc} = 12 \text{ k}\Omega$ . Measured  $R_{\text{barrier}} + R_{\text{sc}}$  for the device with the same parameters are also shown in the figure to verify theory. Measurements were made using an HP/Agilent 4156 with a grounded connection to the metal-semiconductor contact while the contact to the electron collector is swept in voltage. The derivative of the

Downloaded 13 Feb 2009 to 128.187.0.164. Redistribution subject to AIP license or copyright; see http://jap.aip.org/jap/copyright.jsp



FIG. 11. Test setup used to measure the frequency response of SIM devices.

measured current versus swept voltage is then used to calculate the total resistance for a given current. The calculated and measured values shown in Fig. 10 match very closely confirming that thermionic barrier emission and space charge are the dominant resistance effects in this particular SIM design (Schottky contact injection on *p*-type semiconductor).

The implications of these resistance terms on the frequency response of this SIM design can be shown by substituting (13) and (14) into (4), resulting in

 $f_{3 \text{ dB}}$ 

$$\approx \frac{1}{2\pi[\{(kT/I - I_d)[(d - W/W)] + (d^2/2\varepsilon_s vA)\}(C_1 + C_{\rm pd})]}.$$
(15)

The frequency response at low input currents is expected to be almost linearly dependent on input current. Given the large barrier resistances, frequency response is also very limited as verified in the next section.

#### V. FREQUENCY RESPONSE MEASUREMENT

Frequency response measurements of SIM devices were done using the test setup illustrated in Fig. 11. In the frequency response test setup, a sinusoidal signal drives an analog transmitter laser source ( $\lambda$ =850 nm), allowing a single harmonic rather than multiharmonic signal to be injected into the SIM and used for frequency response evaluation. The laser passes through an attenuator before reaching a photodiode. This provides a precise method to reduce electron photocurrent injected into the SIM and facilitates the testing of device bandwidth at different but quantifiable current injection levels. A Keithley 2400 voltage-measure unit keeps the *p-i-n* photodiode reverse biased at all times and gives an accurate average measurement of the ac plus dc leaving the photodiode anode  $(I_{pd})$ . The vertical and horizontal fields necessary for impact ionization and depletion are formed as a Keithley 2410 voltage-measure unit reverse biases the semiconductor between the electron collector and hole collector. Current is also monitored using the Keithley 2410 as it flows either through the electron collector  $(I_{\text{SIM}})$  or hole sink  $(I_{\text{sub}})$ . Electron current  $(-I_{\text{SIM}})$  leaving the electron collector passes through a bias tee where the ac and dc components are separated. ac electron current is fed into a femtocurrent amplifier acting as a transimpedance amplifier. This amplifier employs a virtual ground on its input so that none of the ac signal is quenched or diverted through the dc leg of the bias tee by having to pass through a high input impedance amplifier. The current amplifier's constant transimpedance gain of 5  $\times 10^4$  V/A provides a substantial voltage signal that is averaged over several cycles to provide accurate measurement and analysis on an oscilloscope. 3 dB bandwidth is then determined as the frequency where the voltage signal on the oscilloscope falls to  $\sqrt{1/2}$  of its maximum value.

Capacitance parameters necessary to compare measured to predicted bandwidths were obtained using an HP/Agilent C-V plotter 2480A. SIM device terminals were biased to voltages conditions similar to those found in actual operation. For instance, depletion and pad capacitances between the electron collector and hole sink were measured by biasing the junction to potential identical to actual device performance before recording capacitance. The test setup allowed measurement of actual device capacitances with or without stray and additional capacitances caused by probes and substrate electrodes.

Frequency response testing revealed a bandwidth dependent on the amount of photocurrent injected into the SIM as expected from (15). Using the setup illustrated in Fig. 11, several frequency response measurements were made on actual SIM devices at progressively lower injected currents. The SIM was biased to a  $V_{\text{SIM}}$  voltage greater than  $V_{\text{dep}}$  so that the device would produce current gain. However, frequency response measurements were found to be independent of the gain produced in the SIM. This confirms that frequency response limitations for this specific SIM design are due to RC effects and not to impact ionization delay times. The different values of injected current and actual device parameters including measured capacitances  $(C_1 + C_{pd})$ =6.8 pF) were then used in the calculation of frequency response using (15). The total capacitance value also includes stray and additional capacitances from the test probes used in the frequency response measurement. Matching of the actual and predicted values can be seen in Fig. 12. The specific SIM device used was the same one whose measured resistance values are shown in Fig. 10 with dopings and geometry described in the previous section. The close match in both the frequency response magnitude and dependence versus input current confirms the accuracy of the circuit model describing the SIM as well as the effects of the metal-semiconductor contact barrier and space charge on device operation.

### **VI. HIGH SPEED SIM OPERATION**

The measurements of SIM frequency response confirm that for the specific SIM design built on p doped epitaxial layers, response for low input currents is limited by RC effects dominated by the metal-semiconductor barrier. These speed limitations are so severe that transit time and avalanche multiplication delays do not come into play. Transit



FIG. 12. 3 dB frequency response vs injected input current. Theoretical values were generated from (15) and measured values come from measurements on the same SIM device used to generate figure (p-type semiconductor with Schottky injection).

time and avalanche multiplication delays are expected to be in the tens of picoseconds time frame or gigahertz frequency response range for devices with depletion regions of several microns. To be useful in most applications, next generation SIM designs will need to operate at significantly higher frequency responses. While there are a number of possibilities which may enhance overall SIM frequency response major improvements must include modifying the metalsemiconductor barrier in order to drop the effective barrier resistance (even for low input currents) and altering the device geometry to lower the space charge resistance. Optimization of RC parameters must also make account for capacitances which if decreased during barrier and space charge resistance optimization will further enhance overall SIM performance.

# **VII. CONCLUSIONS**

This paper has explored the frequency response of SIM devices presenting a theoretical model for response limits based on resistance and capacitance parameters. One key conclusion is that the resistance due to the metalsemiconductor current injection point can dominate the frequency response. For first generation SIMs built on *p*-type silicon epitaxial layers, this injection point is a Schottky contact with electrons injected into a depletion region through thermionic emission. This creates a very large effective barrier resistance which is inversely proportional to input current. Theoretical models of this barrier resistance along with the resulting frequency response match very closely to measurements for real devices. Frequency responses for first generation device designs are too low for most applications. However, the models and descriptions of device operation contained in this paper provide a clear path forward to increasing the frequency response for redesigned SIMs by decreasing injection barrier resistance and altering device geometries to decrease space charge resistance.

### ACKNOWLEDGMENTS

We gratefully acknowledge financial support for this research through the Raytheon Ideas Program and from the Defense Advanced Research Projects Agency through Grant No. NBCHC050160, directed by Raymond Balcerak.

- <sup>1</sup>J. Campbell et al., IEEE J. Quantum Electron. 10, 777 (2004).
- <sup>2</sup>T. Al-Attar and T. H. Lee, IEEE Trans. Microwave Theory Tech. **53**, 3557 (2005).
- <sup>3</sup>O. N. Jarvis, P. Van Belle, M. A. Hone, G. J. Sadler, G. A. H. Whitfield, F. E. Cecil, D. S. Darrow, and B. Esposito, Fusion Technol. **39**, 84 (2001).
- <sup>4</sup>H.-W. Lee and A. R. Hawkins, Appl. Phys. Lett. 87, 073511 (2005).
- <sup>5</sup>H.-W. Lee, J. L. Beutler, and A. R. Hawkins, Appl. Phys. Lett. **13**, 8760 (2005).
- <sup>6</sup>H.-W. Lee, J. L. Beutler, and A. R. Hawkins, IEEE J. Quantum Electron. **42**, 471 (2006).
- <sup>7</sup>P. Webb, R. McIntyre, and J. Conradi, RCA Rev. **35**, 234 (1974).
- <sup>8</sup>M. J. Van der Tol and S. G. Chamberlain, IEEE Trans. Comput.-Aided Des. **10**, 1015 (1991).
- <sup>9</sup>S. M. Sze, *Physics of Semiconductor Devices* 2nd ed. (Wiley, New York, 1981).
- <sup>10</sup>M. Morschbach, C. Schollhorn, M. Oehme, and E. Kasper, Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 9–11 April 2003, pp. 122–125.