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ANALYSIS AND DESIGN OF LOW-JITTER OSCILLATORS

by

Justin Jennings Fitzpatrick

A thesis submitted to the faculty of

Brigham Young University

in partial fulfillment of the requirements for the degree of

Master of Science

Department of Electrical and Computer Engineering

Brigham Young University

April 2004

BRIGHAM YOUNG UNIVERSITY

GRADUATE COMMITTEE APPROVAL

Of a thesis submitted by

Justin Jennings Fitzpatrick

This thesis has been read by each member of the following graduate committee and by majority vote has been found to be satisfactory.

3/10/04
Date

Donald T. Comer, Chair

3/10/04
Date

David J. Comer

3/10/04
Date

Craig S. Petrie

BRIGHAM YOUNG UNIVERSITY

As chair of the candidate's graduate committee, I have read the thesis of Justin Jennings Fitzpatrick in its final form and have found that (1) its format, citations, and bibliographical style are consistent and acceptable and fulfill university and department style requirements; (2) its illustrative materials including figures, tables, and charts are in place; and (3) the final manuscript is satisfactory to the graduate committee and is ready for submission to the university library.

3/10/04
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ABSTRACT

ANALYSIS AND DESIGN OF LOW-JITTER OSCILLATORS

Justin Jennings Fitzpatrick

Department of Electrical and Computer Engineering

Master of Science

This thesis presents an examination of the jitter performance of different oscillator types in the presence of flicker noise, white noise and power supply noise. Key results are achieved using time domain simulations to determine cycle jitter of several different oscillator architectures, semiconductor processes and component features. In the end, a design procedure is developed for creating a low-jitter oscillator in a TSMC .25μm CMOS semiconductor process.

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I would like to thank Dr. Donald Comer for his extensive help with this thesis. He has shared his intuition and knowledge in the research process. He has also provided needed critique in the writing of this thesis work. Without his guidance the completion of this work would never had happened.

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Chapter 1

Introduction

The spectral purity of a signal represents a critical specification in most communication systems. In order to optimize a design for noise, the traditional method for determining noise has typically relied on frequency domain simulations to discover phase noise. While this offers one view of the noise performance of a circuit, it may not include time domain effects that exist in a real world circuit. Being able to simulate noise in the time domain, a designer would be able to get another picture of the expected performance in the circuit.

One reason designers usually do not simulate noise in the time domain is the inability of commercial circuit simulators to perform that function. This thesis analyzes methods that may be employed to include noise in a transient simulation in modern EDA software. Several oscillators are simulated and characterized according to their cycle jitter performance.

1.1 Contributions of this Thesis

The contributions of this thesis are:

- Developed a simulation method to generate time domain noise in any SPICE simulator. This allows the effects of flicker and white noise to be accounted for along with other time domain noise sources.

- Characterized and compared various classical oscillator architectures for cycle jitter performance based on device noise.
- Analyzed susceptibility of various oscillators to supply noise based upon circuit parameters.
- Demonstrated that passive device tuned oscillators have lower jitter than active device counterparts.
- Characterized CMOS, BJT and HBT oscillator circuits according to transient noise.
- Showed that bipolar devices have less cycle jitter than CMOS devices due to a low flicker noise corner frequency
- Compared the resulting cycle jitter due to supply noise on different voltage supplies.
- Observation of the major contribution of supply noise on oscillator jitter and suggestions for minimization of this effect.
- Procedure to optimize noise of the Colpitts oscillator by following general oscillator design guidelines.

Chapter 2

Phase Noise and Jitter in Oscillators

Noise related measurements represent one of the key parameters used to characterize timing circuits in modern day electronic systems. Noise performance is usually described in terms of phase noise for the frequency domain, or jitter for the time domain. Both terms represent a periodic signal's deviation from the ideal signal in their respective domains. This chapter presents an overview of phase noise and jitter and relates the two domains through mathematical analysis.

2.1 Phase Noise

The power spectrum of a pure sinusoidal signal when observed through a spectrum analyzer would show all of the signal's energy at one carrier frequency as shown in Figure 1. Because of noise distortion, an observed signal usually differs from the ideal case and some of the signal power "bleeds" into nearby frequencies, as shown in Figure 2 [1].

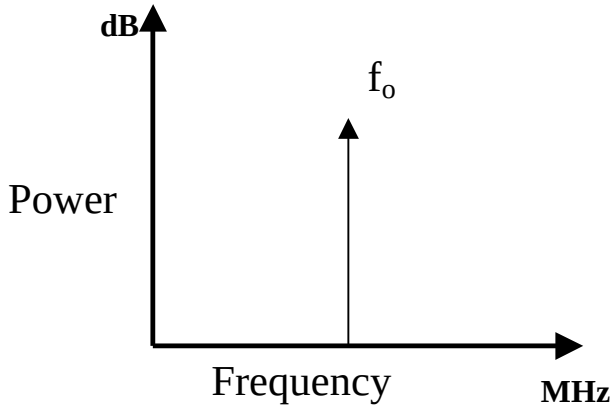

Figure 1 – Spectral density graph for ideal sine wave

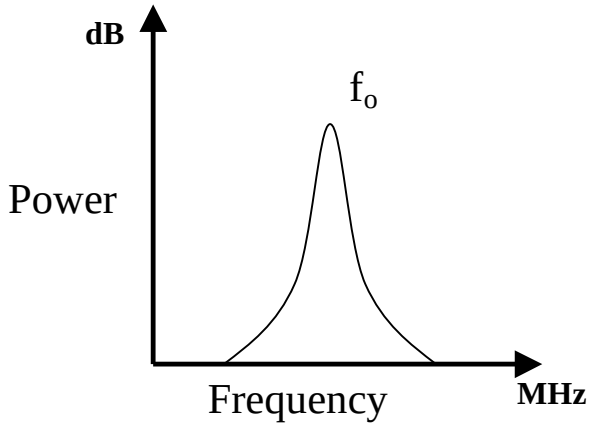

Figure 2 – Spectral density graph for typical sine signal

A representative logarithmic spectral density plot of a free running oscillator can be seen in Figure 3. Typical oscillator noise is divided into two distinct regions, one indicating up-converted flicker noise and the other indicating up-converted white noise. Up-conversion is the result of noise being modulated by the carrier frequency. Flicker noise falls at 10 dB per decade in a typical spectral density plot. When the noise is up-

converted by the oscillation frequency, it is characterized by the spectral density of the oscillator falling at 30 dB per decade [22]. It is often referred to as 1/f noise since it is inversely proportional to the offset frequency from the carrier. White noise refers to the spectral density of noise that is constant over a given frequency range. When this noise is up-converted, it shows a typical falloff of 20 dB per decade. It is also necessary to understand the 1/f noise corner. Frequencies below the 1/f noise corner display flicker noise characteristics. Frequencies above the 1/f noise corner show more of a white noise falloff [2].

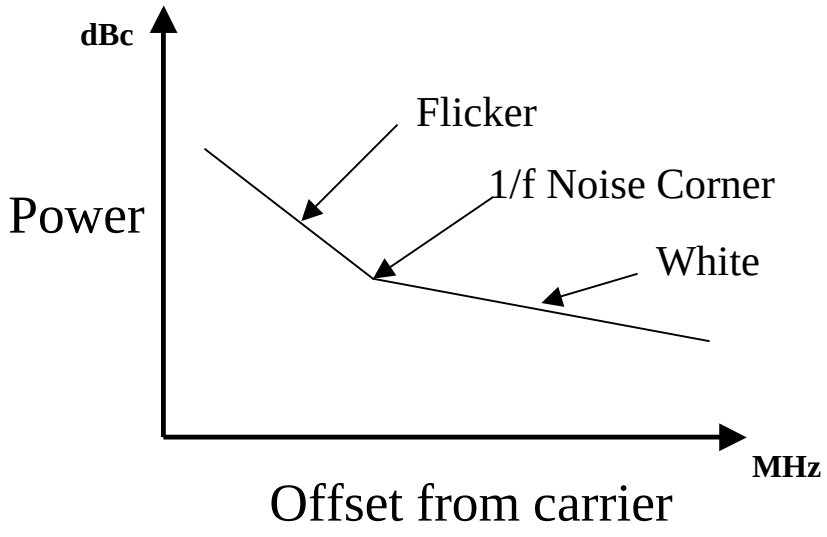

Figure 3 – Spectral density representation of free running oscillator

A perfect sinusoidal signal can be represented in the form:

$$V(t)=V\sin(\omega t), \quad (1)$$

where V is the signal amplitude and ω is the frequency of oscillation in radians per second.

A sinusoidal signal with noise added can then be represented in the following form:

$$V(t)=V(1+\alpha(t))\sin(\omega t+\phi(t)), \quad (2)$$

where a time varying $\alpha(t)$ causes amplitude modulation and $\phi(t)$ causes frequency modulation to the signal.

The functions $\alpha(t)$ and $\phi(t)$ are usually zero-mean Gaussian processes. Additionally, amplitude noise can be ignored by constraining the output swing or removed from the circuit through the implementation of a limiter [3]. The representative sinusoidal equation then is shown as:

$$V(t)=V\sin(\omega t+\phi(t)). \quad (3)$$

The function $\phi(t)$ can also be represented by its power spectral density $S_\phi(f)$. A frequency measurement instrument such as a spectrum analyzer might also show phase noise in terms of $S_\upsilon(f)$, the voltage power spectral density [3]. The ratio of sideband power to the carrier power is also a key parameter used in describing phase noise and is sometimes denoted as $SSCR_{fm}$ (single sideband to carrier ratio) as in [28] or as $(N_o/P_o)_{fm}$ in [3] or $L(f_m)$ as in [4]. All refer to the ratio of noise power in the sideband specified to the power in the signal located at the oscillation frequency.

2.2 Jitter

Jitter is the time domain measurement of noise. In a world without noise, one would know the exact amount of time between different cycles of a signal. Jitter refers to the difference between this expected cycle time and the time it actually takes a signal to complete a cycle. This deviation from an ideal cycle length is illustrated in Figure 4.

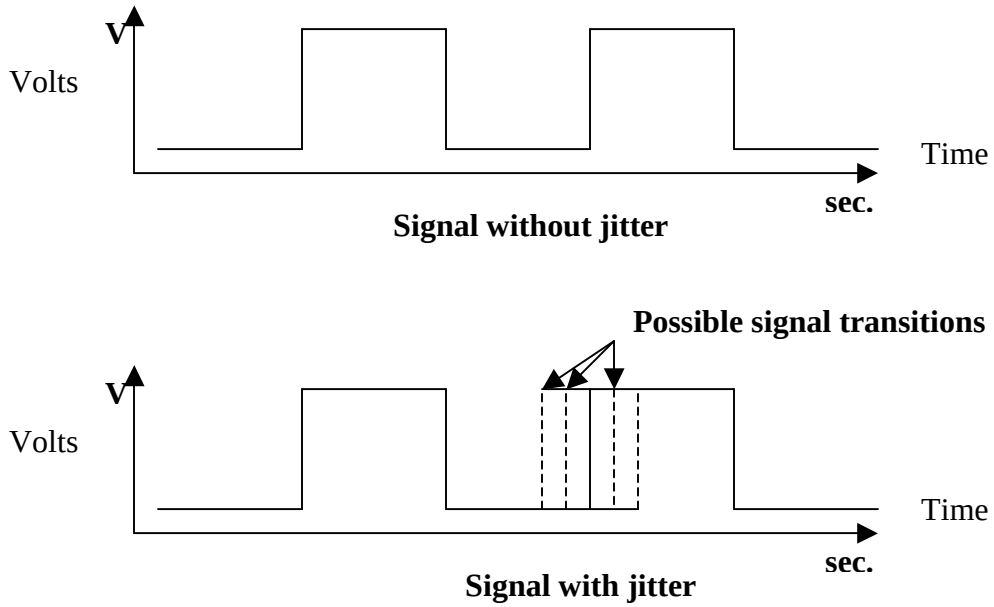

Figure 4 – Representation of ideal signal and signal with jitter

Jitter can be explained through different terms. Herzel [12] explains that there is three different ways to explain jitter more precisely: cycle jitter, cycle-to-cycle jitter and long-term jitter. Long-term jitter, also called absolute jitter, is defined as:

$$\Delta T_{abs}(N) = \sum_{n=1}^{N} \Delta T_n \,, \tag{5}$$

where:

$$\Delta T_n = T_n - \overline{T} \,, \tag{6}$$

in which $\overline{T}$ is the average period of the signal and T_n is defined as:

$$T_n = t_{n+1} - t_n \,. \tag{7}$$

The nth zero crossing of the signal is defined as t_n. Long-term jitter is used mainly in reference to phase-locked loops because $\Delta T_{abs}(N)$ diverges with increasing number of cycles.

Herzel does provide two measurements more applicable to describing oscillator performance. The first, cycle jitter, ΔT_c, is a comparison of individual cycle changes to the average period $\overline{T}$ and is defined as:

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \ . \tag{8}$$

Cycle jitter is useful for showing long term effects in jitter. For showing more immediate changes, cycle-to-cycle jitter is commonly used. Cycle-to-cycle jitter, ΔT_{cc}, is a comparison of one cycle to the preceding cycle and can be described as:

$$\Delta T_{cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (T_{n+1} - T_n)^2} \ . \tag{9}$$

In [3], the authors refer to Herzel's cycle jitter as period jitter and Poore [6] mentioned that Hajimari [13] refers to the above-mentioned cycle jitter as cycle-to-cycle jitter. Future references in this paper to jitter will use the convention that Herzel has proposed.

In [3] and [6], cycle jitter and cycle-to-cycle jitter are also be linked by:

$$\Delta T_{cc} = \sqrt{2}\Delta T_c \ . \tag{10}$$

2.3 Relating Phase Noise to Jitter

Kundert [5] provides a method for determining phase noise from jitter. Previously, Demir [4], showed that the single sideband phase noise $L(f_m)$, also referred to as the Lorentzian spectrum, of a free running oscillator is

$$L(f_m) \approx \frac{c f_o^2}{c^2 \pi^2 f_o^4 + f_m^2}, \tag{11}$$

where f_o is the frequency of oscillation, f_m is some offset from f_o and c is a scalar constant. This equation holds true as long as $f_{corner} < f_m < f_o$. Where f_{corner} is a corner frequency that is defined as:

$$f_{corner} = \pi c f_o^2 . \tag{12}$$

Kundert shows that for an f_m that is larger than the corner frequency, this equation for the Lorentzian spectrum can now be represented as:

$$L(f_m) = \frac{c f_c^2}{f_m^2} \equiv S_{\phi_{FM}}(f_m) . \tag{13}$$

Kundert also relates jitter and the standard period for a free running oscillator according to the equation:

$$J = \sqrt{cT} . \tag{14}$$

where c is derived from the Lorentzian spectrum as in (7). In [3], McCorquodale has shown that manipulation of (13) gives:

$$c = \frac{f_m^2}{f_c^2} L(f_m) \tag{15}$$

and combining (14) and (15) and the fact that period T is the inverse of the frequency of oscillation provide us with the following result:

$$J = \sqrt{\frac{f_m^2}{f_c^3} L(f_m)} = \sqrt{\frac{2 f_m^2}{f_c^3} \left(\frac{N_o}{P_o} \right)_{fm}} . \tag{16}$$

The frequency of reference f_m is usually chosen to be greater than the flicker noise corner frequency as given in (12) and less than the carrier frequency f_o. McCorquodale also explains that this equation does not represent the flicker noise that would exist in the oscillator.

Several attempts [7-11] have been made to combine a Gaussian spectrum representing flicker noise with the standard Lorentzian spectrum to prepare a more accurate spectral representation of oscillator phase noise, which would include the effects of flicker noise on the noise spectrum. These methods are currently not incorporated into commercial software because no analytical expression exists to correctly analyze flicker noise, and in some cases, simulated flicker noise can show greater power in the sidebands than at the carrier signal frequency [6].

Until an analytical model is derived that correctly models flicker noise in the oscillator's phase noise spectrum and is usable in commercial EDA software, the phase noise analysis offered by current simulators is a reasonably accurate approximation of the spectrum.

2.4 Summary

A brief explanation of phase noise and jitter has been given. The two measurement parameters have also been related through analytical expressions when flicker noise is ignored. While commercial simulators are capable of producing a reasonably accurate model for oscillator phase noise, the capability to simulate jitter at the device level has remained elusive to designers.

Chapter 3

Simulation Methodology

Much of the published literature concerning oscillator noise performance has focused on phase noise, as opposed to jitter. Commercial simulators are able to simulate phase noise reasonably accurately, while time domain noise simulation is largely non-existent. While it has been shown that jitter can be approximated from phase noise, no transient effects of jitter can be observed at the circuit level. This chapter outlines three types of noise in semiconductors and proposes several methods to correctly simulate jitter from noise sources at a circuit level.

3.1 Three Types of Noise

Thermal motion of electrons, or holes in a conducting substance, causes thermal noise. The noise has constant spectral density for all frequencies and is a function of the operating temperature. Resistors are a common source of this type of noise [2].

Shot noise is present in any pn junction and is due to sharp changes in the amount of current flowing through the junction. Shot noise is dependent on the quantity of current flowing through the junction and has a constant spectral density for all frequencies. [2].

Flicker noise is the result of charge carriers being stopped in semiconductor material for some amount of time. In order for flicker noise to occur there must be current

flowing through the device. The noise is dependent on frequency and often is referred to as 1/f noise due to the spectral density plot having a 1/f slope [2]. Flicker noise in active devices is usually represented in simulation models by the KF and AF parameters [32].

3.2 Traditional Methods

Behavioral models have been used for some time to model oscillator jitter at a more abstract level. In [14], jitter is modeled in Verilog-A through randomly changing the length of each clock cycle for a VCO. The simulated jitter was within 2dB of the measured result of the VCO. The amount of period variation was determined by running a phase noise analysis first, and then extrapolating jitter, assuming the noise follows a Lorentzian pattern and ignores flicker noise. This method allows for short simulation time and offers an excellent view of general circuit behavior. However, this behavioral simulation method does not allow for the accuracy often required in analog design.

Several other papers [15-17] have added multiple sine waveforms with different frequencies and random phases to produce flicker or white noise. Matlab is used to simulate the waveforms, which are sampled at a given frequency. The sampled data is then imported into a SPICE simulator and a piecewise linear waveform block is used to represent the noise source at the component level.

In this method, the spectral density for each waveform has to be generated prior to incorporation into the circuit. For the noise to not be correlated, different noise datasets have to be generated for each noise source. This can prove to be quite extensive since some components have multiple noise sources as part of their models. In [18], a FET model typically uses three independent noise sources and a BJT model uses six noise sources. Specific noise models for semiconductor components will not be covered in this paper but the reader is directed to [18] for further information on this subject. Therefore,

in order for accurate transient simulation of jitter, large numbers of sampled waveforms are needed even with a relatively small number of components in the circuit using this "Matlab" method.

In [23], a linear time varying theory is used to analyze oscillator jitter also. An impulse response analysis is used to determine possible cycle length fluctuations that contribute to the jitter observed at the oscillator output. This method allows for accurate simulation of jitter but requires some evaluation of devices and can be extremely complex and time consuming for circuits with more than a few devices.

The methods listed above have severe limitations in allowing for general simulation of jitter within circuit systems. Because of this, widespread use of jitter simulation has not been performed. These methods, however, do allow for limited jitter simulation in the time domain.

3.3 Proposed Methods

In order to create a methodology that allows designers to accurately model transient noise at the circuit level, several proposed enhancements are made to the "Matlab" method mentioned above to make it more easily incorporated into designs.

Instead of generating noise specific data in Matlab, a generic "m-file" script was created that would allow for a generic white noise model that could be used in a SPICE simulator. The script may be run repeatedly to allow for the generation of multiple noise datasets. Each dataset can be associated with a different noise source using the circuit simulator. Each of these noise sources has an uncorrelated noise signal. The Matlab code is located in Appendix A.

The Matlab code will generate a stimulus file "data.stl" which will include gaussian distributed values with an average of 0 and a standard deviation of 1. This file is

designed to work with PSPICE Stimulus blocks, but may be modified to work with any SPICE circuit simulator. The spectral density of this circuit in its current form is white. Any spectral density form may be achieved through the use of a Laplace component to modify the frequency content.

This method is then incorporated into a resistor model, as shown in the Fig. 5 below. In [18], the equation for effective noise current $\overline{i_{nR}^2}$ from thermal noise in a resistor is given by:

$$\overline{i_{nR}^2} = \frac{4kT}{R\Delta f}, \tag{17}$$

where k is Boltzmann's constant, T is the temperature in kelvins, R is the resistance value in ohms and Δf is the noise bandwidth.

This equation can then be modeled into the Laplace component as a function of the value of R. This allows for the scaling of the noise according to the value of the resistor; therefore, new Matlab files are not needed with every modification to the resistor size. A transient plot is shown in Fig. 6 along with an FFT plot of the output showing the spectral density in Fig. 7. Also, a parameter to the block can be set up to define which noise dataset to use as the stimulus source.

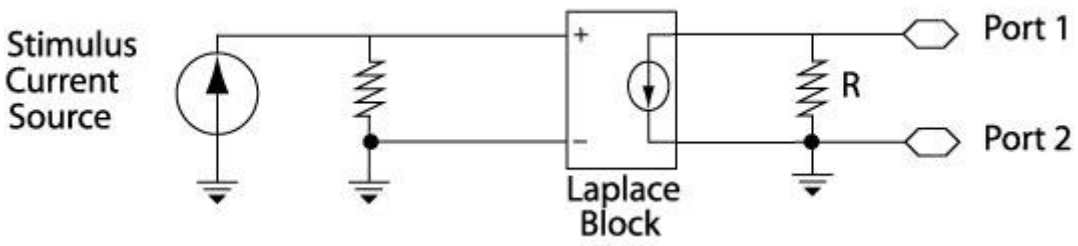

Figure 5 – Schematic representation of resistor model

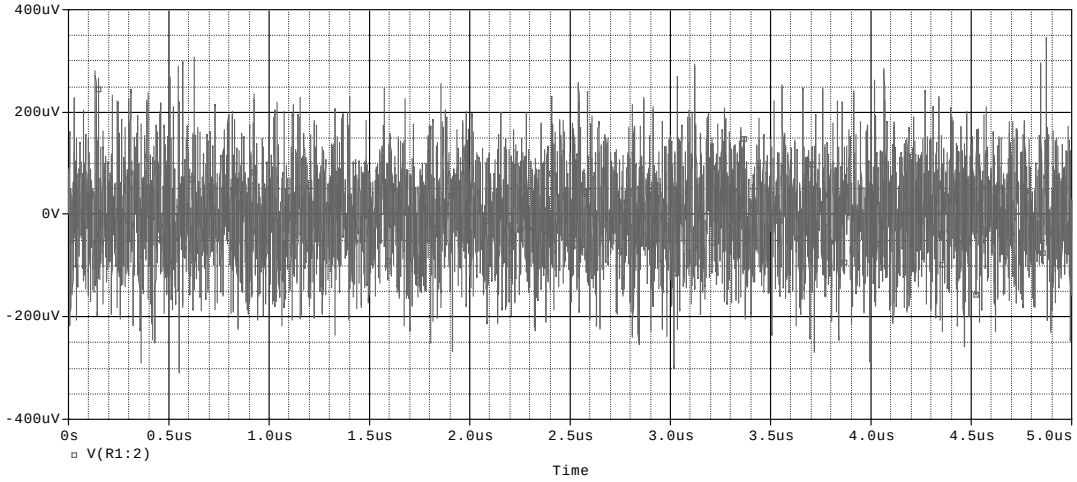

Figure 6 – Transient plot of thermal noise for 1 kOhm resistor

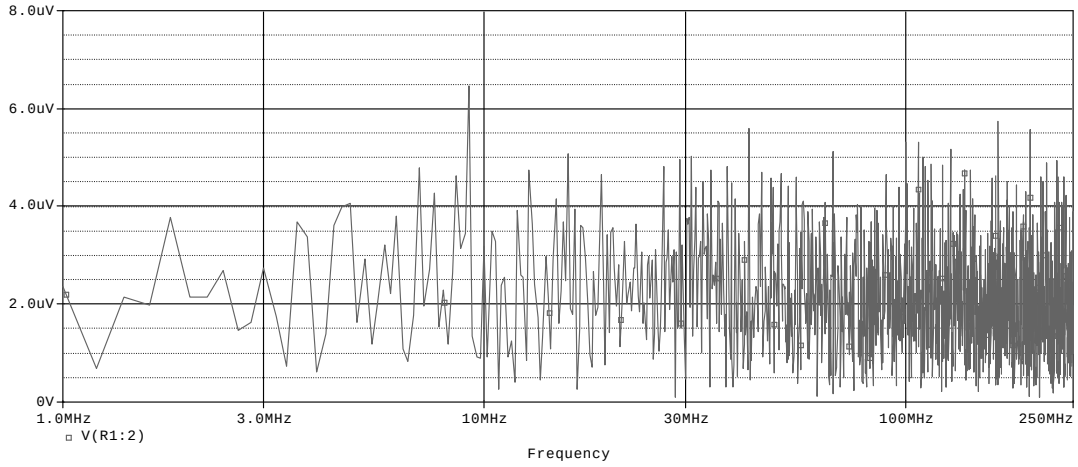

Figure 7 – FFT plot of 1 kOhm resistor thermal noise showing white noise spectral density

While this method is able to generate all types of noise within the circuit, an inherent limitation is the setup work needed to designate each noise source within the circuit. In addition, since noise is theoretically random, the data set for each stimulus noise source would have to be changed with each subsequent simulation run to avoid repeating the same noise effects within the circuit.

Agilent's Advanced Design System (ADS) has incorporated within its software package a transient noise simulator that allows for the simulation of all three types of circuit noise. The amount of thermal noise is generated in relation to the resistance value, and flicker and shot noise are determined by their respective device model parameters. To model substrate and supply noise, various voltage and current sources are available and produce noisy waveforms. ADS also allows for noise levels to be increased for all devices to emphasize the effects of noise on the entire circuit.

Very little has been published using the ADS simulator and its ability to simulate jitter. In [3], ADS was used to simulate transient jitter and was then compared to a phase noise analysis that was performed using Cadence's SpectreRF. Good agreement was found between the two simulated values. Some discrepancy will inherently be included because the jitter is determined from a random process and convergence cannot be completely achieved since only a limited amount of data points can be observed. It was also shown that the cycle jitter has a Gaussian distribution, as would be expected for a typical oscillator.

In order to show a relationship between our method and ADS a 1kOhm resistor was simulated in ADS for its phase noise. The transient plot is shown in Figure 8. As can be seen there is good agreement between our method and the ADS method in results achieved.

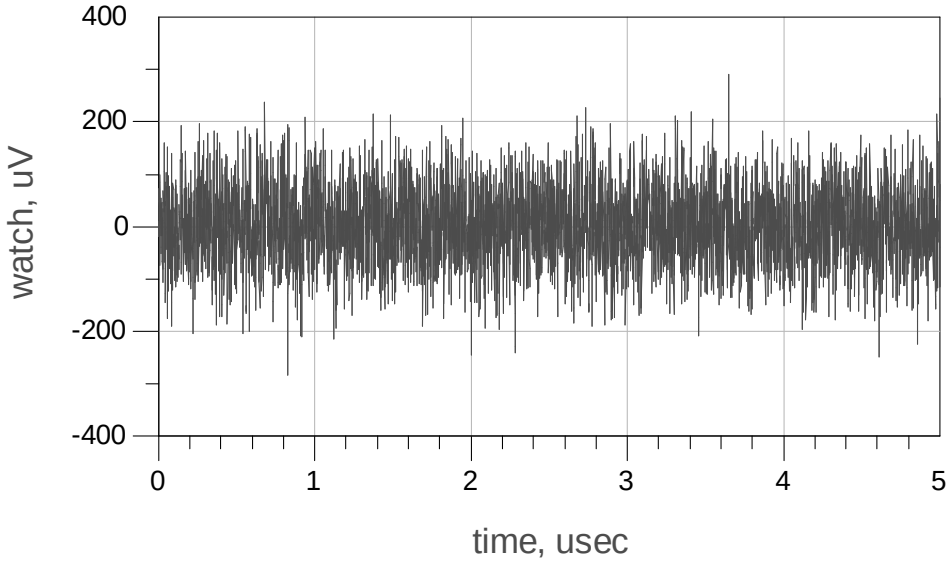

Figure 8 - Transient plot of thermal noise for 1 kOhm resistor in ADS

ADS has several distinct advantages over the methods discussed so far. There is no need for complex mathematical analysis and different noise datasets do not need to be generated using an external program.

Further simulations shown in this work will utilize the ADS simulator. While any of the above methods may be used, the ADS software is accessible on the Brigham Young University network and is efficient for required noise simulations.

3.4 Summary

In this chapter, jitter simulation techniques have been outlined. Already existing techniques to simulate jitter have been looked at. These methods tend to either present only a behavioral look at circuit noise or require extensive calculation and the use of external programs. This complexity doesn't allow them to be utilized on a large scale.

Two new methods have also been analyzed. The first method utilizes an external program, Matlab, but the amount of preparation needed to conduct the simulation has

been reduced. Using this method, several enhancements have been made to other previously proposed methods to allow for easier integration in to the design process. The second method used the transient noise simulator within the ADS EDA software package.

The time domain noise generation is transparent within the ADS software and requires very little settings to be changed within the schematic environment to include noise in a transient simulation. All semiconductor devices with known noise characteristics are available and noise sources can be used to incorporate noise not represented. ADS has another distinct advantage in the fact that no external software is required for the noise generation.

The proposed “BYU” method is more universal in that it can work in any circuit simulator. The method does require more setup and complexity than the ADS simulator. Some of the complexity may be alleviated through the use of a design kit to eliminate some of the redundancy of adding the same noise sources for similar devices.

Good agreement between the two transient simulation methods has also been shown. Which method works best is dependent on the environment. Given certain limitations (available simulator, time, etc.), a specific method may prove to be more advantageous than another. Given the above methods the designer may then choose one that best suits his needs and design methodology.

Chapter 4

Comparison of Oscillator Architectures for Jitter Performance

As has been noted previously, research into oscillator architectures in the past has concentrated on frequency domain analysis. Based on the mathematical link between the two domains, it is generally accepted that lower phase noise results in lower jitter. Without commercial software available for transient noise simulation, frequency domain simulations were the best methods designers had to verify their timing system's performance. As a result, the effects of time domain noise not shown in the frequency domain have largely gone unrecognized. This chapter analyzes standard oscillator architectures and shows sample results, which determine the cycle jitter of standard oscillator architectures in the presence of various noise sources. These designs are to represent examples of typical oscillators and are used to provide a general reference of jitter performance for common oscillator architectures.

In this chapter, five different CMOS architectures are presented and characterized according to their period jitter. The five types of oscillator architectures that will be tested are: Colpitts, Hartley, Delay Line, Ring, and Active Inductor. The TSMC .25μm CMOS process is used for active devices. Two different noise situations will then be used to test each circuit. The first is with only device noise included. The second situation includes the modulation of the supply voltage with a sinusoidal signal that causes the supply

voltage to deviate plus/minus five percent from its nominal DC value. All oscillators are designed to oscillate at a frequency close to 1 GHz. The sinusoidal noise on the supply is running at 50 MHz.

4.1 Colpitts Oscillator

The Colpitts Oscillator is a LC Oscillator circuit characterized by a tapped capacitor configuration [38]. It is common in high frequency communication applications because of low phase noise and the ability to oscillate at high frequencies. Another advantage of the Colpitts oscillator in semiconductor design is that the oscillator tends to require less chip area than most of the other passive device oscillators. A simplified schematic is shown below in Figure 9.

4.2 Hartley Oscillator

The Hartley Oscillator is another LC Oscillator, but is characterized with a split inductor configuration [38]. Like most LC type oscillators, it tends to have lower jitter than active device oscillators. In semiconductor processes, this architecture is not as common as the Colpitts oscillator, mainly because the higher amount of chip area required as a result of the extra inductor. Figure 10 shows a simplified model.

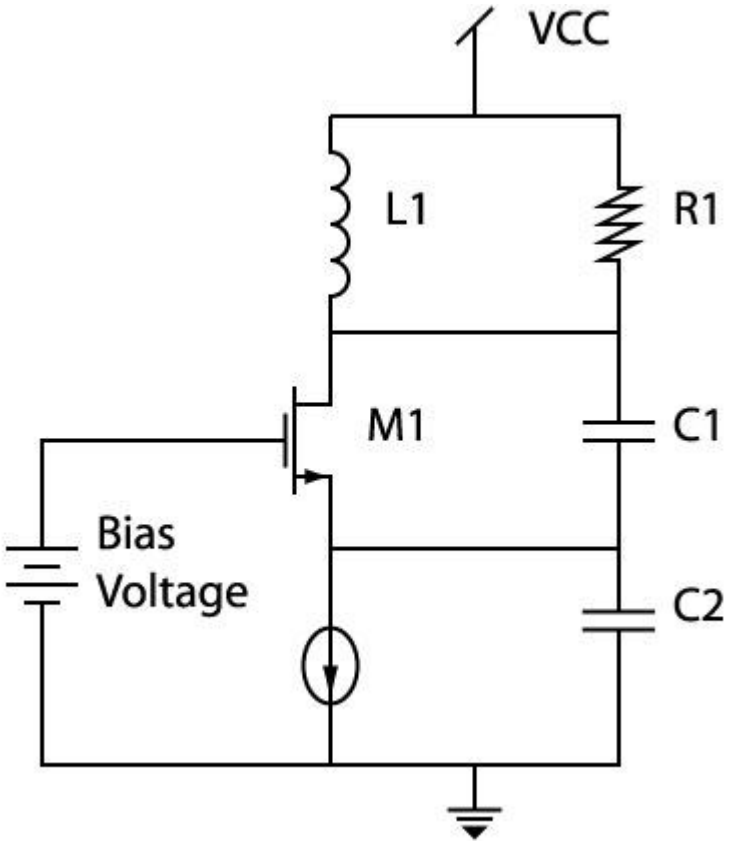

Figure 9 – Schematic of Colpitts oscillator

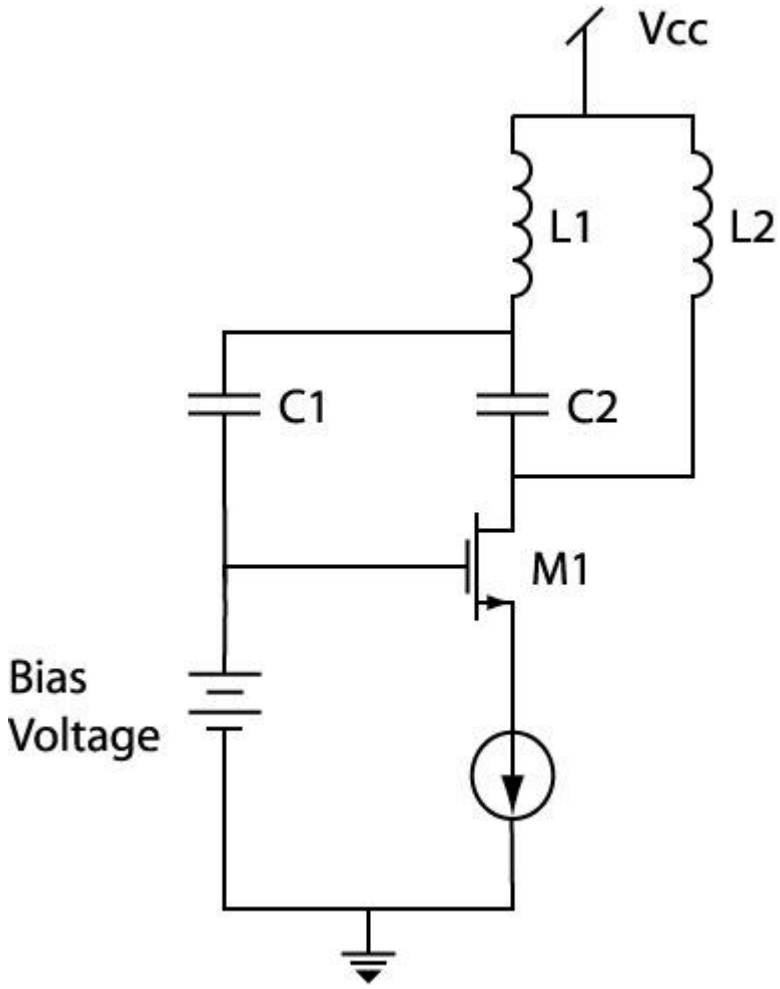

Figure 10 – Schematic of Hartley oscillator

4.3 Delay Line Oscillator

The Delay Line Oscillator is another passive device architecture comprised of a gain stage and feedback stage through transmission lines [39]. This is not a common oscillator architecture either, mainly because of the large chip area required by lengthy transmission lines. However, it is a basic architecture used in surface acoustic wave (SAW) oscillators. The length of the delay lines determines the frequency of oscillation. As the center frequencies of oscillators get larger, the length required for the transmission

line gets smaller, so this oscillator may gain wider application as circuit speeds increase. A simplified schematic is shown below in Figure 11.

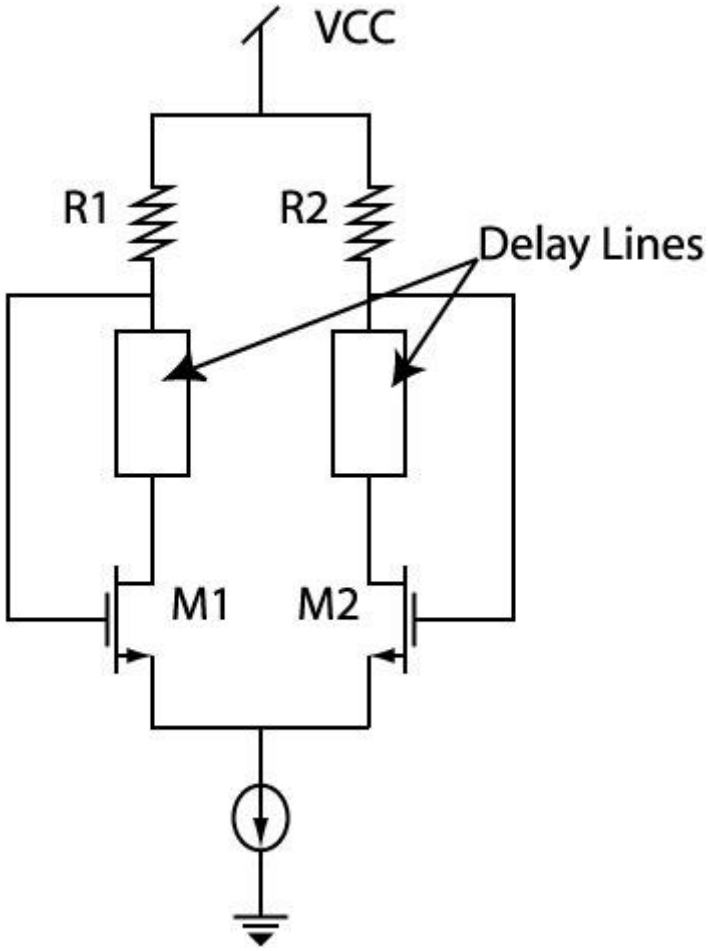

Figure 11 – Schematic of delay line oscillator

4.4 Ring Oscillator

The Ring Oscillator is another common oscillator architecture typically found in digital systems [24]. It is comprised of an odd number of buffer stages, each of which adds a time delay in the feedback path. The inverse of this time delay provides the frequency of oscillation. Ring oscillators are simple structures and are known for having

higher phase noise than the passive device oscillators. A simplified schematic of one buffer stage is shown in Figure 12. The circuit that was implemented for this thesis includes three buffer stages.

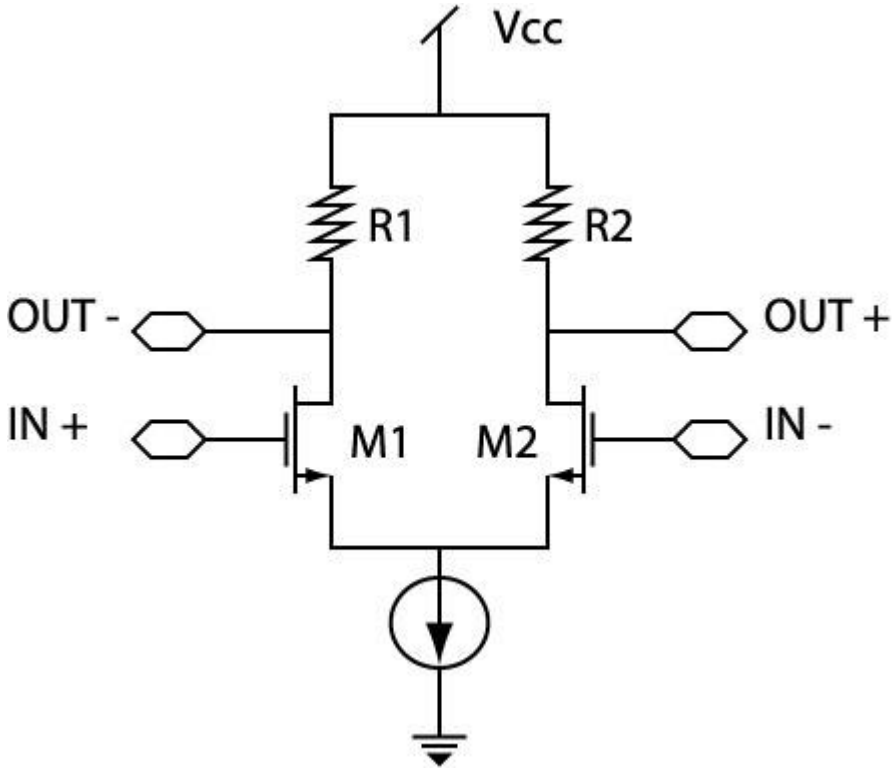

Figure 12 – Schematic of ring oscillator buffer stage

4.5 Active Inductor Oscillator

There are several active inductor or gyrator designs in use today. In this circuit, active devices are used to create a negative resistance and a gain stage. Where the negative resistance has the highest impedance determines the frequency of operation. The actual circuit simulated is a variation of active inductor oscillators recently published [33-35]. A simplified schematic is shown in Figure 13.

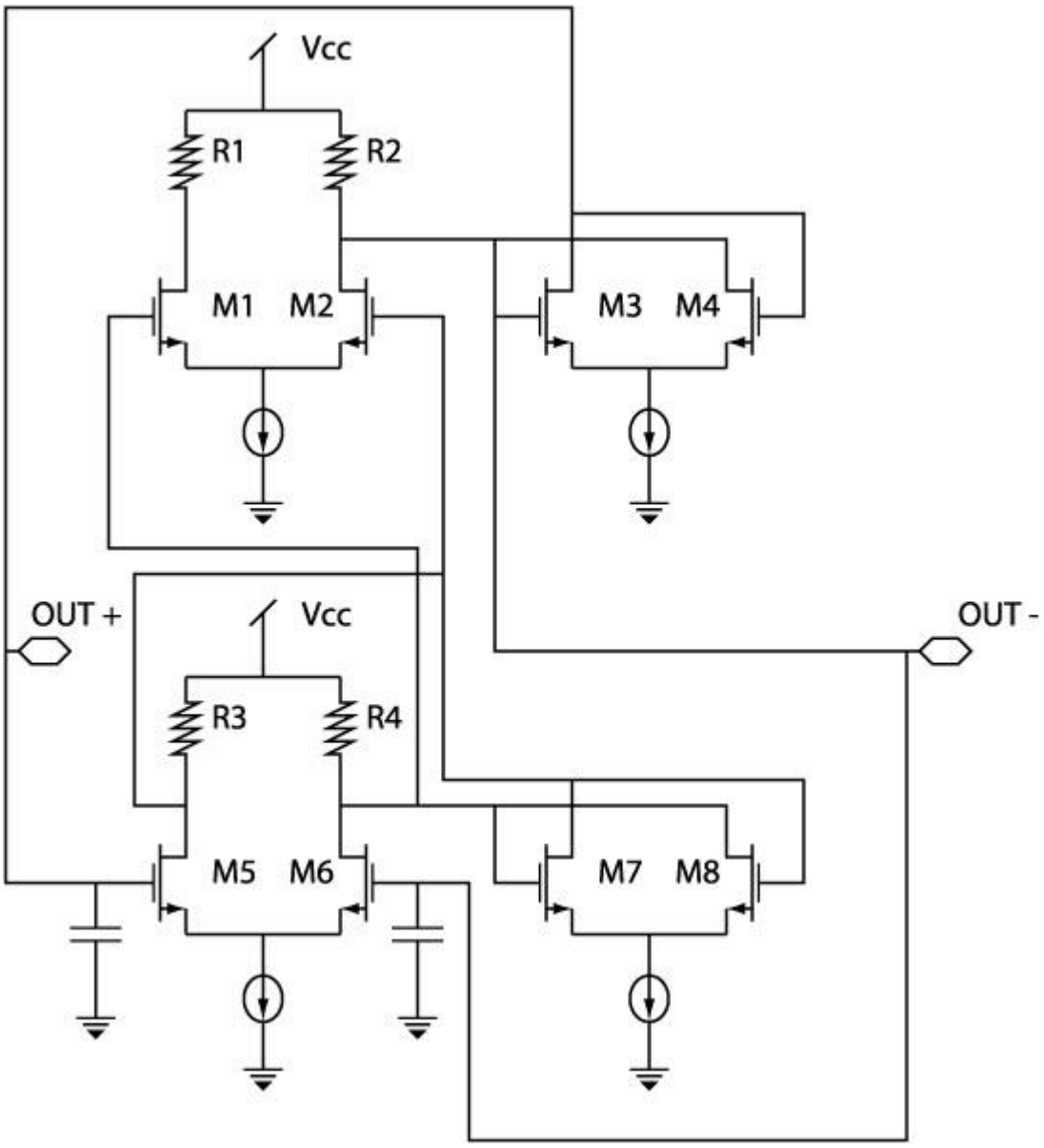

Figure 13 – Simplified schematic of active inductor oscillator

4.6 Simulation Results

All five oscillators were simulated to determine their jitter in two different noise situations. The first case involved the simulation of only device noise in the circuit, generally resulting from resistors and active devices. The second case involved the addition of a 50 MHz sinusoidal noise source that had ±5% voltage swing added to the

positive supply voltage. Cycle jitter was measured only single-endedly at the output of each circuit. The results also include the output voltage swing and the frequency dependence on supply voltage fluctuations. The frequency dependence of supply voltage is measured as the inverse of the time between the zero crossings of the signal given that the zero reference point is determined by the average value of the entire measured signal. The results are tabulated in the Table 1.

Table 1 – Results from transient noise simulation of oscillator architectures

Oscillator Type	Cycle Jitter w/o supply noise (sec.)	Cycle Jitter w/ supply noise (sec.)	Output Voltage Swing (Volts)	Frequency Dependence on Supply Voltage (MHz/Volt)
Colpitts	6.85E-15	3.41E-12	6.95	26.5
Hartley	3.05E-14	4.56E-12	1.53	38.7
Delay Line	1.39E-14	3.65E-12	0.45	26.7
Ring	2.22E-13	1.30E-11	1.48	103
Active Inductor	1.31E-12	3.64E-11	0.21	475

In general, the oscillators utilizing passive devices are less prone to suffer from device or supply voltage noise. Of these, the Colpitts oscillator had the lowest cycle jitter. In addition to having higher device noise from more active components, the two active device oscillators are more susceptible to noise in the supply, and as a result, suffer greater output frequency modulation by the supply noise. This higher jitter is a result of greater changes from the DC bias conditions for the active devices causing changes in operation and performance speed.

These results agree with general assumptions that have been made from conclusions obtained through phase noise simulations in the frequency domain. The results also show why the Colpitts oscillator is often a popular choice among analog designers for its noise performance in addition to more favorable physical layout characteristics.

The other passive device oscillators, Hartley and Delay Line, also showed low jitter for both noise cases, but they are probably not as widely used in integrated circuits as the Colpitts because of larger chip area required for the inductors or transmission lines.

The ring oscillator is often a popular choice for oscillators in digital designs despite its higher cycle jitter as shown in the simulations. While cycle jitter is almost 2 orders of magnitude larger than the Colpitts design, it does not require the large chip area used by large passive devices such as an inductor or even a capacitor. This makes it suitable for designs with space restrictions and higher acceptable jitter.

The active inductor circuit also showed high cycle jitter. This is probably due to the large amount of active devices required for operation. Efforts are currently being made to further lower the phase noise of this oscillator [26-27].

It should be noted that the ring and active inductor oscillators are also very susceptible to supply noise variations compared to their passive device counterparts. This can be seen in both the cycle jitter but also the output frequency sensitivity. For minimization of this supply noise sensitivity, all oscillators should be powered as much as possible through a separate supply bus than other circuitry or compensated in some manner to reduce this effect.

4.7 Summary

In this chapter, several general oscillator designs are simulated in the time domain to determine cycle jitter. Each oscillator architecture was simulated for two noise situations: first, with only device noise present and second, with additional supply noise added.

Based upon these results, a good oscillator for a low-jitter application would be the Colpitts oscillator. It had the lowest cycle jitter for both noise cases tested. The

Hartley and Delay Line oscillators also had low jitter and should be useful in many applications.

The ring oscillator had the best cycle jitter of the two active device oscillators tested. Despite the higher phase noise when compared to passive device oscillators, the ring oscillator requires very little chip area and therefore will continue to be used in integrated environments. The active inductor oscillator was measured with the highest jitter. This is a relatively new oscillator and development work still continues on this oscillator to lower its cycle jitter.

In general, passive device oscillators have less cycle jitter than those oscillators relying more on active devices. The lower cycle jitter is due to a combination of less cycle jitter from active devices, but also the frequency sensitivity to supply noise is less for the passive devices. Passive device oscillators will not work in all cases given other constraints in the circuit such as chip area. A designer would have to choose the oscillator architecture that best meets the design requirements.

Chapter 5

Comparison of Cycle Jitter of Semiconductor Processes

It has long been known that bipolar processes generally have a lower noise figure than a MOSFET process. For integrated communication circuits with low phase noise constraints, bipolar designs have usually been implemented.

One of the most important noise characteristics when comparing the noise figure of bipolar to MOS devices is that the bipolar device's flicker noise corners are usually below 500 Hz while the CMOS noise corner is typically around 1 MHz and might be as high as 10 MHz [20,21,36]. This quality of bipolar designs leads to less observed phase noise in frequency domain simulations.

Sometimes requirements are specified according to jitter instead of phase noise. A designer might be able to extract some information from a phase noise plot, but as has been described earlier, the analytical conversion ignores flicker noise. Flicker noise is a key characteristic, however, between these two processes. To be "safe," the designer might make the design in a bipolar process and rely on the odds that it will meet specification based on the assumption that there should be less jitter. However, the bipolar process is often times more expensive and offers no guarantee that the jitter specifications will be met even then.

Being able to simulate test circuits in the time domain would allow the designer the chance to verify that his circuits meet the system requirements before having to go through an expensive fabrication process. Having the ability to test these circuits in the time domain would allow the designer the ability to observe if a cheaper CMOS process would meet specifications or if the bipolar process would be required or capable of even meeting the design requirements.

An example oscillator will be tested using active devices from three typical processes. The oscillator is similar to the Colpitts oscillator that was tested in Chapter 4 and is shown in Figure 9. The design in this chapter has been modified with the addition of a buffer to drive a 50-Ohm load. A simplified schematic is shown in Figure 14. This oscillator circuit was chosen because it allows for minimal adjustments to be made to the rest of the circuitry when the active devices are changed. The oscillator is designed to operate at a center frequency of 1 GHz. Similar to the tests in Chapter 4, there will be two noise situations tested for each semiconductor process, one with only device noise and the second with supply noise added.

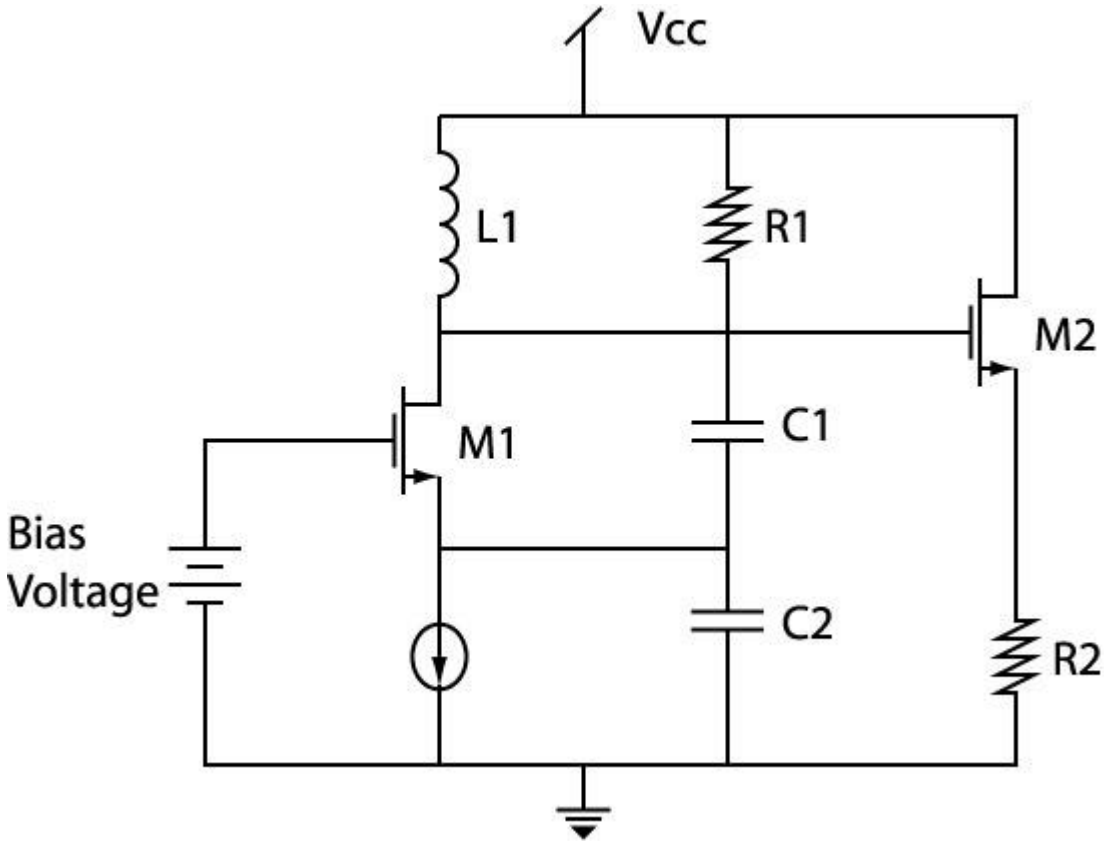

Figure 14 – Colpitts oscillator with buffer stage

5.1 Processes

The three processes that will be analyzed are CMOS, HBT, and silicon BJT. Flicker noise parameters for a typical CMOS process are taken from the TSMC documentation for the .25 um process [19]. CMOS devices are represented by model parameters specified in the .25μm TSMC documentation. The SiGe HBT and Si BJT flicker noise parameters are derived from flicker noise corners recorded in [20]. In [21], the equation to generate the KF parameter from the flicker noise corner frequency f_{flk} is given as:

$$f_{flk} = \frac{K_f}{2q(1+1/\beta)}, \tag{18}$$

where q is the charge of an electron and β is the forward current gain of a bipolar transistor.

Given noise corners of 373 Hz for SiGe and 480 Hz for Si, the KF parameters are .12E-15 and .15E-15. The model parameter AF is assumed to be 1. For the bipolar circuits, all other parameters are left at their default model parameter settings.

5.2 Simulation Results

All three processes were simulated first with only device noise present. The tests were then repeated to include a 50 MHz sinusoidal noise signal on the output node. This added noise modulates the supply voltage plus/minus five percent. Cycle jitter was only measured on a single output node. The results are tabulated in Table 2.

Table 2 – Results from transient noise simulation of semiconductor processes

Process Type	Cycle Jitter w/o supply noise (sec.)	Cycle Jitter w/ supply noise (sec.)	Output Voltage Swing (Volts)	Frequency dependence on Supply Voltage (MHz/Volt)
TSMC .25um	2.64E-13	3.54E-12	0.213	29
SI BJT	3.30E-14	1.03E-11	0.183	86.5
SiGe HBT	3.47E-14	1.03E-11	0.183	83.6

The tests conducted with only supply noise present show that the bipolar devices have lower cycle jitter when only device noise is being simulated. Without a method to simulate both supply noise and device noise in the transient domain, the designer might also conclude that the bipolar design would have lower cycle jitter when supply noise is added based solely on the phase noise simulation. As can be seen from the results, this is not always the case. When supply noise is added to the circuit, the bipolar oscillators have a much higher cycle jitter. The frequency dependence on supply voltage is

approximately three times greater for the bipolar oscillators, leaving these oscillators more susceptible to supply noise.

The results also show very little difference between the two bipolar processes. In actuality, the flicker noise corners for the Si and SiGe devices do not differ greatly [20], leading to similar noise results when simulated. These devices show less device noise than the CMOS devices when simulated with only device noise, but often more factors have to be analyzed in the design of the circuit.

5.3 Conclusion

A simple transient analysis of different processes shows that bipolar processes often have less noise than the MOSFET counterpart. In our simulation of the Colpitts oscillator with only device noise present the MOSFET circuit had about 7.5x greater jitter than the bipolar designs. Because of results like this, a bipolar oscillator is often believed to have lower phase noise than a CMOS oscillator.

In real world applications there are many more effects in the circuit, which influence performance. In our tests, it is shown that in the given configuration the bipolar design is much more susceptible to supply noise variations and has 3x greater jitter for the given sinusoidal supply noise. This shows that general assumptions do not apply in every case and often times there are more circuit effects that also need to be taken into consideration.

By simulating the oscillators in the time and frequency domains, a designer could make appropriate design decisions given the extra information that a simulation in the time domain might provide. In addition, the results seen in this chapter show that a designer cannot make general assumptions on oscillator performance without analyzing the complete environment the circuit will operate in.

Chapter 6

Influence of Supply Voltage Variations on Oscillator Noise

As seen from results observed thus far, supply noise can greatly affect oscillator noise. This chapter analyzes how a parameter, the inductor Q, influences the effects of supply noise on the oscillator's noise performance. In addition, this process shows how one may observe the noise given a certain parameter within an oscillator and optimize the circuit accordingly. The CMOS Colpitts oscillator used in Chapter 4 and shown in Figure 9 will be used as the test circuit in this chapter.

6.1 Supply and Substrate Noise

The simulations involving supply noise so far have involved the use of a sinusoidal noise signal. The purpose of this signal is to modulate the supply noise plus/minus five percent at a constant frequency. A random noise source will also be added to the supply noise signal. This noise source will have a white spectral density. It has zero mean and a standard deviation of 18mV, about .5 % of the DC supply voltage.

The first tests performed are designed to show what effect the circuit/Inductor Q would have on reducing noise. It is assumed that the capacitor Q is greater and the inductor Q has more influence on circuit performance. The circuit Q is determined from the impedance observed at frequencies around the center frequency of operation. Q can be calculated from the following equation:

$$Q = \frac{f_0}{\Delta f} \tag{19}$$

where f_0 is the center frequency and Δf is the bandwidth between the 3dB points on the impedance plot. The inductor Q is a term referencing the ideality of the inductor [37].

For each inductor Q setting, the circuit Q was calculated. In addition, four noise situations were simulated:

1 Device noise only

2 Device noise with white noise signal on supply

3 Device noise with sinusoidal noise signal on the supply

4 All three noise signals (device, white, sinusoidal) present

The results are shown in Table 3 below.

Table 3 – Transient simulation results with additional supply noise

Inductor Q	Simulated Q	Output Swing (Volts)	Cycle jitter with device noise only (sec)	Cycle jitter with additional white noise (sec)	Cycle Jitter with additional sinusoidal noise (sec)	Cycle Jitter with all noise sources (sec)
10	37.6	3.272	6.32E-15	1.00E-12	2.40E-12	2.57E-12
15	16.89	4.127	4.87E-15	7.89E-13	2.34E-12	2.45E-12
20	12.92	4.491	4.37E-15	7.98E-13	2.40E-12	2.60E-12
25	11.41	4.704	5.38E-15	7.85E-13	2.47E-12	2.64E-12
30	10.91	4.847	6.49E-15	7.20E-13	2.51E-12	2.65E-12

As can be seen by these results, the circuit Q decreases with increasing inductor Q. This is due to the fact that this configuration of the Colpitts oscillator is a negative resistance oscillator. Cycle jitter with only device noise is shown in Figure 15. As can be seen by the plot, this noise appears to be lowest with an inductor Q around 20. With the addition of white noise, there is a steady improvement in cycle jitter with higher inductor

Q as seen in Figure 16. When sinusoidal noise is added to the circuit, cycle jitter is lowest with as inductor Q of 15, but it steadily rises as the inductor Q gets larger. This is shown in Figure 17. Figure 18 shows that with all noise sources added, the jitter is minimized at an inductor value of 15. It should be noted that cycle jitter with all noise sources is just the square root of the sum of the noise variances.

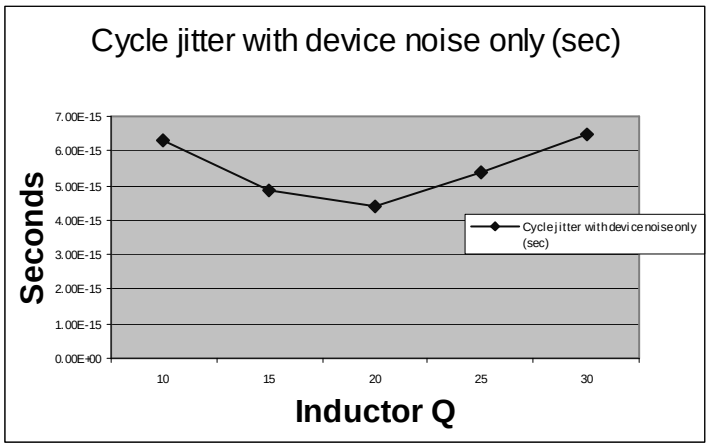

Figure 15 – Cycle jitter with device noise only

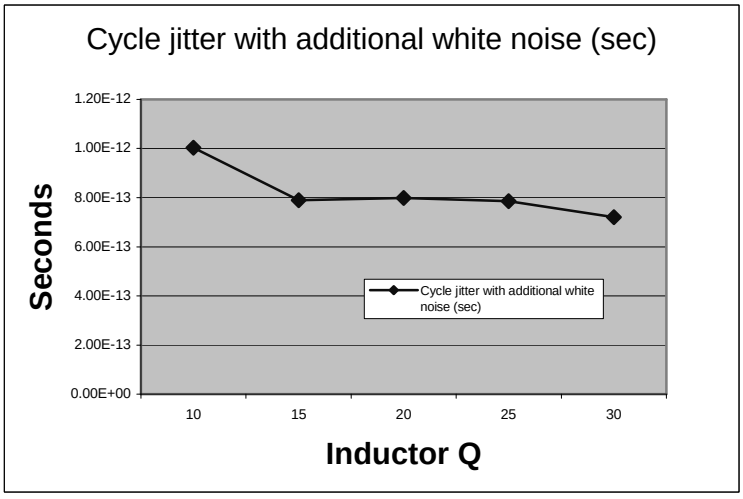

Figure 16 – Cycle jitter with additional white noise on supply voltage

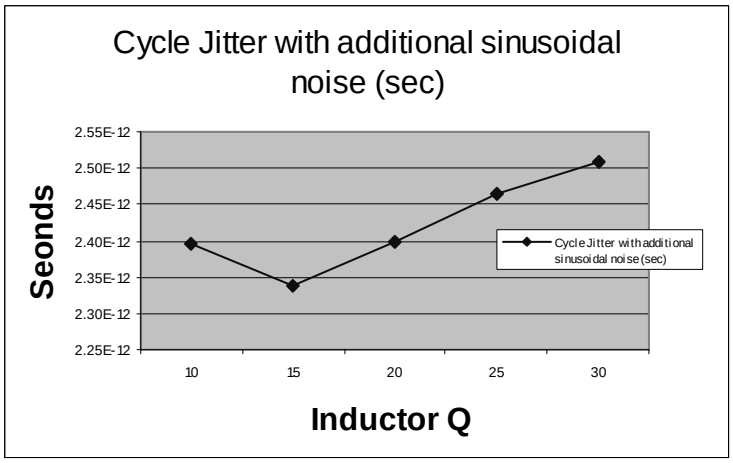

Figure 17 – Cycle jitter with additional sinusoidal noise on supply voltage

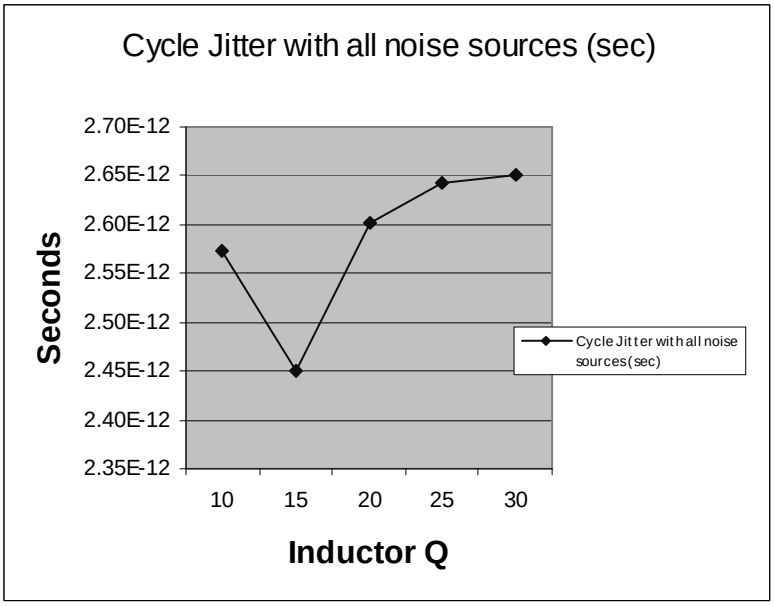

Figure 18 – Cycle jitter with all noise sources included

Following intuition, one would expect that a higher inductor Q would lower phase noise and cycle jitter of the circuit. As the results show, this is not always the case. To further test this principle, the sinusoidal frequency of the noise is changed to match the

oscillation frequency of 1 GHz. Simulation results for each inductor Q are shown in Table 4 and can be seen in Figure 19.

Table 4 – Cycle jitter with sinusoidal supply noise at 1 GHz

Inductor Q	Simulated Jitter with additional Supply Noise (sec)	Simulated Jitter with additional Substrate and Supply Noise (sec)
10	4.65E-15	7.38E-13
15	4.70E-15	6.72E-13
20	4.75E-15	6.73E-13
25	4.76E-15	6.40E-13
30	4.80E-15	6.76E-13

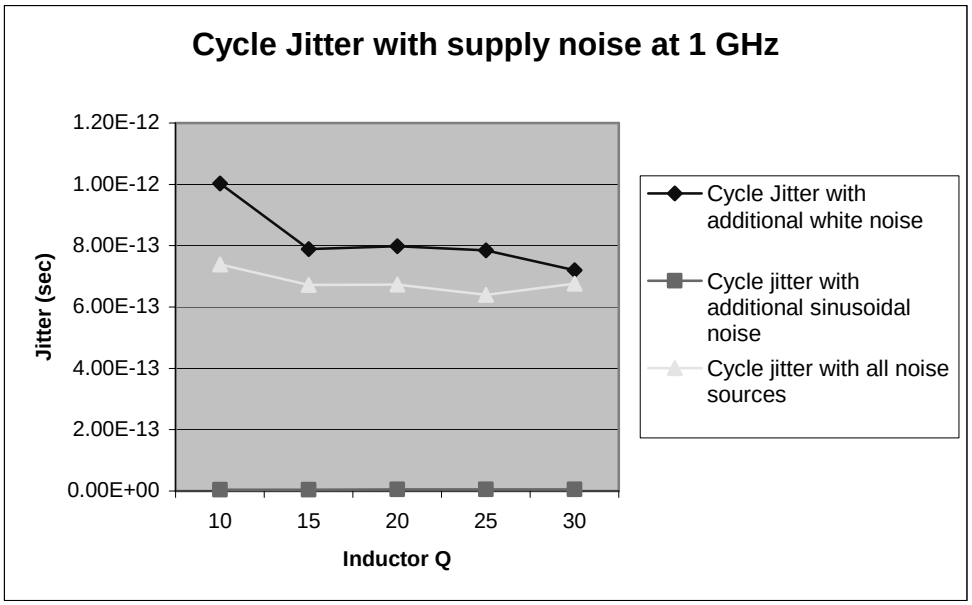

Figure 19 – Cycle Jitter with sinusoidal supply noise at 1 GHz

As seen in the results when the sinusoidal noise signal is “phase locked” with the oscillator and is running at the same speed as the oscillator the noise caused by the sinusoidal signal is drastically reduced. A typical application in which this occurs might

be a circuit such as a phase-locked loop, which might use two oscillators running at roughly the same oscillation speed, and both are usually phase locked to each other. Because the modulation from the sinusoidal signal is reduced, the cycle jitter is largely determined by the white noise. Because the cycle jitter from white noise is reduced, as the inductor Q gets larger, cycle jitter with all noise sources present tends to be reduced.

Another test was run to see what occurs when the phase noise is running at a speed much greater than the center frequency of the oscillator. In this case the sinusoidal noise is running at 10 GHz. A summary of the results is shown in Table 5 and a graphical representation is shown in Figure 20.

Table 5 – Cycle jitter with sinusoidal supply noise at 10 GHz

Inductor Q	Simulated Jitter with additional sinusoidal nise (sec)	Simulated Jitter with additional Substrate and Supply Noise (sec)
10	9.20E-14	9.82E-13
15	7.78E-14	7.99E-13
20	7.71E-14	7.65E-13
25	7.78E-14	7.46E-13
30	7.79E-14	7.13E-13

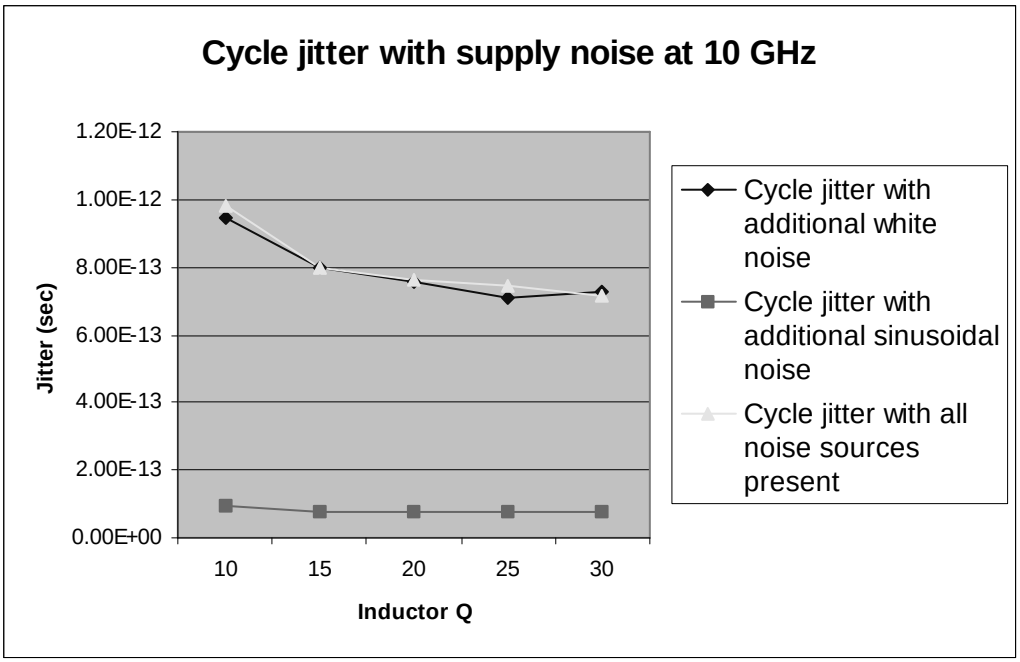

Figure 20 – Cycle jitter with sinusoidal supply noise at 10 GHz

Similar to the previous test, the sinusoidal noise effect is drastically reduced when running at a frequency that is greater than the center frequency of the oscillator. Again, the cycle jitter from the white noise is larger and affects the cycle jitter of the oscillator more. This results in the cycle jitter of the oscillator falling as the inductor Q gets larger.

6.2 Conclusion

In this chapter, several simulations are run to show the effect of the inductor Q on the circuit performance. In the given Colpitts circuit, it has been concluded that a higher inductor Q results in less cycle jitter generated from white noise in the power supply.

The supply noise has a slightly different effect on circuit jitter. If the sinusoidal noise modulating the supply is at a lesser frequency than the oscillation frequency the cycle jitter generally appears to increase with increasing Q. When the sinusoidal noise is

at the same frequency or higher frequency than the center frequency of the oscillator, the supply noise has much less of an effect on the jitter of the circuit.

To explain why this occurs, it should be noted that a high inductor Q would try to hold its operating point more stable. When the frequency of noise is equivalent to or a higher frequency that is a multiple of the oscillation frequency, every cycle of the oscillator will in essence be “phase-locked” to a portion of the sinusoidal noise frequency and each cycle of the oscillator will occur when the sinusoidal noise is at the same voltage point.

For sinusoidal noise frequencies less than the frequency of operation, the signal is no longer “phase-locked” but each oscillator cycle occurs at a different phase of the noise signal. As a higher Q inductor will try to hold its DC value, the tank DC voltage will tend to follow the sinusoidal noise frequency closer than in a low Q circuit. Since the cycle jitter measurement is calculated from the mean of the entire signal, the zero crossing of each cycle occurs with a different DC value compared to the average of the entire signal. If the measurement were made from the zero crossing of one cycle to the next, the jitter measurement would be expected to decrease with higher inductor Q similar to the white noise results.

This chapter has shown how time domain noise simulation may be used to prove that a higher inductor Q tends to reduce the cycle jitter caused by supply noise. An equivalent process could be done to analyze any part of the circuit. The information collected from time domain simulation can either supplement knowledge from the frequency domain or be used alone to allow a circuit designer to optimize the circuit under development.

Chapter 7

Supply Noise Considerations

One of the greatest advantages in time domain noise simulation is the ability to observe the effects of supply noise on cycle jitter. As has been shown in earlier chapters, sinusoidal supply noise modulating the signal can increase cycle jitter by a few orders of magnitude. This chapter examines the effect of varying supply noise on standard oscillator architectures in greater detail.

Typically, the supply noise on a chip will affect both the positive and negative supplies. A proposed method to represent this noise would be to fix one supply voltage at a DC value and represent the cumulative noise in the two signals on the other supply voltage. In the first part of this chapter, several oscillators are analyzed in an effort to determine how much discrepancy modeling the cumulative noise on only one power supply generates.

The circuits that will be tested are the Colpitts, Hartley, Delay Line and Ring Oscillators used in chapter 4. The sinusoidal noise on the supply causes plus or minus five percent variations to the supply voltage. In addition, both the positive and negative supplies were tested individually for each oscillator to determine if there was any change in the results as a function of which supply was being modulated.

7.1 Simulation Results for Supply Modulation

The results for the supply noise on the positive supply are shown in table 6 below. In addition, the results for the negative supply are shown in table 7.

Table 6 – Cycle Jitter with supply noise on positive supply

Oscillator	Cycle Jitter with supply noise at 50 MHz (sec.)	Cycle Jitter with supply noise at 1 GHz (sec.)
Colpitts	3.41E-12	7.57E-15
Hartley	4.56E-12	2.01E-14
Delay Line	3.65E-12	9.95E-15
Ring	1.30E-11	3.97E-12

Table 7 – Cycle Jitter with supply noise on negative supply

Oscillator	Cycle Jitter with supply noise at 50 MHz (sec.)	Cycle Jitter with supply noise at 1 GHz (sec.)
Colpitts	2.55E-13	6.55E-12
Hartley	4.68E-12	1.79E-14
Delay Line	1.27E-12	5.59E-12
Ring	1.37E-11	2.14E-12

These results show that for two oscillators, the Colpitts and Delay Line, there is a difference in measured cycle jitter depending on which supply is modulated. The other two oscillators, Hartley and Ring, showed similar results according to which supply was being modulated.

Because the Colpitts and Delay Line show greater discrepancy in supply jitter according to the supply being modulated, greater care would have to be taken to accurately model supply noise for a design. In the example above, supply noise on the positive supply causes greater cycle jitter on the output for these two oscillators.

However, when the supply noise is at 1 GHz, the cycle jitter is greater with supply noise on the positive supply.

These observations are due to the fact that with the tank circuitry tied to the positive supply, there is greater influence from lower frequency voltage fluctuations on the tank circuitry when the positive supply is modulated. Frequency modulation at the frequency of oscillation or higher affects the tank circuitry also but it causes a phase-locking effect which helps lower cycle jitter. However, since most devices that are being simulated are NMOS devices, the negative supply modulation affects the active parts of these circuits more since their substrates are usually tied to the negative supply.

7.2 Supply Noise Levels

As has been seen in previous results, a change of plus or minus five percent in the supply voltage can cause the magnitude of cycle jitter to increase by two or three orders of magnitude. The second part of this chapter deals with determining how much supply noise is necessary to have that noise become more influential in cycle jitter than device noise.

Previously it has been shown how measured cycle jitter depended on which supply was being modulated. For these tests, we will only test supply noise on the positive supply. It should be noted that different results would be achieved depending on which supply is modulated, but for the purposes of this thesis, the effect of positive supply modulation only will be shown.

The supply noise will be modulated at 50 MHz as in previous supply noise tests. To complete the testing process, device noise was first removed from the circuit. The supply noise was then adjusted until the cycle jitter was approximately equal to the cycle jitter with no device noise. This percentage of supply noise variation is shown in Table 8

along with the generated cycle jitter. The device noise is then added to the circuit and the cycle jitter is then measured again.

Table 8 – Supply noise modulation required to overtake device noise in overall effect on cycle jitter

Oscillator	Cycle Jitter with supply noise at 50 MHz (sec.)	Supply noise amplitude modulation (%)	Cycle Jitter with supply noise and device noise (sec.)
Colpitts	6.42E-15	6.66E-03	7.86E-15
Hartley	3.04E-14	3.33E-02	4.41E-14
Delay Line	1.41E-14	1.82E-02	1.38E-14
Ring	2.13E-13	8.18E-02	3.03E-13

These results show that with a lower amount of device noise, less supply noise modulation is necessary to overtake the device noise in cycle jitter effects. The Colpitts oscillator had the lowest noise modulation needed at .00667 percent of the supply voltage while the ring oscillator could accept the greatest supply modulation at .0818 percent of the supply voltage. It is also interesting that the Delay Line oscillator showed no change in cycle jitter from the case of supply noise or device noise individually included to the case when both noise sources were added.

With multiple independent random noise sources, the expected total variance would be the sum of the individual variances. It should be noted that even though the supply noise is not a random process, every oscillator except the Delay Line oscillator exhibits this effect.

7.3 Conclusion

In this chapter, the effect of sinusoidal supply noise on cycle jitter has been further investigated. The first experiment outlined was to see how supply noise on an individual supply would affect circuit performance. Then it was determined how much

supply noise was required on the positive supply to equal the amount of cycle jitter that device noise produced in the circuit.

It was determined that supply noise on the positive supply generally had greater influence on cycle jitter than at lower frequencies. Because the lower frequency fluctuations appear almost as DC changes to the oscillators, the noise causes greater bias changes in the tank and active circuitry. Similar results were seen and explained in chapter 6.

For higher frequencies, the supply noise on the negative supply had more of an influence. One reason for this is the tank circuitry, which is more directly coupled to the positive supply, can often become phase locked to the supply noise leading to less cycle jitter if the supply noise is also low jitter. A second reason is that the substrates of the active devices are often tied to the negative supply. This results in small but observable changes in the device operation leading to increased cycle jitter.

It was discovered how much supply noise is required to produce an equal amount of cycle jitter as was generated by device noise in the circuit. Generally, it was found that circuits with more device noise would tolerate increased amounts of sinusoidal noise to create equivalent amounts of cycle jitter. When device and supply noise were simulated together, it was found that the two noise sources showed characteristics of being independent of one another. The Colpitts oscillator was an exception and showed no increase in cycle jitter with both device and supply noise present. This might indicate that one of the noise sources is dependent on the presence of the other.

Chapter 8

Design Optimization Using Transient Simulation

Having established a process by which oscillators may be analyzed for noise performance, an attempt is now made to design a low-jitter oscillator using transient analysis. Given that a designer would have both frequency and time domains available to simulate an oscillator design, he could use the information provided from both domains to design his circuit accordingly. Since the emphasis of this thesis is on the analysis of transient noise, the simulation performed in this chapter will be mainly done in the time domain. Some information more readily obtained through frequency domain analysis will occasionally be used.

The Agilent ADS software package will be used for circuit analysis. The oscillator will be designed with the .25μm TSMC CMOS process that is available through Mosis.

8.1 Oscillator Enhancement

The basic circuit used for this design will be based on the Colpitts oscillator originally shown if Figure 9 in chapter 4. This circuit had low cycle jitter as determined from the tests conducted in chapter 4 and provides a good starting point for further improvement. Also, to make this circuit applicable to high frequency applications, a

buffer will be added to drive a 50-Ohm load as in chapter 5. A simplified schematic representation is shown in Figure 14.

Much study and research has been conducted in the field of oscillator phase noise and a plethora of theories have been put forth on how to minimize the noise. This chapter will look at some of the most important methods, as given by [23]. They are:

1. Make the signal power as large as possible
2. Make the resonator Q as large as possible
3. Use the minimum amount of active devices
4. Design the circuit so that energy is delivered to the resonant tank as instantaneously as possible
5. Have transistors remain off as much as possible, waking up only to deliver pulse of energy as needed
6. Deliver current to resonator during signal peak
7. Design the circuit to be symmetrical

Each of these qualifications is now examined individually to improve the basic oscillator design. Without any modifications the cycle jitter has been measured at 1.613E-13s with only device noise present. The oscillator is also adjusted with each modification to oscillate at 1 GHz.

First, we will make the signal power larger to improve cycle jitter. A frequency domain analysis of this circuit shows that the signal power for the circuit is presently –7.3dBm with a 50-Ohm load. If increasing the device sizing in the buffer stage increases the signal power to 0dBm and 6dBm the cycle jitter is lowered to 6.021E-14s and 2.18E-14s respectively. A disadvantage of adding extra output power is that it often increases the total power consumed by the oscillator. Ideally, we could make the oscillator signal

output have as much power as possible, but to keep the situation realistic, we will assume that to generate an output of 6dBm we use as much power as is available to us. In a real-life design situation, a designer would have to determine what trade-offs were appropriate for his design. The buffer will be adjusted with each design step to ensure that the same signal power is provided to the load to allow for fairer comparison of improvements.

The next qualification is that the resonator Q is high. Since it is usually assumed that the Q of an inductor is lower than the Q of a capacitor in modern integrated circuits, it is assumed that inductor Q is the predominant factor in determining the Q of the resonant circuit. In our original circuit design, it was assumed that the inductor Q is 15. With a completed layout, the designer would be able to extract the exact Q using an electromagnetic simulator. The layout could then be adjusted to maximize the Q of the circuit. Since a current layout has not been completed of this design, the inductor Q will be left at 15. The reader is referred to Chapter 6 for simulations involving the inductor Q to minimize cycle jitter.

An ideal oscillator would have the minimum amount of active devices. Active devices have both flicker and shot noise in addition to thermal noise, while passive devices have only thermal noise. Because of this, including passive devices instead of active devices to perform basic functions minimizes the noise of the circuit. A simple example of this would be to look at the active inductor oscillator, which is comprised mainly of active devices. Compare that circuit to either the Hartley or Colpitts oscillators that have more passive components. Since an oscillator must have a gain stage by definition, an oscillator with no active devices is not an option either because there is always some loss in the passive circuitry. The current oscillator design uses only two NMOS transistors: one for the gain stage and one for the buffer stage. Since removal of

one of these transistors is not possible and yet remain functional, no active devices can be further removed.

Next, to reduce phase noise it is desirable to supply current to the tank circuit as instantaneously as possible and to have the transistor remain off as much as possible. These two design guidelines are associated with each other because there is only one transistor supplying current to the tank circuit and it is supplying current whenever it is on. The amount of time that the current is being supplied to the tank is .61ns. Shown in Figure 21 is a plot displaying the current flow into the tank circuit.

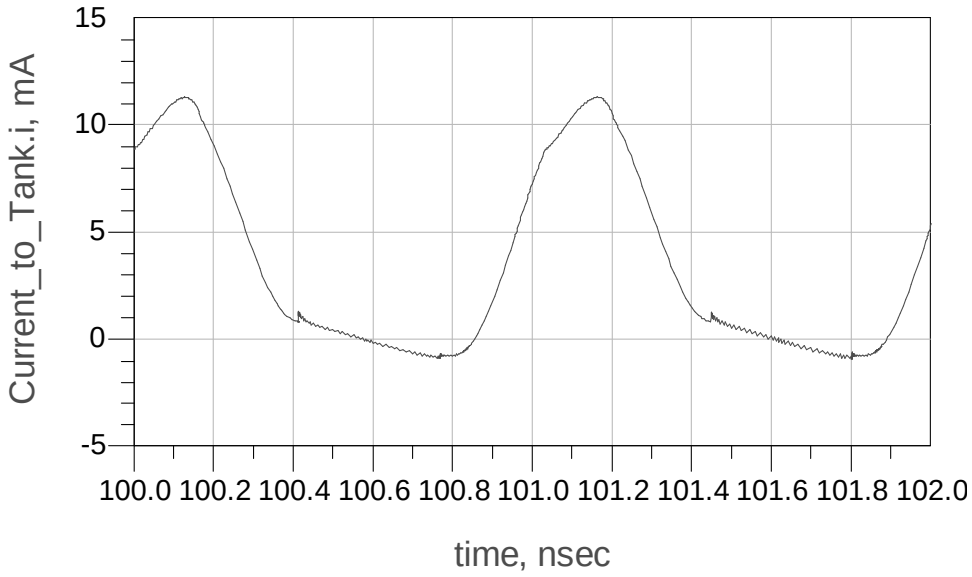

Figure 21 – Current delivered to the tank

In order for more performance enhancement, the ratio of the tapped capacitors is changed from 1:1 to 2:1. The time period that the transistor remains on is .61ns, however, it is not supplying as much current during the entire time the transistor is on. This can be seen in Figure 22. As a result, the cycle jitter is only 1.313E-14s.

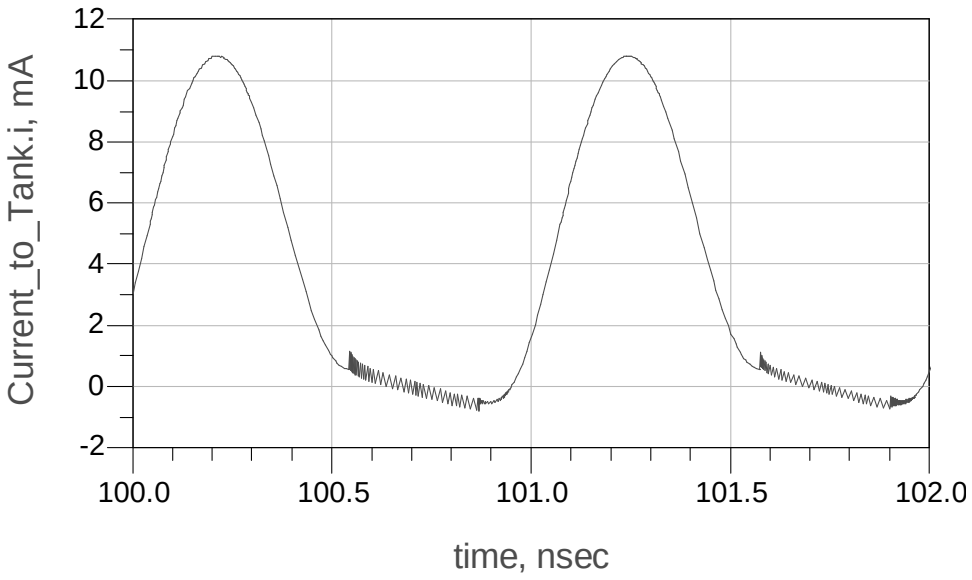

Figure 22 – Current delivered to the tank after capacitor modification

The next design guideline to reduce cycle-jitter is to deliver current to the resonator during signal peaks instead of during the signal transitions. This avoids jitter caused by the transistor switching on and off and interfering when the signal is transitioning. Supplying the current during signal peaks will increase amplitude noise, but as mentioned in chapter 2, this has much less effect than phase noise and is often filtered out. Figure 23 shows both the current to the resonant circuit and also the voltage at the resonator. As can be seen from the plots, the highest current values occur around the time the voltage peaks in the signal waveform and not during the middle of the signal transition. The current design will be deemed adequate and will not be optimized further.

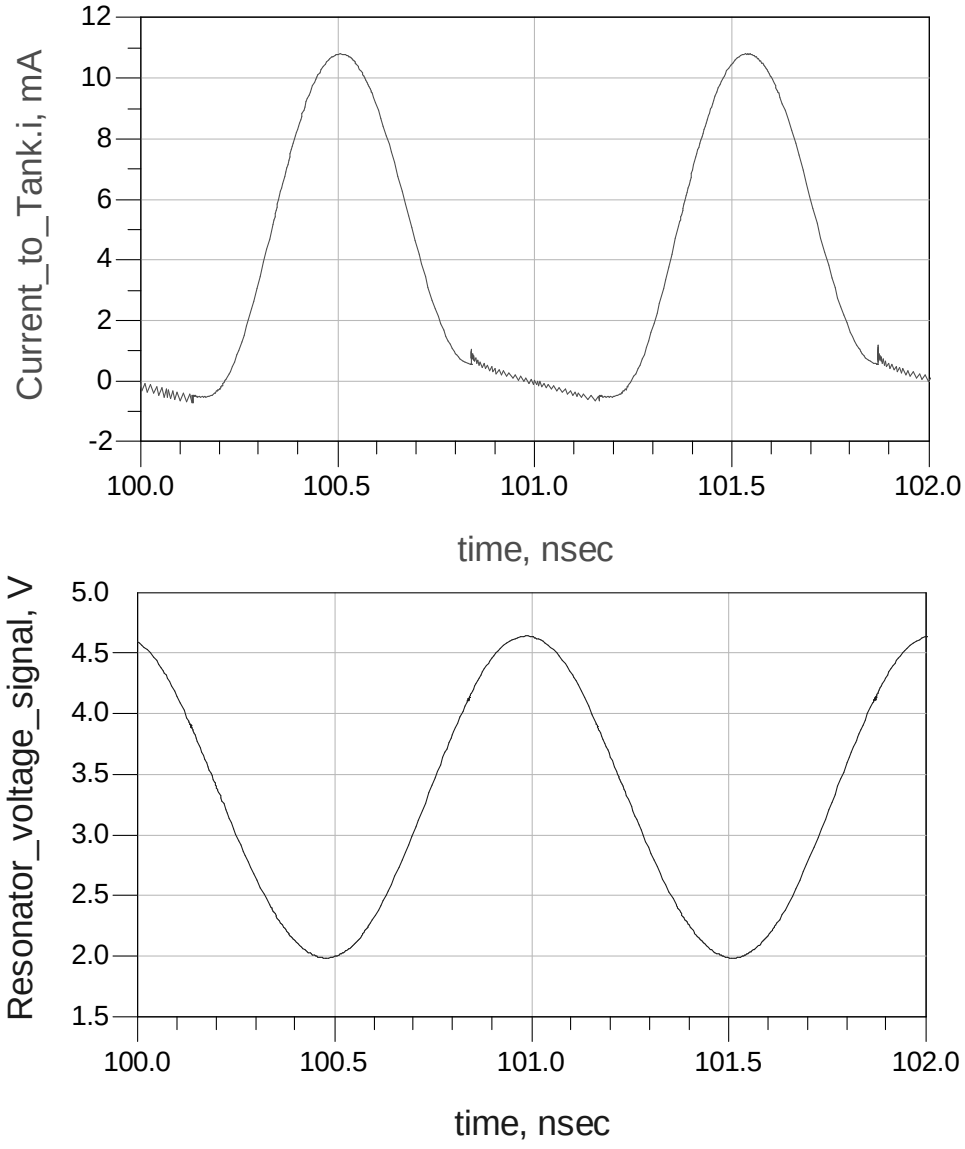

Figure 23 – Current to the tank and voltage of the tank circuit

The final design guideline to be implemented is to add symmetry to the circuit. To make this Colpitts oscillator symmetrical the oscillation circuitry and buffer are replicated allowing for either single ended or differential operation. A simplified schematic is shown in Figure 24. When simulated single-endedly this design was measured with a cycle jitter of 1.711E-14s. But when the outputs are taken differentially

the cycle jitter is reduced to 1.268E-14s. This cycle jitter represents only 8 percent of the original cycle jitter.

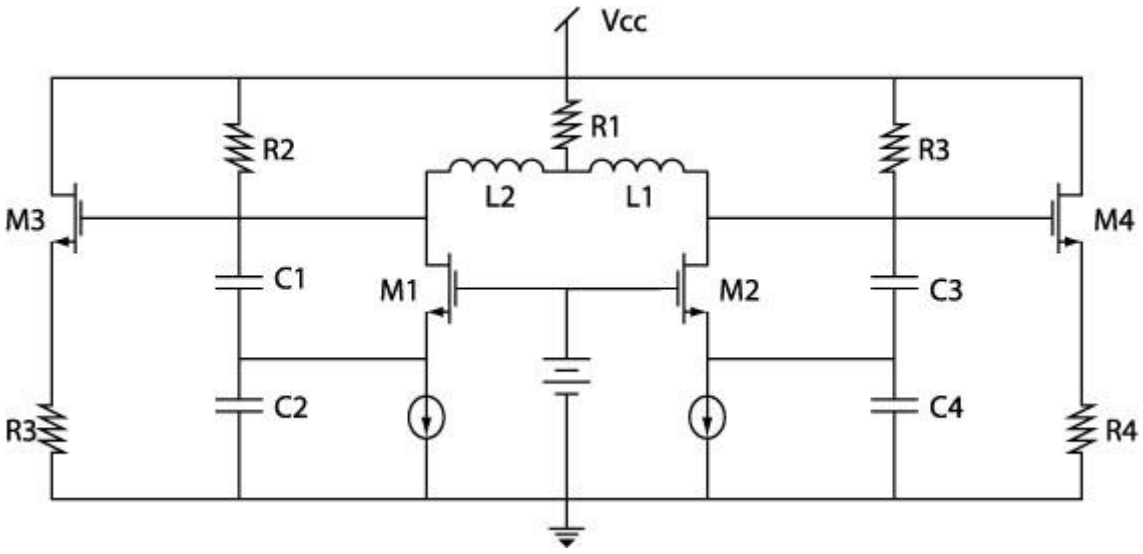

Figure 24 – Differential Colpitts oscillator schematic

This design enhancement process demonstrates how transient simulations may be employed to optimize an oscillator for phase noise performance. Some steps like output noise power optimization can be performed in the frequency domain, but other steps were best accomplished in the time domain. An example of this would be minimizing the current flow to the resonator circuit. This can easily be accomplished by analyzing the transient plot of the current.

8.2 Summary

Given the fact that a circuit may be analyzed in the time domain, a process is shown where a design is optimized to reduce cycle jitter. Several design guidelines suggested previously have been utilized in the circuit design and then verified using

transient noise simulation. As a result the noise has been reduced by a factor of 12 from 1.613E-13s to 1.268E-14s.

To achieve even greater accuracy in simulation, the designer may complete the layout and extract any parasitics that occur in the circuit to ensure the highest possible design verification.

Chapter 9

Conclusion

Using the techniques developed in this thesis, several conclusions regarding jitter performance for oscillators have been arrived at. First, in order to gain more understanding in the design of an oscillator for low noise, both time and frequency domain simulations must be utilized.

It has been shown that, in general, passive device oscillators can have as much as 7 times less cycle jitter than active device oscillators with only device noise being simulated. With supply noise added, the passive oscillators also had 3 times less cycle jitter.

For a long time, it had been know that the flicker noise of bipolar devices has been less than that of CMOS devices but previously no time domain noise comparison has been done. The simulations in this thesis demonstrate that in the simulated Colpitts oscillator, the design with the bipolar devices had 8 times less cycle jitter than the CMOS equivalent circuit.

It has also been shown that a higher inductor Q generally reduces the effects of supply noise on cycle jitter. For frequencies greater than the oscillation frequency, a

change in inductor Q from 10 to 40 reduced cycle jitter about 8 and 27 percent respectively in the two cases measured.

In addition, this thesis has shown how much supply noise can be tolerated before its effect on cycle jitter begins to overshadow the device noise. Oscillators with greater device noise could tolerate more supply variation. However, it was observed that for every oscillator tested, less than .1 percent supply modulation would lead to a greater amount of cycle jitter resulting from supply noise instead of device noise.

A process has been demonstrated where an oscillator has been optimized utilizing time domain noise simulation. The original Colpitts oscillator design had 1.613E-13s in cycle jitter before modifications. By implementing several general design guidelines given in [23] and analyzing the transient simulations, the cycle jitter of the new oscillator was reduced to 1.268E-14s. This cycle jitter represents only 8 percent of the cycle jitter measured in the original circuit.

In past years, this ability to add noise to a transient simulation was not widely available. This thesis has also shown two methods whereby a designer may simulate transient noise: one specific to ADS and the other applicable to any circuit simulator, thereby allowing for more accurate analysis of circuit noise. Agreement has been demonstrated between the two methods using the case of thermal noise in a resistor.

Chapter 10

Further work

This thesis has explored ways that time domain simulations may be used to provide a more comprehensive view of oscillator jitter performance. Further work that could be done to extend this research is:

1. Verification of the time domain noise simulations through measurements of actual circuits in silicon.
2. Addition of extracted layout parasitics to design for more precise simulation and optimization of noise performance derived from physical effects.
3. Analytical method to evaluate cycle jitter from phase noise given nonlinear aspects of the phase noise spectrum (spurs, flicker noise, etc.).
4. Generation of design kits using “BYU” method for time domain noise generation in EDA software not yet including transient noise simulation.
5. Development of better jitter test methods that correlate with the time domain techniques presented.
6. Further investigation into rms jitter as a function of measurement time as discussed in [13], and generation of ADS or “BYU” method simulations that show similar results.

Appendix

Appendix

The source of this code was originally written by David Dai [30]. Some modifications have been made to allow for incorporation into the noise generation method discussed in this paper.

```
format short g; %to avoid long e
TLENGTH =5000; %PSPICE final time with unit of ns
TUNIT =10/10; %PSPICE time step with unit of ns and number of points in each time step
DNUM = TLENGTH/TUNIT; %number of signal point wanted
randn('state', sum(100*clock)); %give a random state to start
data=randn(DNUM,1); % get an array of random number with rms of 1.
data_initial=0;

fn = fopen('data.stl', 'w');
%header of the stimulus file
fprintf(fn, '.STIMULUS din1 PWL\n');%this defines the stimulus name
fprintf(fn, '+ TIME_SCALE_FACTOR = 1\n');
fprintf(fn, '+ VALUE_SCALE_FACTOR = 1\n');

fprintf(fn, '+  (0, %6.4f)\n', data_initial);
```

```
for k=1:DNUM
fprintf(fn, '+  (%6.4fe-009,  %8.6f)\n', k*TUNIT, data(k,1)*1 );%scale to get proper rms
value
end


fclose(fn);
```

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